ECE102 - Digital Circuit Logic - spring 2020

Instructor: Prof. Mahdi Nikdast (http://www.engr.colostate.edu/~mnikdast/)
Email: Mahdi.Nikdast@colostate.edu
Office Hours: Tuesday (16:00 to 17:00) & Wednesday (14:00 to 15:00); walk-in subject to availability
Office: C103A Engineering Building

Teaching Assistants and Grader:

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Office hours and Contact Info.</th>
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<tbody>
<tr>
<td>Ms. Gunjan Mahindre</td>
<td>Graduate Teaching Fellow</td>
<td>Wednesday: 10:00 to 11:00 Thursday: 09:00 to 10:00&lt;br&gt;&lt;em&gt;Location: C207&lt;/em&gt;&lt;br&gt;<a href="mailto:gunjansp20ece102@gmail.com">gunjansp20ece102@gmail.com</a></td>
</tr>
<tr>
<td>Ms. Pricilla Vasquez</td>
<td>Teaching Assistant</td>
<td>Monday: 11:40 to 12:40 Wednesday: 11:00 to 12:00&lt;br&gt;&lt;em&gt;Location: C207&lt;/em&gt;&lt;br&gt;<a href="mailto:priscilla.sp20.ece102@gmail.com">priscilla.sp20.ece102@gmail.com</a></td>
</tr>
<tr>
<td>Ms. Maxine Smith</td>
<td>Course Assistant (Grader)</td>
<td>Monday: 14:30 to 16:00&lt;br&gt;&lt;em&gt;Location: BC Infill&lt;/em&gt;&lt;br&gt;<a href="mailto:maxsmi@rams.colostate.edu">maxsmi@rams.colostate.edu</a></td>
</tr>
<tr>
<td>Mr. Ben Fox</td>
<td>Learning Assistant</td>
<td>Monday: 12:15 to 14:00 Tuesday: 10:45 to 12:30 Tuesday: 16:30 to 18:00 Thursday: 13:45 to 15:15&lt;br&gt;&lt;em&gt;Location: BC Infill&lt;/em&gt;&lt;br&gt;<a href="mailto:benfox98@rams.colostate.edu">benfox98@rams.colostate.edu</a></td>
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Lectures: Tuesday, Thursday 12:30 - 13:45, Clark A103

Objectives: To understand the concepts of digital logic and learn methods and tools for the design of digital circuits.

Prerequisites: Major in ECE or prior approval.

URL: The official home page for ECE102 is Canvas. Students are expected to visit the official home page frequently for class handouts, homework assignments, lab assignments, and important announcements!
Grading Policy: The grade will be based on

<table>
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<tr>
<th>Component</th>
<th>Weight</th>
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<tr>
<td>Homework (Every week)</td>
<td>20%</td>
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<tr>
<td>Labs (13 in total)</td>
<td>25%</td>
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<tr>
<td>iClicker Quizzes</td>
<td>10%</td>
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<tr>
<td>Midterm 1 (Feb. 28, 2020)</td>
<td>15%</td>
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<tr>
<td>Midterm 2 (Apr. 10, 2020)</td>
<td>15%</td>
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<tr>
<td>Final Exam (May 11, 2020)</td>
<td>15%</td>
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The +/- grading scheme will be used, with the scale

<table>
<thead>
<tr>
<th>Grade</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>&gt;95%</td>
<td>90-94%</td>
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<tr>
<td>85-89%</td>
<td>80-84%</td>
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<tr>
<td>75-79%</td>
<td>70-74%</td>
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<tr>
<td>65-69%</td>
<td>64-54%</td>
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<tr>
<td>55-64%</td>
<td>40-54%</td>
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<tr>
<td>&lt;40%</td>
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iClicker Quizzes: During the lectures (and mostly at the beginning of each lecture), there will be several in-class quizzes using iClickers. iClicker quizzes cover the material taught on the same day of the lecture OR to review materials delivered in the previous lecture. Therefore, it is very important to attend the lectures to take part in iClicker quizzes, which account for 10% of the final course grade. Finally, there will be a few online quizzes/assignments (with some bonus credits) related to a project on diversity and inclusion in engineering criteria.

Homework Procedures: Homework assignments are due online (must be submitted on Canvas). Selected questions from each homework assignment will be graded. However, turn in ALL of the assigned problems. All assigned problems are equally important for the development of your understanding of the subjects of digital logic. To receive full credit for your homework, show ALL reasonable steps in solving the problem. Written solutions will be available in the lab/online after the due date of the homework. Make sure the file you submit to Canvas is readable, otherwise the course grader may not grade your assignment.

Late Policy: Quizzes and Exams must be taken as scheduled in order to receive credit. Late homework will not be accepted unless its lateness is due to circumstances beyond your control (official proof is required). To receive full credit, lab reports must be submitted online through Canvas on/before the date due. Late lab reports will be accepted, but points will be deducted from the score (see penalties below).

Lab Assignments and Attendance: Laboratory assignments are a very important component of this course. You will learn to design and develop digital logic circuits, and by the end of the semester, will be able to design sophisticated digital circuits. We use a set of digital tools used by professional engineers, which may appear a bit intimidating at first. After the first two to three labs, you will become comfortable with the tools and will be on your way to designing some interesting circuits.

- You must pass EVERY lab assignment with score > 60% to pass the course.
- Lab attendance: Mandatory. In rare situations when you cannot attend your scheduled lab session due to circumstances beyond your control, you must obtain clearance.
in advance from your lab instructor. In such a case, you must attend another lab section
during that same week. Failing that, you will be marked absent for the project and will
receive a penalty (-5%). Remember that all projects must be completed with a passing
grade in order to pass the course (i.e., >60%).

- **Conduct in the lab:** Students are expected to maintain a professional working atmosphere
  in the lab, which includes not disturbing other students or groups, not talking loudly, and
  following additional instructions provided by the Teaching Assistants. **Use of cellphones**
  (for voice or texting) is not allowed. **No food or drinks allowed in C207. TAs are**
  **responsible to report any misconduct or unprofessional behavior to the instructor for**
  **further actions.**

- **Prelab:** Prelabs must be submitted online at the beginning of corresponding lab sessions.
  This prelab must be included in your lab reports every week.

- **Demonstration of hardware circuits & Submitting Project reports:** You may show the
  hardware demo anytime before the start date of the next project for your lab section (during
  GTA's office hours or during other lab sections). At the time of the demo, you must present
  your circuit diagram built using Quartus software. Your lab instructor will confirm this
diagram once she/he has seen your hardware circuit working correctly. The circuit diagram
should then be incorporated into your project report. Demonstrating your hardware circuit
during the next lab meeting is permitted, but make sure that it works flawlessly. You will
not be given extra time to debug your circuit at that time. **No excuses will be entertained**
in this regard.

- **Policy on collaboration with other students:** Design alone, build alone, write alone, and
  submit individually prepared reports and circuits. It is fine to talk, give advice, receive
  advice, but do your own work.

- **Grading policy:** The grading differs from one project to the other. An example would be:
hardware circuit: 30%, required technical items in the report: 40%, memo text: 20%,
instructor discretion: 10%. A neatness bonus of 5% may be assigned.

- **Penalties:** Penalties will be assessed for each lab report (except where specifically
  allowed): -5% for not attending the lab session, -5% for missing prelab, -2.5%-per-day for
  late submission, and -10% for not following Banana memo format.

**Conduct and Nature of Exams:** You will be allowed to use one double-sided page of notes,
prepared by you, during the three exams. Exams will be straightforward, but will demand the kind
of preparation only possible through continual, daily study.

**Instructional Objectives:** Given during class, these are the bases of all quiz and exam
questions, and homework assignments. For this reason, consistent class attendance is very
important.

**Textbook:** Fundamentals of Logic Design, by Charles H. Roth published by Cengage
Learning. The latest is the 7th Edition. Sixth, fifth or fourth editions are acceptable.
Some of these earlier editions were published by Thompson Publishing Co. Be aware that there are differences in chapter, page and problem numbers of the
different editions. CSU Bookstore carries a paperback version containing the necessary chapters
of the 7th edition at a lower price compared to the regular version. It is not critical to have the text during the first week.
**Tutoring:** The course's Graduate Teaching Assistants will be available for drop-in consultation as well as help sessions at times and places listed on the website.

**Academic Integrity:** This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (http://www.conflictresolution.colostate.edu/academic-integrity) and the Student Conduct Code (http://www.conflictresolution.colostate.edu/conduct-code). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services. **My policy is that of zero tolerance.** Minor first infraction in HWs and Lab reports will lead to a zero score (-40% for Lab assignments) as well as one letter level (e.g., A to B) reduction in the course grade. Project or Major or repeated infractions in HWs and Lab reports will result in “F” grade for the course as well as reporting to the Dean’s Office. Any misconduct in an exam (e.g., cheating) will lead to a zero score for that exam, and very likely, course failure.

All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one’s own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken.

**Diversity Statement:** As the instructor in ECE102, I am deeply committed to helping build an inclusive culture in this classroom, in the Department of Electrical and Computer Engineering, in the Walter Scott, Jr. College of Engineering, and at CSU. Each individual brings diversity to our class in the identities they hold, the ways they think, their interests and skills, their background and past experiences. To me, inclusion means not only accepting these differences, but embracing them and understanding that we can leverage these differences to be better engineers.

My goal for this class is to create an environment where we do not discriminate against individuals because of their identities (e.g., race, ethnicity, sex, gender identity, sexual orientation, religion, nationality, age, levels of ability). It is also important to understand that even when we hold egalitarian beliefs, we can hold implicit or unconscious biases that can also influence the way we treat others or approach engineering design. It is my expectation that students in this class will:

1. Adhere to the CSU Principles of Community https://diversity.colostate.edu/principles-of-community/;
2. Work in teams in ways that recognize the contributions of all team members and provide all team members the opportunity to learn;
3. Examine their own behaviors and refrain from acting in biased ways;
4. Reflect on the ways bias can influence engineering work;
5. Speak with the professor when biased behaviors may occur from other students, their TAs, and the professor;
6. Be sensitive to context and acknowledge that hurtful comments can sometimes be inadvertent but they still have an impact.
Topics (Dates/Topics may change with reasonable notice):

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<tr>
<th>Week</th>
<th>Course Objectives</th>
<th>Readings</th>
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| W1 (Jan. 20 – Jan. 24) | **Introduction to digital systems**  
- State the differences between analog and digital systems                                                                                                  | N/A      |
| W2 (Jan. 27 – Jan. 31) | **Binary representation of information**  
- Define the term “positional number system”  
- Represent numbers in decimal, binary, octal and hexadecimal notations and convert from one notation to the other  
- Add, subtract, multiply and divide binary numbers  
- Represent numbers in sign-magnitude, one's complement and two's complement forms  
- Carry out addition and subtraction, and identify overflow conditions  
- Represent numbers in binary coded decimal format (BCD)  
- Represent characters using ASCII format | Ch. 1    |
| W3 (Feb. 3 – Feb. 7) W4 (Feb. 10 – Feb. 14) | **Boolean Algebra and Combinational Logic**  
- Define the basic logic operations (AND, OR, NOT)  
- Evaluate Boolean expressions  
- Derive the logic function implemented by a combinational logic circuit  
- Use Laws and Theorems of Boolean Algebra to simplify logic expressions  
- Find the complement of a Boolean expression using DeMorgan's Law  
- Find the dual of a Boolean expression  
- State and use the Negative Logic Theorem  
- Use Consensus theorem to simplify logic expressions  
- Implement Boolean expressions using 2-level networks (SOP, POS) | Ch. 2    |
|               | W5 (Feb. 17 – Feb. 21) | **- Convert functional specifications (written in English) to logic expressions**  
- Convert specifications written in English to a truth table  
- Write a logic expression as a minimum POS, minimum SOP, canonical POS and a canonical POS  
- Design logic circuits to add/subtract two's complement numbers  
- Obtain minterm and maxterm expansions (using m/M notations or in algebraic form) from a truth table or an algebraic expression | Ch. 4    |
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<th>Week</th>
<th>Tasks</th>
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<td>W6 (Feb. 24 – Feb. 28)</td>
<td>- Convert a minterm expansion into a maxterm expansion and vice versa&lt;br&gt;- Use m/M notation to obtain product/sum of logic expressions&lt;br&gt;- Find the minterm and maxterm expansions of $F'$, $F \cdot G$, $F + G$ where $F$, $G$ are Boolean functions&lt;br&gt;Hardware for Arithmetic&lt;br&gt;- Design logic circuits to add/subtract two's complement numbers&lt;br&gt;- Design an array multiplier for binary integers&lt;br&gt;- Use don't care terms to simplify logic expressions&lt;br&gt;- Represent 3, 4, 5, and 6 variable functions using K-maps&lt;br&gt;- Represent expressions given in SOP, POS, maxterm or minterm form on K-maps&lt;br&gt;- Obtain minimum POS and SOP expansions using K-map&lt;br&gt;- Design multiple output circuits using K-maps&lt;br&gt;- Represent 5 and 6 variable functions using K-maps and obtain minimum SOP, POS&lt;br&gt;Midterm 1 (February 28, 2020)</td>
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<td>W7 (Mar. 2 – Mar. 6) W8 (Mar. 9 – Mar. 13)</td>
<td>- Implement logic functions using multilevel networks&lt;br&gt;- Derive alternative gate symbols for basic logic gates&lt;br&gt;- Implement logic functions using basic 2-level forms (NAND-NAND, AND-OR, etc.)&lt;br&gt;- Convert networks from one form to another&lt;br&gt;- Implement logic functions using only NOR gates or only NAND gates&lt;br&gt;- Describe the operation of tri-state logic gates, multiplexers and decoders&lt;br&gt;- Implement logic functions using multilevel networks&lt;br&gt;- Design multiple-output circuits&lt;br&gt;- Implement combinational logic expressions using multiplexers, decoders, ROMS and programmable logic&lt;br&gt;Ch. 5&lt;br&gt;Ch. 7&lt;br&gt;Ch. 8&lt;br&gt;Ch. 9</td>
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<td>W9 (Mar. 16 – Mar. 20)</td>
<td>Break (No class)</td>
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<td>W10 (Mar. 23 – Mar. 27) W11 (Mar. 30 – Apr. 3)</td>
<td>Sequential Circuits&lt;br&gt;- Describe the operation of S-R, T, D, and J-K latches and flip-flops&lt;br&gt;- Draw timing diagrams of circuits containing latches and flip-flops&lt;br&gt;- Draw the circuit diagram, and describe the operation of registers, shift registers, cyclic shift registers, etc&lt;br&gt;Ch. 11&lt;br&gt;Ch. 12</td>
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<td>Week</td>
<td>Dates</td>
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<td>W12</td>
<td>Apr. 6 – Apr. 10</td>
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<td>W13</td>
<td>Apr. 13 – Apr. 17</td>
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<td>W14</td>
<td>Apr. 20 – Apr. 24</td>
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<td>W15</td>
<td>Apr. 27 – May 1</td>
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<td>W16</td>
<td>May 4 – May 8</td>
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