Manycore CPU/GPU Chip Design

- Nearly all modern innovations depend on continued advances in manycore computing (CPU/GPU) chip performance.
- Major impact on innovation across application domains: automotive, defense, medical, multimedia, telecommunications, aerospace, embedded computing.
- But manycore chip design in advanced semiconductor fabrication technologies today creates new design challenges:
  - High power density, die temperature, power-consumption concerns.
  - Increasing multithreaded, multi-core, multi-tasking workloads.
  - Increasing demand for performance vs scalability.

Machine Learning (ML) Accelerators: Hardware/Software CoDesign

- Conventional hardware accelerators for AML are increasing limited by Dennard scaling slowdown.
- NoCs have replaced on-chip buses, but face challenges:
  - High scalability for ever-decreasing interconnection delays on-chip.
  - Need to solve multiple gate delay vs. routing design constraints.
  - How to balance NoC protocols and adaptation.
  - Runtime macromodeling for system-level performance.
- Fault-tolerant NoC protocols and adaptation.
  - New paradigm: optical AML accelerators.
  - Chip-scale photonic networks.
  - Light-speed communication and data processing.

Network-on-Chip Architecture Design

- Efficient Energy Harvesting IoT Platforms

- Energy-Efficient Mobile Computing

- Robust Real-Time Autonomous Platforms

- Sustainable Datacenter Computing

- Embedded System and IoT Application Prototypes

- Collaboration/Research Opportunities

- Mission: Design of innovative software algorithms, hardware architectures, and hardware-software co-design techniques for energy-efficient, fault-tolerant, real-time, and secure computing across embedded/IoT systems, cyber-physical systems, and HPC/datacenters.