VITA – SUDEEP PASRICHA

November, 2020

Highlights

- **R&D Accomplishments:** Performed some of the first groundbreaking research on the design of energy-efficient and reliable communication/memory architectures and CAD tools for multi-core processing chips found in all embedded/IoT, mobile, and high performance computing systems; the resulting outcomes have been integrated into commercial products by many semiconductor companies (e.g., Intel, Fujitsu, Conexant, STMicroelectronics). Conducted seminal research towards realizing energy-efficiency and robustness in high performance computing systems such as datacenters and supercomputers; the outcomes have been deployed in large-scale computing clusters at Oak Ridge National Laboratory (ORNL) and the Department of Defense (DoD).
- **Research Funding:** Over $6M in funding from NSF, DOE, AFOSR, SRC, DoD/ORNL, NASA, Monfort, Rockwell, and FCA, and over $1M in equipment grants from industry.
- **Publications:** Over 200 peer-reviewed publications in IEEE/ACM conferences (20-30% acceptance rates) and journals. More than 4000 citations, h-index: 32, and i10-index: 109. *7 Best Paper Awards* (ACM/IEEE NOCS ’18, ACM GLSVLSI ’18, ACM SLIP ‘16, ACM GLSVLSI ‘15, IEEE AICCSA ‘11, IEEE ISQED ‘10, IEEE/ACM ASPDAC ‘06), *6 Best Paper Finalist* selections (ACM GLSVLSI’20, IEEE/ACM NOCS’18, IEEE TMSCS’17 journal, IEEE SCNS ’16, IEEE ISQED ‘16, IEEE/ACM DAC ‘05), and *1 Best Poster Award* (FCRC HPC Symp. ‘11)
- **Selected Honors and Awards:** George T. Abell Outstanding Faculty Research Award, 2019. ACM SIGDA Distinguished Service Award, 2019. Mid-Career Research Achievement Award, IEEE-CS Technical Committee on VLSI (TCVLSI), 2018. CSU Walter Scott, Jr. College of Engineering Rockwell-Anderson Professorship, 2016-2019. CSU Monfort Professorship 2016-2018. Award for Excellence for Mid-Career Researcher, IEEE Technical Committee on Scalable Computing (TCSC) 2015. George T. Abell Outstanding Mid-Career Faculty Award at CSU 2014. Air Force Office of Scientific Research (AFOSR) Young Investigator Award 2013. Honorary Affiliate Faculty Member at the Center for Embedded and Cyber Physical Systems (CECS) 2013.
- **Student Advising:** Graduated 10 PhD and 25 MS students. Currently advising 10 PhD students and 3 MS students. Have supervised 39 senior design projects at CSU (total: 107 undergraduate students), 14 ViP students, 9 Honors thesis, and 10 high school interns. Student Awards: Best Poster Award, IEEE/ACM DAC PhD Forum (2019); First place, CSU Engg. Days Competition (2013, 2012); Best senior design project ECE student awards (2015, 2014); CSU IEEE Open Design Competition First Place Award (2013); IEEE Region 5 Best Undergrad Paper Award (2012); NASA Space Grant Symp. First Place (2009).
- **Collaborations:** Collaborated with numerous industry partners and government labs including: Broadcom, Double Black Imaging, HP, Fiat-Chrysler, Conexant, Fujitsu, Intel, Keysight, Micron, NASA, Oak Ridge National Lab (ORNL), STMicro, Synopsys, and Woodward. National and international collaboration with prominent universities and research institutes.
- **Professional Service:** Senior Associate Editor, ACM JETC (2019-). Currently serving on Editorial Board of 4 journals (IEEE TCAD, ACM TECS, IEEE D&T, IEEE CM). General Chair for 2020 NOCS, 2019 HCW, 2018 IGSC, 2018 iSES, and 2017 ICESS; Program Chair for 2019 NOCS, 2019/2018 CODES+ISSS, 2018 VLSID, 2018 HCW, 2017 IGSC, 2017 iNIS. Served on Steering Committee of 3 major IEEE conferences; Organizing Committee of 34 international IEEE/ACM workshops and conferences; Technical Program Committee of 78 international IEEE/ACM workshops and conferences; Session Chair for 23 IEEE/ACM workshops and conferences. Senior Member of the IEEE and ACM.

Personal Information

Contact Information

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Professional Experience

2019 - current	Colorado State University Professor, Department of Electrical and Computer Engineering Professor, Department of Computer Science (Courtesy Appointment)	Fort Collins, CO
2016 - 2019	Colorado State University Walter Scott Jr. College of Engineering Rockwell-Anderson Professor	Fort Collins, CO
2016 - 2018	Colorado State University University Monfort Professor	Fort Collins, CO
2014 - 2019	Colorado State University Associate Professor, Department of Electrical and Computer Engineering Associate Professor, Department of Computer Science (Courtesy Appointment)	Fort Collins, CO
2008 - 2014	Colorado State University Assistant Professor, Department of Electrical and Computer Engineering Assistant Professor, Department of Computer Science (Courtesy Appointment)	Fort Collins, CO
2005 - 2008	Center for Embedded Computer Systems Graduate Research Assistant	Irvine, CA
2003 - 2005	Conexant Systems Inc. Design Engineer Intern	Newport Beach, CA
2002 - 2003	University of California, Irvine	Irvine, CA

	Research and Teaching Assistant	
2000 - 2002	STMicroelectronics Inc. Associate Design Engineer	Noida, India/Crolles, France

Education

2008	University of California, Irvine Ph.D. in Computer Science Doctoral Dissertation: "COMMSYN: On-Chip Communication Architecture Synthesis for Multi-Processor System-on-Chips" Advisor: Nikil Dutt	Irvine, CA
2005	University of California, Irvine M.S. in Computer Science Advisor: Nikil Dutt	Irvine, CA
2000	Delhi Institute of Technology B.E. in Electronics and Communications Engineering	Delhi, India
1996	St. Columbas High School High School	Delhi, India

Awards and Honors

2020	Best Paper Award Honorable Mention (Top 3 selection). ACM Great Lakes Symposium on VLSI (GLSVLSI), for the paper: *F. Sunny, A. Mirza, I. Thakkar, S. Pasricha, and M. Nikdast, "LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip"*
2019	WSCOE George T. Abell Outstanding Faculty Research Award
2019	Invited Panelist, Heterogeneous Computing for Energy Efficiency, IEEE International Green and Sustainable Computing Conference
2019	ACM SIGDA Distinguished Service Award
2018	Selected for Researcher Spotlight, ACM SIGDA Newsletter, September 2018.
2018	Research on Smartphone-based Indoor Navigation highlighted in the IEEE Signal Processing Magazine, Sep 2018, in the article "Signal Processing Opens the Internet of Things to a New World of Possibilities"
2018	Best Paper Award, IEEE/ACM International Symposium on Networks-on-Chip (NOCS), for the paper: *Y. Raparti, S. Pasricha, "DAPPER: Data Aware Approximate NoC for GPGPU Architectures"*

2018 Shortlisted for Graduate Advising and Mentorship Award at CSU

2018 Mid-Career Research Achievement Award, IEEE Computer Society Technical Committee on VLSI (TCVLSI).

2018 Best Paper Award, ACM Great Lakes Symposium on VLSI (GLSVLSI), for the paper: *A. Mittal, S. Tiku, S. Pasricha, "Adapting Convolutional Neural Networks for Indoor Localization with Smart Mobile Devices"*

2017 Best Journal Paper Award Finalist, IEEE Transactions on Multi-Scale Computing Systems (TMSCS), for the paper: *Y. Raparti, N. Kapadia, S. Pasricha, "ARTEMIS: An Aging-Aware Runtime Application Mapping Framework for 3D NoC-based Chip Multiprocessors"*

2017 Featured Paper, IEEE Transactions on Multi-Scale Computing Systems (TMSCS), April-June Issue: *Y. Raparti, N. Kapadia, S. Pasricha, "ARTEMIS: An Aging-Aware Runtime Application Mapping Framework for 3D NoC-based Chip Multiprocessors"*

2016 Best Paper Award Finalist, IEEE Smart Cloud Networks & Systems Conference (SNCS) for the paper: *Y. Biran, S. Pasricha, G. Collins, J. Dubow, "Enabling Green Content Distribution Network by Cloud Orchestration"*

2016 Best Paper Award Finalist, IEEE International Symposium on Quality Electronic Design (ISQED) for the paper: *S. V. R. Chittamuru, I. Thakkar, S. Pasricha, "Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures"*

2016 Selected as a Distinguished Rockwell-Anderson Professor for Outstanding Mid-Career Faculty in the College of Engineering at Colorado State University

2016 Best Paper Award, ACM System Level Interconnect Prediction (SLIP) Workshop, for the paper: *I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects"*

2016 Selected as a Distinguished Monfort Professor at Colorado State University for Excellence in Research, Teaching, and Mentoring by the Office of the Provost

2015 Keynote Talk, IEEE Workshop on Low-Power Dependable Computing (LPDC) on *"Integrated Photonics in Future Multicore Computing: New Directions in Dependability and Power Efficiency"*

2015 ACM Special Interest Group on Design Automation (SIGDA) Service Award

2015 Award for Excellence for a Mid-Career Researcher, IEEE Technical Committee on Scalable Computing (TCSC)

2015 Best Paper Award, ACM Great Lakes Symposium on VLSI (GLSVLSI), for the paper: *S. V. R. Chittamuru, S. Desai, S. Pasricha, "A Reconfigurable Silicon-Photonic Network with Improved Channel Sharing for Multicore Architectures"*

2014	George T. Abell Outstanding Mid-Career Faculty Award, Colorado State University
2013	Elevated to ACM Senior Member status
2013	Elevated to IEEE Senior Member status
2013	Honorary Affiliate Faculty Member, Center for Embedded and Cyber Physical Systems
2013	AFOSR Young Investigator Award (1 out of 40 scientists in the USA selected)
2012	ACM Special Interest Group on Design Automation (SIGDA) Technical Leadership Award
2011	Best Paper Award, ACS/IEEE International Conference on Computer Systems and Applications (AICCSA) for the paper: *J. Apodaca, D. Young, L. Briceno, J. Smith, S. Pasricha, A. Maciejewski, H. Siegel, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou, "Stochastically Robust Static Resource Allocation for Energy Minimization with a Makespan Constraint in a Heterogeneous Computing Environment"*
2011	Best Poster Award, Front Range High Performance Computing Symposium, for the poster: *D. Young, J. Apodaca, L. Briceno, J. Smith, S. Pasricha, A. Maciejewski, H. Siegel, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou, "Energy-Constrained Dynamic Resource Allocation in a Heterogeneous Computing Environment"*
2010	Best Paper Award, IEEE International Symposium on Quality Electronic Design (ISQED) for the paper: *S. Bahirat, S. Pasricha, "UC-PHOTON: A Novel Hybrid Photonic Network-on-Chip for Multiple Use-Case Applications"*
2008	Bob and Barbara Kleist Outstanding PhD Dissertation Award
2006-07	Joseph Fischer Memorial Award for Outstanding Achievement in Computer Science
2006	Best Paper Award, ACM/IEEE Asia South Pacific Design Automation Conference (ASPDAC) for the paper: *S. Pasricha, N. Dutt, M. Ben-Romdhane, "Constraint-Driven Bus Matrix Synthesis for MPSoC"*
2005	Best Paper Award Finalist, Design Automation Conference (DAC) for the paper: *S. Pasricha, N. Dutt, E. Bozorgzadeh, M. Ben-Romdhane, "Floorplan-aware Automated Synthesis of Bus-based Communication Architectures"*
2005	DAC Student Mentor Award, Design Automation Conference (DAC)
2004-07	Center for Pervasive Communications and Computing (CPCC) Fellowship Award
2003	2nd place, Best Poster Award, Southern California Embedded Sytems Symposium (SCESS) for the poster: *S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt, N. Subramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices"*

2003 DAC Young Student Award, Design Automation Conference (DAC)

2002-03 Regents Fellowship, Department of Information and Computer Science, UC Irvine

1996-97 Best Student in Electronics and Communications, Delhi Institute of Technology, India

1994-96 National Math Olympiad, Outstanding Performance Merit Award, Gov't of India

1994 Ramanujan Society of Born Mathematicians Award, All India 7th Rank

Professional Society Memberships

2017 Activities Committee Member, IEEE CEDA

2014-Present Elected Senior Member, IEEE

2014-Present Elected Senior Member, ACM

2011-Present Advisory Board Member, ACM SIGDA

2002-2014 Member, IEEE

2008-2014 Member, ACM

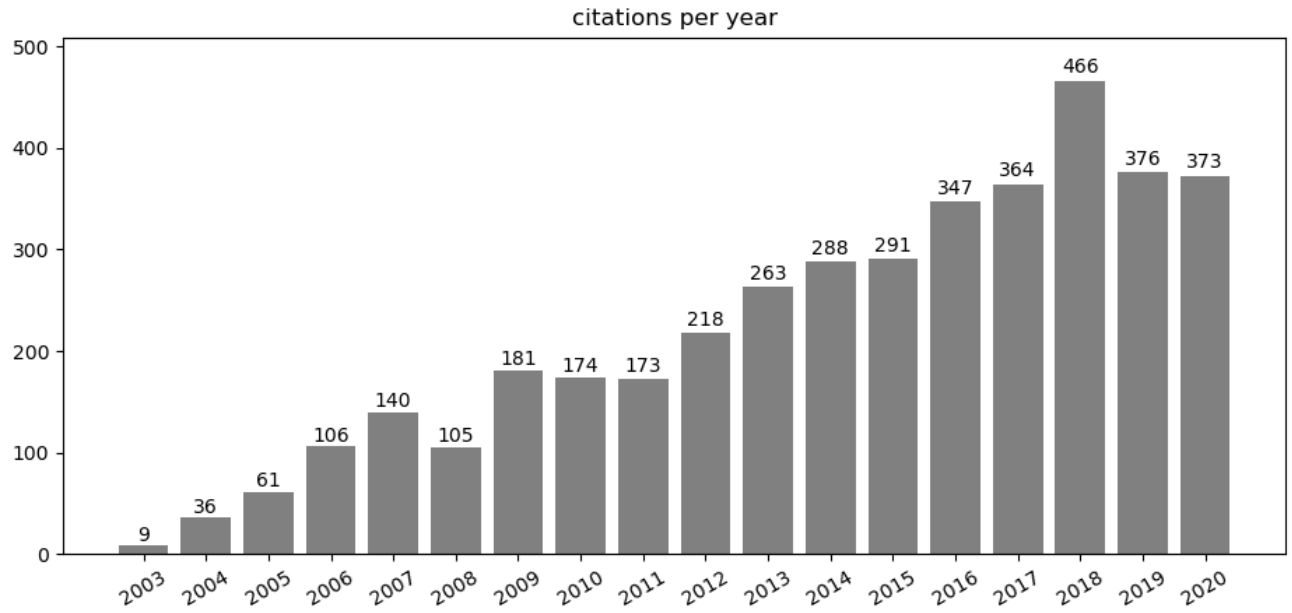
Research Activities

Research Interest Statement

My research broadly focuses on software algorithms, hardware architectures, and hardware-software co-design for energy-efficient, fault-tolerant, real-time, and secure computing. These efforts target multi-scale computing platforms, including embedded and Internet of Things (IoT) systems, cyber-physical systems, mobile devices, and datacenters.

Publication Citations
(Google Scholar as of 15 November, 2020)

	All	Since 2015
Citations	4019	2219
h-index	32	23
i10-index	109	81



Research Books Authored

B2 – M. Nikdast, S. Pasricha, G. Nicolescu, A. Sysedi, D. Liang, *Silicon Photonics for High Performance Computing and Beyond*, CRC Publishers, 2021.

B1 – S. Pasricha, N. Dutt, *On-Chip Communication Architectures*, Morgan Kauffman, ISBN 978-0-12-373892-9, 544 pages, Apr. 2008.

Research Book Chapters

BC9 – I. G. Thakkar, S. V. R. Chittamuru, V. Bhat, S. S. Vatsavai, S. Pasricha, "Securing Silicon Photonic NoCs Against Hardware Attacks", *Springer Book on Network-on-Chip Security and Privacy, 2021.*

BC8 – V. Y. Raparti, S. Pasricha, "Securing 3D NoCs from Hardware Trojan Attacks", *Springer Book on Network-on-Chip Security and Privacy, 2021.*

BC7 – I. Thakkar, S. V. R. Chittamuru, V. Bhat, S. S. Vatsavai, S. Pasricha, "Hardware Security in Emerging Photonic Network-on-Chip Architectures," *Springer Book on Emerging Computing, June 2020.*

BC6 – I. Thakkar, S. Pasricha, V. S. P. Karempudi, S. V. R. Chittamuru, "Exploring Aging Effects in Photonic Interconnects for High-Performance Manycore Architectures," *Silicon Photonics for High Performance Computing and Beyond, to appear, CRC Press/Taylor & Francis Group, December 2019.*

BC5 – S. Pasricha, "Network and Communication Signals for Indoor Navigation", to appear, *21st Century PNT, Wiley Publishers, 2019.*

BC4 – S. Pasricha, S. V. R. Chittamuru, I. Thakkar, "Enhancing Process Variation Resilience in Photonic NoC Architectures", *Optical Interconnects for Computer Systems, River Publishers, 2017*.

BC3 – N. Kapadia, S. Pasricha, "Robust Application Scheduling with Adaptive Parallelism in Dark-Silicon Constrained Multicore Systems", *The Dark Side of Silicon (Computing in the Dark Silicon Era), Springer, 2017*.

BC2 – S. Pasricha, Y. Zou, "Hybrid Partially Adaptive Fault Tolerant Routing for 3D Networks-on-Chip", *Embedded Systems: Hardware, Design, and Implementation, (ed K. Iniewski), John Wiley & Sons, Inc., Hoboken, NJ, USA. doi: 10.1002/9781118468654.ch10,* Nov 2012.

BC1 – S. Pasricha, N. Dutt, "On-chip Optical Ring Bus Communication Architecture for Heterogeneous MPSoC", *Integrated Optical Interconnect Architectures for Embedded Systems, I. O'Connor and G. Nicolescu (eds.), DOI 10.1007/978-1-4419-6193-8_5,* Nov 2012.

Peer-Reviewed Journal Publications

J66 – S. V. R. Chittamuru, I. Thakkar, S. Pasricha, S. S. Vatsavai, V. Bhat "Exploiting Process Variations to Secure Photonic NoC Architectures from Snooping Attacks", *to appear, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD), 2020.*

J65 – V. K. Kukkala, S. V. Thiruloga, and S. Pasricha, "INDRA: Intrusion Detection using Recurrent Autoencoders in Automotive Embedded Systems", *to appear, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD), 2020.*

J64 – J. Dey, W. Taylor, S. Pasricha, "VESPA: Optimizing Heterogeneous Sensor Placement and Orientation for Autonomous Vehicles", *to appear, IEEE Consumer Electronics, 2020.*

J63 – S. Pasricha, Raid Ayoub, M. Kishinevsky, S. K. Mandal, U. Y. Ogras, "A Survey on Energy Management for Mobile and IoT Devices", *IEEE Design and Test, vol. 37, no. 5, pp. 7-24, Oct 2020.*

J62 – K. Khan, S. Pasricha, R. G. Kim, "A Survey of Resource Management for Processing-in-Memory and Near-Memory Processing Architectures", *Journal of Low Power Electronics and Applications, Special Issue on Design Space Exploration and Resource Management of Multi/Many-Core Systems, Sep 2020.*

J61 – S. Tiku, S. Pasricha, "A Hidden Markov Model based Smartphone Heterogeneity Resilient Portable Indoor Localization Framework", *Journal of Systems Architecture, Sep 2020.*

J60 – S. Pasricha, M. Nikdast, "A Survey of Silicon Photonics for Energy Efficient Manycore Computing", *IEEE Design and Test, vol. 37, no. 4, pp. 60-81, 2020.*

J59 – V. Kukkala, S. Pasricha, T. H. Bradley, "SEDAN: Security-Aware Design of Time-Critical Automotive Networks", *IEEE Transactions on Vehicular Technology, vol. 69, no. 8, Aug 2020.*

J58 – V. Y. Raparti, S. Pasricha, "Approximate NoC and Memory Controller Architectures for GPGPU Accelerators", *IEEE Transactions on Parallel and Distributed Systems (TPDS), Vol. 31, Iss 5., May 2020.*

J57 – S. Tiku, S. Pasricha, "Overcoming Security Vulnerabilities in Deep Learning Based Indoor Localization on Mobile Devices", *ACM Transactions on Embedded Computing Systems (TECS), Vol. 18, Iss. 6, Jan 2020.*

J56 – V. Kukkala, S. Pasricha, T. H. Bradley, "JAMS-SG: A Framework for Jitter-Aware Message Scheduling for Time-Triggered Automotive Networks", *ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 24, Iss. 6, Nov 2019.*

J55 – S. Tiku, S. Pasricha, "PortLoc: A Portable Data-driven Indoor Localization Framework for Smartphones", *IEEE Design and Test, Vol. 36, Iss. 5, Oct 2019.*

J54 – A. Khune, S. Pasricha, "Mobile Network-Aware Middleware Framework for Energy Efficient Cloud Offloading of Smartphone Applications", *IEEE Consumer Electronics, Vol. 8, Iss. 1, Jan 2019.*

J53 – V. Y. Raparti, S. Pasricha, "RAPID: Memory-Aware NoC for Latency Optimized GPGPU Architectures", *IEEE Transactions on Multi-Scale Computing Systems (IEEE TMSCS), Vol. 4, No. 4, Oct-Dec 2018.*

J52 – S. V. R. Chittamuru, I. Thakkar, S. Pasricha, "LIBRA: Thermal and Process Variation Aware Reliability Management in Photonic Networks-on-Chip", *IEEE Transactions on Multi-Scale Computing Systems (TMSCS), Vol. 4, No. 4, Oct-Dec 2018.*

J51 – S. V. R. Chittamuru, D. Dharnidhar, S. Pasricha, R. Mahapatra "BiGNoC: Accelerating Big Data Computing with Application-Specific Photonic Network-on-Chip Architectures", *IEEE Transactions on Parallel and Distributed Systems (TPDS), Vol. 29, Iss. 11, Nov 2018.*

J50 – J. Tunnell, Z. Asher, S. Pasricha, T. H. Bradley, "Towards Improving Vehicle Fuel Economy with ADAS", *SAE International Journal of Connected and Automated Vehicles, Oct 2018.*

J49 – N. Hogade, S. Pasricha, A. A. Maciejewski, H.J. Siegel, M. Oxley, E. Jonardi, "Minimizing Energy Costs for Geographically Distributed Heterogeneous Data Centers", *IEEE Transactions on Sustainable Computing (TSUSC), Vol. 3, No. 4, Oct-Dec 2018.*

J48 – D. Dauwe, S. Pasricha, A. A. Maciejewski, H.J. Siegel, "Resilience-Aware Resource Management for Exascale Computing Systems", *IEEE Transactions on Sustainable Computing (TSUSC), Vol. 3, No. 4, Oct-Dec 2018.*

J47 –V. Kukkala, J. Tunnell, S. Pasricha, "Advanced Driver Assistance Systems: A Path Toward Autonomous Vehicles", *IEEE Consumer Electronics, Vol. 7, Iss. 5, Sept 2018.*

J46 – I. Thakkar, S. Pasricha, "DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency and Restorable Endurance", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD), Volume: 37, Issue: 9 , Sept. 2018.*

J45 – Y. Xiang, S. Pasricha, "Mixed-Criticality Scheduling on Heterogeneous Multicore Systems Powered by Energy Harvesting", *Integration, the VLSI Journal, vol. 61, pp. 114-124, Mar 2018.*

J44 – M. Oxley, E. Jonardi, S. Pasricha, H. J. Siegel, T. Maciejewski, P. J. Burns, and G. Koenig "Rate-based Thermal, Power, and Co-location Aware Resource Management for Heterogeneous Data Centers", *Journal of Parallel and Distributed Computing (JPDC), vol. 12, part 2, pp. 126-139, Feb 2018.*

J43 – S. V. R. Chittamuru, I. Thakkar, S. Pasricha, "HYDRA: Heterodyne Crosstalk Mitigation with Double Microring Resonators and Data Encoding for Photonic NoC", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol. 26, iss. 1, pp. 168 – 181, Jan 2018.*

J42 – Y. Biran, S. Pasricha, G. Collins, J. Dubow, "Clean Energy Use for Cloud Computing Federation Workloads", *Advances in Science, Technology and Engineering Systems Journal, vol. 2, Issue 6, pp. 1-12, 2017.*

J41 – H. Mahajan, T. Bradley, S. Pasricha, "Application of systems theoretic process analysis to a lane keeping assist system", *Journal of Reliability Engineering and System Safety, vol. 167, pp. 177-183, Nov. 2017.*

J40 – D. Machovec, B. Khemka, N. Kumbhare, S. Pasricha, A. A. Maciejewski, H. J. Siegel, A. Akoglu, G. A. Koenig, S. Hariri, C. Tunc, M. Wright, M. Hilton, R. Rambharos, C. Blandin, F. Fargo, A. Louri, N. Imam, "Utility-Based Resource Management in an Oversubscribed Energy-Constrained Heterogeneous Environment Executing Parallel Applications", *Journal of Parallel Computing (PARCO), Nov. 2017.*

J39 – C. Langlois, S. Tiku, S. Pasricha, "Indoor localization with smartphones", *IEEE Consumer Electronics, 6(4), Oct 2017.*

J38 – Y. Raparti, N. Kapadia, S. Pasricha, "ARTEMIS: An Aging-Aware Runtime Application Mapping Framework for 3D NoC-based Chip Multiprocessors", *IEEE Transactions on Multi-Scale Computing Systems (IEEE TMSCS), Vol. 3, No. 2, pp. 72-85, Apr-Jun 2017.* ***(Selected as Featured Paper for Apr-Jun issue)***

J37 – S. V. R. Chittamuru, S. Desai, S. Pasricha, "SWIFTNoC: A Reconfigurable Silicon-Photonic Network with Multicast Enabled Channel Sharing for Multicore Architectures", *ACM Journal on Emerging Technologies in Computing Systems (JETC), Vol. 13, No. 4, pp. 58:1-58:27, Jun 2017.*

J36 – N. Kapadia, S. Pasricha, "A Runtime Framework for Robust Application Scheduling with Adaptive Parallelism in the Dark-Silicon Era", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 25, No. 2, pp. 534-546, Feb. 2017.*

J35 – J. Dubow, Y. Biran, S. Pasricha, G. Collins, J. M. Borky, "Considerations for Planning a Multi-platform Energy Utility System", *Journal of Energy and Power Engineering, 09(12):723-749, Jan 2017.*

J34 – D. Dauwe, E. Jonardi, R. Friese, S. Pasricha, A. A. Maciejewski, D. Bader, H.J. Siegel, "HPC Node Performance and Energy Modeling Under the Uncertainty of Application Co-Location", *Journal of Supercomputing, Vol. 72, No. 12, pp. 4771-4809, Nov. 2016.*

J33 – S. Bahirat, S. Pasricha, "A Software Framework for Rapid Application-Specific Hybrid Photonic Network-on-Chip Synthesis", *Electronics, 5(2), 21, Special Issue on Rapid System Design with Dedicated Architectures and Specific Software Tools, 2016.*

J32 – N. Kapadia, S. Pasricha, "A System-Level Co-Synthesis Framework for Power Delivery and On-chip Data Networks in Application-Specific 3D ICs", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol.24, no.1, pp.3-16, Jan. 2016.*

J31 – Y. Xiang, S. Pasricha, "Soft and Hard Reliability-Aware Scheduling for Multicore Embedded Systems with Energy Harvesting", *IEEE Transactions on Multi-Scale Computing Systems (IEEE TMSCS), Oct-Dec, vol. 1, no. 4, pp. 220-235, 2015.*

J30 – Y. Xiang, S. Pasricha, "Run-Time Management for Multi-Core Embedded Systems with Energy Harvesting", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol.23, no.12, pp.2876-2889, Dec. 2015.*

J29 – M. Oxley, S. Pasricha, A. A. Maciejewski, H. J. Siegel, J. Apodaca, D. Young, L. Briceno, J. Smith, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou,, "Makespan and Energy Robust Stochastic Static Resource Allocation of Bags-of-Tasks to a Heterogeneous Computing System", *IEEE Transactions on Parallel and Distributed Systems, vol.26, no.10, pp. 2791-2805, Oct. 2015.*

J28 – I. Thakkar, S. Pasricha, "3D-ProWiz: An Energy-Efficient and Optically-Interfaced 3D DRAM Architecture with Reduced Data Access Overhead", *IEEE Transactions on Multi-Scale Computing Systems (TMSCS), vol.1, no.3, pp.168-184, Sep. 2015.*

J27 – I. Thakkar, S. Pasricha, "3D-WiRED: A Novel Wide I/O DRAM with Energy-Efficient 3D Bank Organization", *IEEE Design and Test (IEEE D&T), vol.32, no.4, pp.71-80, Aug. 2015.*

J26 – B. Donohoo, C. Ohlsen, S. Pasricha, "A Middleware Framework for Application-aware and User-specific Energy Optimization in Smart Mobile Devices", *Journal of Pervasive and Mobile Computing, vol. 20, pp. 47-63, Jul 2015.*

J25 – S. V. R. Chittamuru, S. Pasricha, "Crosstalk Mitigation for High-Radix and Low-Diameter Photonic NoC Architectures", *IEEE Design and Test (IEEE D&T), vol.32, no.3, pp.29-39, June 2015.*

J24 – B. Khemka, R. Friese, S. Pasricha, A. A. Maciejewski, H. J. Siegel, G. A. Koenig, S. Powers, M. Hilton, R. Rambharos, and S. Poole, "Utility Maximizing Dynamic Resource Management in an Oversubscribed Energy-Constrained Heterogeneous Computing System", *Journal of Sustainable Computing: Informatics and Systems, 2014, Volume 5, pp. 14–30, March 2015.*

J23 – A. M. Al-Qawasmeh, S. Pasricha, A. M. Maciejewski, H. J. Siegel, "Power and Thermal-Aware Workload Allocation in Heterogeneous Data Centers", *IEEE Transactions on Computers, vol. 64, Iss 02, pp. 477-491, Feb 2015.*

J22 – Y. Xu, S. Pasricha, "Silicon Nanophotonics for Future Multicore Architectures: Opportunities and Challenges", *IEEE Design and Test (IEEE D&T), Special Issue on Silicon Nanophotonics for Future Multicore Architectures, Sep/Oct, pp. 9-17, 2014.*

J21 – B. Donohoo, C. Ohlsen, S. Pasricha, C. Anderson, Y. Xiang, "Context-Aware Energy Enhancements for Smart Mobile Devices", *IEEE Transactions on Mobile Computing, Vol 13, No. 8, pp. 1720-1732, Aug 2014.*

J20 – S. Bahirat, S. Pasricha, "METEOR: Hybrid Photonic Ring-Mesh Network-on-Chip for Multicore Architectures", *IEEE Transactions on Embedded Computing Systems (TECS), 13(3):116:1-116:33, Mar 2014.*

J19 – L. Bathen, Y. Ahn, S. Pasricha, N. Dutt, "MultiMaKe: Chip-Multiprocessor Driven Memory-aware Kernel Pipelining", *IEEE Transactions on Embedded Computing Systems (TECS), 12(1), Mar 2013.*

J18 – D. Young, J. Apodaca, L. Briceno, J. Smith, S. Pasricha, A. Maciejewski, H. Siegel, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou, "Deadline and Energy Constrained Dynamic Resource Allocation in a Heterogeneous Computing Environment", *Journal of Supercomputing, vol. 63, Iss. 2, pp. 326-347, 2013.*

J17 – Y. Zou, Y. Xiang, S. Pasricha, "Characterizing Vulnerability of Network Interfaces in Embedded Chip Multiprocessors", *IEEE Embedded System Letters, 4(2)*, Jun 2012.

J16 – N. Kapadia, S. Pasricha, "A Framework for Low Power Synthesis of Interconnection Networks-on-Chip with Multiple Voltage Islands", *Integration, the VLSI Journal, 45(3):271-281,* Jun 2012.

J15 – Y. Park, S. Pasricha, F. Kurdahi, N. Dutt, "A Multi-Granularity Power Modeling Methodology for Embedded Processors", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 19, No. 4, pp. 668-681, Apr 2011.*

J14 – Y. Zou, S. Pasricha, "NARCO: Neighbor Aware Turn Model Based Fault Tolerant Routing for NoCs", *IEEE Embedded System Letters,* Vol. 2, No. 3, pp. 85-89, Sep. 2010.

J13 – S. Pasricha, F. Kurdahi, N. Dutt, "Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* Vol. 18, No. 9, pp. 1376-1380, Sep. 2010.

J12 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "CAPPS: A Framework for Power-Performance Trade-Offs in Bus Matrix Based On-Chip Communication Architecture Synthesis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* Vol. 18, No. 2, pp. 209-221, Feb. 2010.

J11 – G. Madl, S. Pasricha, N. Dutt, S. Abdelwahed, "Cross-abstraction Functional Verification and Performance Analysis of Chip Multiprocessor Designs" *IEEE Transactions on Industrial Informatics (TII),* Vol. 5, No. 3, pp. 241-256, Aug. 2009.

J10 – D. Cho, S. Pasricha, I. Issenin, N. Dutt, Y. Paek , "Adaptive Scratch Pad Memory Management for Dynamic Behavior of Multimedia Applications", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 28, No. 4, pp. 554-567, Apr. 2009.

J9 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "System-level PVT Variation Aware Power Exploration of On-Chip Communication Architectures", *ACM Transactions on Design Automation of Electronic*

Systems (TODAES), Vol. 14, No. 2, pp. 20:1-20:25, Mar. 2009.

J8 – S. Pasricha, N. Dutt, "Trends in Emerging On-Chip Interconnect Technologies", *Information Processing Society of Japan (IPSJ) Transactions on System LSI Design Methodology*, Vol. 3, No. 4, pp. 630-645, Sep. 2008.

J7 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Fast Exploration of Bus-based Communication Architectures at the CCATB Abstraction", *ACM Transactions on Embedded Computing Systems (TECS)*, Vol. 7, No. 2, pp. 22-32, Feb. 2007.

J6 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "BMSYN: Bus Matrix Communication Architecture Synthesis for MPSoC", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD)*, Vol. 26, No.8, pp.1454-1464, Aug. 2007.

J5 – S. Pasricha, N. Dutt, "A Framework for Co-synthesis of Memory and Communication Architectures for MPSoC", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 26, No. 3, pp. 408-420, Mar. 2007.

J4 – C. Shin, P. Grun, N. Romdhane, C. Lennard, G. Madl, S. Pasricha, N. Dutt, M. Noll, "Enabling Heterogeneous Cycle-Based and Event-Driven Simulation in a SPIRIT-Enabled Design Flow", *Kluwer Journal on Design Automation of Embedded Systems (DAES)*, Vol. 11, No. 2-3, pp. 119-140, Feb. 2007.

J3 – S. Pasricha, N. Dutt, E. Bozorgzadeh and M. Ben-Romdhane, "FABSYN: Floorplan-aware Bus Architecture Synthesis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)* Vol. 14, No. 3, pp. 241-253, Mar. 2006.

J2 – S. Pasricha, M. Luthra, S. Mohapatra, N. Dutt, N. Subramanian, "Dynamic Backlight Adaptation for Low Power Handheld Devices", *IEEE Design and Test (IEEE D&T), Special Issue on Embedded Systems for Real Time Embedded Systems*, Vol. 21, No. 5, pp. 398-405, Sep-Oct 2004.

J1 – S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt, N. Subramanian, "Co-optimization of Streaming Multimedia QoS and Backlight Power Consumption for Mobile Handheld Devices", *Journal of Korean Multimedia Society (KSSM)*, Dec. 2003 (invited).

Peer-Reviewed Conference Publications (approx. 20-30% acceptance rate)

C137 – D. Machovec, J. A. Crowder, H. J. Siegel, S. Pasricha, and A. A. Maciejewski, "Dynamic Heuristics for Surveillance Mission Scheduling with Unmanned Aerial Vehicles in Heterogeneous Environments", *22nd International Conference on Artificial Intelligence (ICAI'20), July 2020.*

C136 –A. Mirza, S. Pasricha, and M. Nikdast, "Variation-Aware Inter-Device Matching in Silicon Photonic Microring Resonator Demultiplexers", *IEEE Photonics Conference (IPC), 2020.*

C135 – F. Sunny, A. Mirza, I. Thakkar, S. Pasricha, and M. Nikdast, "LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip", *ACM Great Lakes Symposium on VLSI (GLSVLSI), 2020.* **(Best Paper Award Honorable Mention)**

C134 – A. Mirza, S. Avari, E. Taheri, S. Pasricha, and M. Nikdast, "Opportunities for Cross-Layer Design in High-Performance Computing Systems with Integrated Silicon Photonic Networks", *IEEE/ACM Design, Automation and Test in Europe (DATE) Conference and Exhibition, March 2020.*

C133 – A. Mirza, F. Sunny, S. Pasricha, and M. Nikdast, "Silicon Photonic Microring Resonators: Design Optimization under Fabrication Non-Uniformity", *IEEE/ACM Design, Automation and Test in Europe (DATE) Conference and Exhibition, March 2020.*

C132 –S. Pasricha, N. Hogade, H.J. Seigel, A. A. Maciejewski, "Green Computing with Geo-Distributed Heterogeneous Data Centers," *IEEE International Green and Sustainable Computing Conference (IGSC), Alexandria, VA, USA, Oct. 2019.*

C131 – M. Adkins, Q. Han, S. Pasricha, "Quality-Aware Voice Convergecast in Mobile Low Power Wireless Networks", *IEEE International Conference on Mobile Computing, Applications and Services (MobiCASE), Hangzhou, China, June 14-15, 2019.*

C130 – S. Tiku, S. Pasricha, B. Notaros, Q. Han, "SHERPA: A Lightweight Smartphone Heterogeneity Resilient Portable Indoor Localization Framework," *IEEE International Conference on Embedded Software and Systems (ICESS), Las Vegas, NV, USA, Jun. 2019.*

C129 – S. Bhosale, S. Pasricha, "SLAM: High Performance and Energy Efficient Hybrid Last Level Cache Architecture for Multicore Embedded Systems," *IEEE International Conference on Embedded Software and Systems (ICESS), Las Vegas, NV, USA, Jun. 2019.*

C128 – Y. Raparti, S. Pasricha, "Lightweight Mitigation of Hardware Trojan Attacks in NoC-based Manycore Computing," *IEEE/ACM Design Automation Conference (DAC), Las Vegas, NV,, USA, Jun. 2019.*

C127 – I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "Mitigating the Energy Impacts of VBTI Aging in Photonic Networks-on-Chip Architectures with Multilevel Signaling," *IEEE Workshop on Energy-efficient Networks of Computers (E2NC): from the Chip to the Cloud, Oct 2018.*

C126 – Y. Raparti, S. Pasricha, "DAPPER: Data Aware Approximate NoC for GPGPU Architectures," *to appear, IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Torino, Italy, Oct 2018.* **(Best Paper Award)**

C125 – S. Pasricha, S. V. R. Chittamuru, I. Thakkar, V. Bhat, "Securing Photonic NoC Architectures from Hardware Trojans," *IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Torino, Italy, Oct 2018.*

C124 – Y. Raparti, S. Pasricha, "PARM: Power Supply Noise Aware Resource Management for NoC based Multicore Systems in the Dark Silicon Era," *IEEE/ACM Design Automation Conference (DAC), San Francisco, CA, USA, Jun. 2018.*

C123 – S. V. R. Chittamuru, I. Thakkar, V. Bhat, S. Pasricha, "SOTERIA: Exploiting Process Variations to Enhance Hardware Security with Photonic NoC Architectures," *IEEE/ACM Design Automation*

Conference (DAC), San Francisco, CA, USA, Jun. 2018.

C122 – D. Dauwe, S. Pasricha, A. A. Maciejewski, H. J. Siegel, "An Analysis of Multilevel Checkpoint Performance Models," *20th Workshop on Advances in Parallel and Distributed Computational Models (APDCM), co-organized with IEEE International Parallel and Distributed Processing Symposium (IPDPS), Vancouver, BC, Canada, May 2018.*

C121 – A. Mittal, S. Tiku, S. Pasricha, "Adapting Convolutional Neural Networks for Indoor Localization with Smart Mobile Devices," *ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2018.* **(Best Paper Award)**

C120 – S. Pasricha, S. V. R. Chittamuru, I. Thakkar, "Cross-Layer Thermal Reliability Management in Photonic Networks-on-Chip," *ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2018.*

C119 – J. Tunnell, Z. Asher, S. Pasricha, T. H. Bradley, "Towards Improving Vehicle Fuel Economy with ADAS", *SAE International, 2018.*

C118 – S. Pasricha, D. Bertozzi, H. Li, "Overcoming Reliability and Energy-Efficiency Challenges with Silicon Photonics for Future Manycore Computing," *IEEE VLSI Test Symposium, Apr 2018. (Extended Abstract)*

C117 – Z. Asher, J. Tunnell, D. A. Baker, R. J. Fitzgerald, F. Banaei-Kashani, S. Pasricha, T. H. Bradley, "Enabling Prediction for Optimal Fuel Economy Vehicle Control," *SAE International, 2018.*

C116 – D. Dauwe, S. Pasricha, A. A. Maciejewski, H. J. Siegel, "An Exploration of Fault Resilience Protocols for Large-Scale Application Execution on Exascale Computing Platforms," *5th Exascale Applications and Software Conference (EASC), Edinburgh, Scotland, 2018. (Extended Abstract)*

C115 – S. Pasricha, "Overcoming Energy and Reliability Challenges for IoT and Mobile Devices with Data Analytics," *IEEE International Conference on VLSI Design (VLSID), Pune, India, Jan 2018.*

C114 – K. Yao, Y. Ye, S. Pasricha, J. Xu, "Thermal-Sensitive Design and Power Optimization for a 3D Torus-Based Optical NoC," *IEEE/ACM International Conference on Computer Aided Design (ICCAD), Irvine, CA, USA, Nov 2017.*

C113 –D. Dauwe, R. Jhaveri, S. Pasricha, A. A. Maciejewski, H. J. Siegel, "Optimizing Checkpoint Intervals for Reduced Energy Use in Exascale Systems," *IEEE Workshop on Energy-efficient Networks of Computers (E2NC): from the Chip to the Cloud, Orlando, FL, USA, Oct 2017.*

C112 – V. K. Kukkala, S. Pasricha, T. Bradley, "JAMS: Jitter-Aware Message Scheduling for FlexRay Automotive Networks," *IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Seoul, Korea, Oct 2017.*

C111 – S. Tiku, S. Pasricha, "Energy-Efficient and Robust Middleware Prototyping for Smart Mobile Computing," *IEEE International Symposium on Rapid System Prototyping (RSP), Seoul, Korea, Oct 2017.*

C110 – I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "Improving the Reliability and Energy-Efficiency of High-Bandwidth Photonic NoC Architectures with Multilevel Signaling," *IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Seoul, Korea, Oct 2017.*

C109 – S. Pasricha, J. Doppa, K. Chakrabarty, S. Tiku, D. Dauwe, S. Jin, P. Pande, "Data Analytics Enables Energy-Efficiency and Robustness: From Mobile to Manycores, Datacenters, and Networks", ACM/*IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Seoul, Korea, Oct 2017.*

C108 –S. V. R. Chittamuru, I. Thakkar, S. Pasricha, "Analyzing Voltage Bias and Temperature Induced Aging Effects in Photonic Interconnects for Manycore Computing," *ACM System Level Interconnect Prediction Workshop (SLIP), Austin, TX, USA, Jun 2017.*

C107 – H. Mahajan, T. Bradley, S. Pasricha, "Application of STPA to a lane keeping assist system", *Workshop on Systems Approach to Safety and Security (STPA/STAMP), Cambridge, MA, USA, 2017.*

C106 – V. K. Kukkala, T. Bradley, S. Pasricha, "Uncertainty Analysis and Propagation for an Auxiliary Power Module," *IEEE Transportation and Electrification Conference (TEC), Chicago, IL, USA, 2017.*

C105 – D. Dauwe, S. Pasricha, A. A. Maciejewski, H. J. Siegel, "An Analysis of Resilience Techniques for Exascale Computing Platforms," *19th Workshop on Advances in Parallel and Distributed Computational Models (APDCM), co-organized with IEEE International Parallel and Distributed Processing Symposium (IPDPS), Orlando, FL, USA, May 2017.*

C104 – D. Machovec, S. Pasricha, A. A. Maciejewski, H. Jay Siegel, G. A. Koenig, M. Wright, M. Hilton, R. Rambharos, T. Naughton, N. Imam, "Preemptive Resource Management for Dynamically Arriving Tasks in an Oversubscribed Heterogeneous Computing System," *International Heterogeneity in Computing Workshop (HCW), co-organized with IEEE International Parallel and Distributed Processing Symposium (IPDPS), Orlando, FL, USA, May 2017.*

C103 – S. Maiti, S. Pasricha, "DELCA: DVFS Efficient Low Cost Multicore Architecture," *ACM Great Lakes Symposium on VLSI (GLSVLSI), Banff, Canada, May 2017.*

C102 – D. Dang, S. V. R. Chittamuru, R. N. Mahapatra, S. Pasricha, "Islands of Heaters: A Novel Thermal Management Framework for Photonic NoCs," *IEEE/ACM Asia & South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 2017.*

C101 – I. Thakkar, S. Pasricha, "DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency," *IEEE International Conference on VLSI Design (VLSI), Hyderabad, India, Jan 2017.*

C100 – Y. Biran, S. Pasricha, G. Collins, J. Dubow, "Enabling Green Content Distribution Network by Cloud Orchestration," *3rd Smart Cloud Networks & Systems Conference, Dubai, UAE, Dec 2016.* **(<u>Best Paper Award Candidate</u>)**

C99 – D. Dauwe, S. Pasricha, A. A. Maciejewski, H. J. Siegel, "A Performance and Energy Comparison of Fault Tolerence Techniques for Exascale Computing Systems," *6th IEEE International Symposium on Cloud and Service Computing (SC-2), Nadi, Fiji, Dec 2016.*

C98 – V. Y. Raparti, S. Pasricha, "CHARM: A Checkpoint-based Resource Management Framework for Reliable Multicore Computing in the Dark Silicon Era," *IEEE International Conference on Computer Design (ICCD), Phoenix, AZ, USA, Oct 2016.*

C97 – I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "Mitigation of Homodyne Crosstalk Noise in Silicon Photonic NoC Architectures with Tunable Decoupling," ACM/*IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Pittsburgh, PA, USA, Oct 2016.* (26% paper acceptance rate)

C96 – V. Y. Raparti, S. Pasricha, "A Cross-Layer Runtime Framework for Checkpoint-based Soft-Error and Aging Management in SoCs," *SRC Techcon, Austin, TX, USA, Sep 2016.*

C95 – M. Oxley, S. Pasricha, T. Maciejewski, H.J. Siegel and P. Burns, "Online Resource Management in Thermal and Energy Constrained Heterogeneous High Performance Computing," *IEEE International Conference on Big Data Intelligence and Computing (DataCom), Auckland, New Zealand, Aug 2016.*

C94 – I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "Run-Time Laser Power Management in Photonic NoCs with On-Chip Semiconductor Optical Amplifiers," *IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Nara, Japan, Aug 2016.*

C93 – I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects," *ACM System Level Interconnect Prediction Workshop (SLIP), Austin, TX, USA, Jun 2016.* **(Best Paper Award)**

C92 – S. V. R. Chittamuru, I. Thakkar, S. Pasricha, "PICO: Mitigating Heterodyne Crosstalk Due to Process Variations and Intermodulation Effects in Photonic NoCs," *IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, Jun. 2016.*

C91 – D. Machovec, B. Khemka, S. Pasricha, A. A. Maciejewski, H. Jay Siegel, G. A. Koenig, M. Wright, M. Hilton, R. Rambharos, N. Imam, "Dynamic Resource Management for Parallel Tasks in an Oversubscribed Energy-Constrained Heterogeneous Environment," *International Heterogeneity in Computing Workshop (HCW), Orlando, FL, USA, May 2016.*

C90 – V. Y. Raparti, S. Pasricha, "Memory-Aware Circuit Overlay NoCs for Latency Optimized GPGPU Architectures," *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, Mar. 2016.*

C89 – S. V. R. Chittamuru, I. Thakkar, S. Pasricha, "Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures," *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, Mar. 2016.* **(Best Paper Award Candidate)**

C88 – P. Pande, S. Pasricha, H, Matsutani, "The Future of NoCs: New Technologies and Architectures,"

IEEE International Conference on VLSI Design (VLSI), Kolkata, India, Jan 2016.

C87 – I. Thakkar, S. Pasricha, "Massed Refresh: An Energy-Efficient Technique to Reduce Refresh Overhead in Hybrid Memory Cube Architectures," *IEEE International Conference on VLSI Design (VLSI), Kolkata, India, Jan 2016.*

C86 – S. V. R. Chittamuru, S. Pasricha, "SPECTRA: A Framework for Thermal Reliability Management in Silicon-Photonic Networks-on-Chip," *IEEE International Conference on VLSI Design (VLSI), Kolkata, India, Jan 2016.*

C85 – S. Pasricha, "Integrated Photonics in Future Multicore Computing: New Directions in Dependability and Power Efficiency," *IEEE Second Workshop on Low-Power Dependable Computing (LPDC), Las Vegas, NV, USA, Dec 2015.* **(Invited Keynote Paper)**

C84 – E. Jonardi, M. Oxley, S. Pasricha, H. J. Siegel and T. Maciejewski, "Energy Cost Optimization for Geographically Distributed Heterogeneous Data Centers," *IEEE Workshop on Energy-efficient Networks of Computers (E2NC): from the Chip to the Cloud, Las Vegas, NV, USA, Dec 2015.*

C83 – I. Thakkar, S. Pasricha, "A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses," *IEEE International Conference on Computer Design (ICCD), New York, NY, USA, Oct 2015.*

C82 – S. Pasricha, V. Ugave, Q. Han and C. Anderson, "LearnLoc: A Framework for Smart Indoor Localization with Embedded Mobile Devices," ACM/*IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Amsterdam, Netherlands, Oct 2015.*

C81 – N. Kapadia, V. Y. Raparti, S. Pasricha, "ARTEMIS: An Aging-Aware Run-Time Application Mapping Framework for 3D NoC based Chip Multiprocessors," *IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Vancouver, Canada, 2015.*

C80 – V. K. Kukkala, T. Bradley, S. Pasricha, "Priority-based Multi-level Monitoring of Signal Integrity in a Distributed Powertrain Control System," *4th IFAC Workshop on Engine and Powertrain Control, Simulation and Modeling, Columbus, OH, USA, Jul 2015.* (**Invited Paper**)

C79 – B. Khemka, R. Friese, S. Pasricha, A. A. Maciejewski, H. J. Siegel, G. A. Koenig, S. Powers, M. Hilton, R. Rambharos, M. Wright, S. Poole, "Comparison of Energy-Constrained Resource Allocation Heuristics Under Different Task Management Environments," *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA), Las Vegas, NV, USA, 2015.*

C78 – S. Maiti, N. Kapadia, S. Pasricha, "Process Variation Aware Dynamic Power Management in Multicore Systems with Extended Range Voltage/Frequency Scaling," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Fort Collins, CO, USA, 2015.*

C77 – S. V. R. Chittamuru, S. Pasricha, "Improving Crosstalk Resilience with Wavelength Spacing in Photonic Crossbar-based Network-on-Chip Architectures," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Fort Collins, CO, USA, 2015.*

C76 – N. Kapadia, S. Pasricha, "Process-Variation and Soft-Error Reliability-Aware Workload Mapping with Adaptive Parallelism in SoCs," *SRC Techcon, Austin, TX, USA, 2015.*

C75 – D. Dauwe, E. Jonardi, R. Friese, S. Pasricha, A. A. Maciejewski, D. Bader, H.J. Siegel, "A Methodology for Co-Location Aware Application Performance Modeling in Multicore Computing," *17th Workshop on Advances on Parallel and Distributed Processing Symposium (APDCM), Hyderabad, India, 2015.*

C74 – S. V. R. Chittamuru, S. Desai, S. Pasricha, "A Reconfigurable Silicon-Photonic Network with Improved Channel Sharing for Multicore Architectures," *ACM Great Lakes Symposium on VLSI (GLSVLSI), Pittsburgh, PA, USA, May 2015,* **(Best Paper Award)**.

C73 – N. Kapadia, S. Pasricha, "VARSHA: Variation and Reliability-Aware Application Scheduling with Adaptive Parallelism in the Dark-Silicon Era," *IEEE/ACM Design Automation & Test in Europe (DATE), Grenoble, France, Mar 2015.*

C72 – S. Pasricha, I. Thakkar, "Re-architecting DRAM memory systems with 3D Integration and Photonic Interfaces", *Memory Architecture and Organization Workshop (MeAOW), New Delhi, India, Oct 2014 (Invited)*

C71 – N. Kapadia, S. Pasricha, "PRATHAM: A Power Delivery-Aware and Thermal-Aware Mapping Framework for Parallel Embedded Applications on 3D MPSoCs," *IEEE International Conference on Computer Design (ICCD), Seoul, Korea, Oct 2014.*

C70 – I. Thakkar, S. Pasricha, "3D-Wiz: A Novel High Bandwidth, Optically Interfaced 3D DRAM Architecture with Reduced Random Access Time," *IEEE International Conference on Computer Design (ICCD), Seoul, Korea, Oct 2014.*

C69 – Y. Zou, S. Pasricha, "HEFT: A Hybrid System-Level Framework for Enabling Energy-Efficient Fault-Tolerance in NoC based MPSoCs," ACM/*IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New Delhi, India, Oct 2014.*

C68 – Y. Xiang, S. Pasricha, "Fault-Aware Application Scheduling in Low Power Embedded Systems with Energy Harvesting," ACM/*IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New Delhi, India, Oct 2014.*

C67 – M. Oxley, E. Jonardi, S. Pasricha, A. A. Maciejewski, G. Koenig and H. J. Siegel "Thermal, Power, and Co-location Aware Resource Allocation in Heterogeneous Computing Systems," *IEEE International Green Computing Conference (IGCC), Dallas, TX, USA, 2014.*

C66 – D. Dauwe, R. Friese, S. Pasricha, A. A. Maciejewski, G. A. Koenig, H. J. Siegel, " Modeling the Effects on Power and Performance from Memory Interference of Co-located Applications in Multicore Systems," *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA), Las Vegas, NV, USA, 2014.*

C65 – H. J. Siegel, B. Khemka, R. Friese, S. Pasricha, A. A. Maciejewski, G. A. Koenig, S. Powers, M. Hilton, J. Rambharos, G. Okonski, and S. W. Poole, "Energy-Aware Resource Management for Computing Systems," *7th International Conference on Contemporary Computing (IC3), Noida, India,*

Aug. 2014.

C64 – B. Khemka, G. A. Koenigz, R, Friese, S. Powers, S. Pasricha, A. A. Maciejewski, M. Hilton, R. Rambharos, H. J. Siegel, Steve Poole, "Utility Driven Dynamic Resource Management in an Oversubscribed Energy-Constrained Heterogeneous System", *23rd International Heterogeneity in Computing Workshop (HCW), Phoenix, AZ, USA*, May 2014.

C63 – Y. Xiang, S. Pasricha, "A Hybrid Framework for Application Allocation and Scheduling in Multicore Systems with Energy Harvesting", *ACM Great Lakes Symposium on VLSI (GLSVLSI), Houston, TX, USA*, May. 2014.

C62 – D. Jaramillo, V. Ugave, R. Smart, S. Pasricha, "A Secure Cross-Platform Hybrid Mobile Enterprise Voice Agent," *IEEE SoutheastCon, Lexington, KY, USA,* Mar 2014

C61 – T. Pimpalkhute, S. Pasricha, "An Application-Aware Heterogeneous Prioritization Framework for NoC based Chip Multiprocessors", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2014.

C60 – S. Bahirat, S. Pasricha, "HELIX: Design and Synthesis of Hybrid Nanophotonic Application-Specific Network-On-Chip Architectures", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2014.

C59 – S. Bahirat, S. Pasricha, "3D HELIX: Design and Synthesis of Hybrid Nanophotonic Application-Specific 3D Network-On-Chip Architectures", *Workshop on Exploiting Silicon Photonics for Energy-efficient Heterogeneous Parallel Architectures (SiPhotonics)*, Jan. 2014.

C58 – T. Pimpalkhute, S. Pasricha, "NoC Scheduling for Improved Application-Aware and Memory-Aware Transfers in Multi-Core Systems", *IEEE International Conference on VLSI Design (VLSID), Mumbai, India,* Jan. 2014.

C57 – N. Kapadia, S. Pasricha, "Process Variation Aware Synthesis of Application-Specific MPSoCs to Maximize Yield", *IEEE International Conference on VLSI Design (VLSID), Mumbai, India*, Jan. 2014.

C56 – M. Oxley, S. Pasricha, H. J. Siegel, and A. Maciejewski, "Energy and Deadline Constrained Robust Stochastic Static Resource Allocation", *Workshop on Power and Energy Aspects of Computation (PEAC) held in conjunction with the 10th International Conference on Parallel Processing and Applied Mathematics (PPAM), Warsaw, Poland,* Sep. 2013.

C55 – R. Friese, T. Brinks, C. Oliver, A. Maciejewski, H. J. Siegel, S. Pasricha, "A Machine-by-Machine Analysis of a Bi-Objective Resource Allocation Problem", *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA), Las Vegas, NV, USA,* Jul. 2013.

C54 – D. Young, J. Smith, S. Pasricha, A. Maciejewski and H. J. Siegel, "Heterogeneous Makespan and Energy Constrained DAG Scheduling", *International Workshop on Energy Efficient High Performance Parallel and Distributed Computing (EEHPDC), New York, NY, USA,* Jun. 2013.

C53 – Y. Xiang, S. Pasricha, "Harvesting-Aware Energy Management for Multicore Platforms with Hybrid Energy Storage", *ACM Great Lakes Symposium on VLSI (GLSVLSI), Paris, France,* May. 2013.

(76 papers accepted out of 238 submissions: 32% acceptance rate)

C52 – N. Kapadia, S. Pasricha, "A Co-Synthesis Methodology for Power Delivery and Data Interconnection Networks in 3D ICs", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2013.

C51 – N. Kapadia, S. Pasricha, "VERVE: A Framework for Variation-Aware Energy Efficient Synthesis of NoC-based MPSoCs with Voltage Islands", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2013.

C50 – Y. Zou, S. Pasricha, "Reliability-Aware and Energy-Efficient Synthesis of NoC based MPSoCs", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2013.

C49 – Y. Xiang, S. Pasricha, "Thermal-Aware Semi-Dynamic Power Management for Multicore Systems with Energy Harvesting", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2013.

C48 – M. Salas, S. Pasricha, "The Roce-Bush Router: A Case for Routing-centric Dimensional Decomposition for Low-latency 3D NoC Routers", *ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 171-180, Tempere, Finland,* Oct 2012. *(48 papers accepted out of 163 submissions: 29% acceptance rate)*

C47 – A. M. Al-Qawasmeh, S. Pasricha, A. M. Maciejewski, and H. J. Siegel, "Thermal-Aware Performance Optimization in Power Constrained Heterogeneous Data Centers", *21st International Heterogeneity in Computing Workshop (HCW), pp. 27-40, Shanghai, China,* 2012.

C46 – B. Donohoo, C. Ohlsen, S. Pasricha, C. Anderson, "Exploiting Spatiotemporal and Device Contexts for Energy-Efficient Mobile Embedded Systems", *IEEE/ACM Design Automation Conference (DAC), pp. 1274-1279, San Francisco, CA, USA,* Jul. 2012. *(168 papers accepted out of 741 submissions: 23% acceptance rate)*

C45 – S. Bahirat, S. Pasricha, "A Particle Swarm Optimization Approach for Synthesizing Application-specific Hybrid Photonic Networks-on-Chip", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA*, Mar. 2012.

C44 – N. Kapadia, S. Pasricha, "A Power Delivery Network Aware Framework for Synthesis of 3D Networks-on-Chip with Multiple Voltage Islands", *IEEE International Conference on VLSI Design (VLSID), Hyderabad, India,* Jan. 2012. *(71 out of 218 papers accepted: 32.7% acceptance rate)*

C43 – S. Pasricha, "A Framework for TSV Serialization-aware Synthesis of Application Specific 3D Networks-on-Chip", *IEEE International Conference on VLSI Design (VLSID), Hyderabad, India,* Jan. 2012. (*71 out of 218 papers accepted: 32.7% acceptance rate)*

C42 – Y. Zou, Y. Xiang, S. Pasricha, "Analysis of On-chip Interconnection Network Interface Reliability in Multicore Systems", *IEEE International Conference on Computer Design (ICCD), Amherst, MA, USA,* Oct. 2011. *(57 out of 206 papers accepted: 28% acceptance rate)*

C41 – B. Donohoo, C. Ohlsen, S. Pasricha, "AURA: An Application and User Interaction Aware Middleware Framework for Energy Optimization in Mobile Devices", *IEEE International Conference on Computer Design (ICCD), Amherst, MA, USA,* Oct. 2011. *(57 out of 206 papers accepted: 28% acceptance rate)*

C40 – D. Young, J. Apodaca, L. Briceno, J. Smith, S. Pasricha, A. Maciejewski, H. Siegel, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou, "Energy-Constrained Dynamic Resource Allocation in a Heterogeneous Computing Environment", *Fourth International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2), Taipei, Taiwan,* 2011.

C39 – J. Apodaca, D. Young, L. Briceno, J. Smith, S. Pasricha, A. Maciejewski, H. Siegel, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou, "Stochastically Robust Static Resource Allocation for Energy Minimization with a Makespan Constraint in a Heterogeneous Computing Environment", *ACS/IEEE International Conference on Computer Systems and Applications (AICCSA), Sharm El-Sheikh, Egypt,* 2011 **(Best Paper Award)**

C38 – N. Kapadia, S. Pasricha, "VISION: A Framework for Voltage Island Aware Synthesis of Interconnection Networks-on-Chip", *IEEE Great Lakes Symposium on VLSI (GLSVLSI), Lausanne, Switzerland,* May 2011. *(57 out of 207 papers accepted: 28% acceptance rate)*

C37 – S. Pasricha, Y. Zou, "A Low Overhead Fault Tolerant Routing Scheme for 3D Networks-on-Chip", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA,* Mar. 2011. (92 out of 290 papers accepted: 31.7% acceptance rate)

C36 – S. Kwon, S. Pasricha, "POSEIDON: A Framework for Application-Specific Network-on-Chip Synthesis for Heterogeneous Chip Multiprocessors", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA,* Mar. 2011. *(92 out of 290 papers accepted: 31.7% acceptance rate)*

C35 – S. Pasricha, Y. Zou, "NS-FTR: A Fault Tolerant Routing Scheme for Networks on Chip with Permanent and Runtime Intermittent Faults", *IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan,* Jan. 2011. *(35% acceptance rate)*

C34 – S. Pasricha, S. Bahirat, "OPAL: A Multi-Layer Hybrid Photonic NoC for 3D ICs", *IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan,* Jan. 2011. *(119 out of 340 papers accepted: 35% acceptance rate)*

C33 – S. Pasricha, Y. Zou, D. Connors, H. J. Seigel, "OE+IOE: A Novel Turn Model Based Fault Tolerant Routing Scheme for Networks-on-Chip", *IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS),* pp. 85-93, *Arizona, USA,* Oct. 2010. *(33 papers accepted out of 98 submissions: 34% acceptance rate)*

C32 – S. Pasricha, "Carbon Nanotube Global Interconnects for Emerging Chip Multiprocessors", *21st Annual IEEE Workshop on Interconnections within High Speed Digital Systems (HSD),* May 2010 **(Invited)**

C31 – S. Bahirat, S. Pasricha, "UC-PHOTON: A Novel Hybrid Photonic Network-on-Chip for Multiple Use-Case Applications", *IEEE International Symposium on Quality Electronic Design (ISQED), Santa*

Clara, CA, USA, pp. 721-729, Mar. 2010 **(Best Paper Award)** *(32.6% acceptance rate)*

C30 – L. A. D. Bathen, Y. Ahn, S. Pasricha, N. Dutt, "A Methodology for Power-aware Pipelining via High-Level Performance Model Evaluations", *IEEE International Workshop on Microprocessor Test and Verification (MTV), Austin, TX, USA*, pp. 19-24, Dec. 2009.

C29 – L. A. D. Bathen, Y. Ahn, N. Dutt, S. Pasricha, "Inter-kernel Data Reuse and Pipelining on Chip-Multiprocessors for Multimedia Applications", *IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia)*, pp. 45-54, *Grenoble, France*, Oct. 2009.

C28 – S. Bahirat, S. Pasricha, "Exploring Hybrid Photonic Networks-on-Chip for Emerging Chip Multiprocessors", *IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS)*, pp. 129-136, *New York, NY, USA*, Oct. 2009. *(51 papers accepted out of 157 submissions: 32% acceptance rate)*

C27 – S. Pasricha, "Exploring Serial Vertical Interconnects for 3D ICs", *IEEE/ACM Design Automation Conference (DAC)*, pp. 581-586, *San Francisco, CA, USA*, Jul. 2009. *(22% acceptance rate)*

C26 – R. Kost, D. Connors, S. Pasricha, "Characterizing the Use of Program Vulnerability Factors for Studying Transient Fault Tolerance in Multi-core Architectures", *Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS)*, pp. 1-11, Jun. 2009.

C25 – A. Gupta, S. Pasricha, N. Dutt, F. Kurdahi, K. Khouri, M. Abadir, "On-Chip Communication Architecture Based Thermal Management for SoCs", *IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, pp. 76-79, *Hsinchu, Taiwan*, Apr. 2009.

C24 – S. Pasricha, N. Dutt, F. Kurdahi, "Dynamically Reconfigurable On-Chip Communication Architectures for Multi Use-Case Chip Multiprocessor Applications", *IEEE/ACM Asia & South Pacific Design Automation Conference (ASP-DAC)*, pp. 25-30, *Yokohama, Japan*, Jan. 2009. *(116 papers accepted out of 355 submissions: 32.6% acceptance rate)*

C23 – S. Pasricha, F. Kurdahi, N. Dutt, "Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications", *IEEE International Conference on VLSI Design (VLSID)*, pp. 499-504, *New Delhi, India*, Jan. 2009. *(79 papers accepted out of 320 submissions, 24.6% acceptance rate)*

C22 – L. A. D. Bathen, S. Pasricha, N. Dutt, "A Framework for Memory-aware Multimedia Application Mapping on Chip-Multiprocessors", *IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia)*, pp. 89-94, *Atlanta, GA, USA*, Oct. 2008.

C21 – Y. Park, S. Pasricha, F. Kurdahi, N. Dutt, "Methodology for Multi-Granularity Embedded Processor Power Model Generation for an ESL Design Flow", *IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS)*, pp. 255-260, *Atlanta, GA, USA*, Oct. 2008. *(44 papers accepted out of 143 submissions: 31% acceptance rate)*

C20 – S. Pasricha, F. Kurdahi, N. Dutt, "System Level Performance Analysis of Carbon Nanotube Global Interconnects for Emerging Chip Multiprocessors", *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, pp. 1-7, *Anaheim, CA, USA*, Jun. 2008.

C19 – H. Homayoun, S. Pasricha, M. Makhzan, A. Veidenbaum, "Dynamic Register File Resizing to Improve Embedded Processor Performance and Energy-delay Efficiency", *IEEE/ACM Design Automation Conference (DAC),* pp. 68-71, *Anaheim, CA, USA,* Jun. 2008. *(23% acceptance rate)*

C18 – D. Cho, S. Pasricha, I. Issenin, N. Dutt, Y. Paek, "Compiler Driven Data Layout Optimization for Regular/Irregular Array Access Patterns", *ACM SIGPLAN-SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES),* pp. 41-50, *Tucson, AZ, USA,* Jun. 2008. *(17 regular papers accepted among 68 submissions: 25% acceptance rate)*

C17 – H. Homayoun, S. Pasricha, M. Makhzan, A. Veidenbaum, "Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-of-Order Embedded Processors", *ACM SIGPLAN-SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES),* pp. 71-78, *Tucson, AZ, USA,* Jun. 2008. *(17 regular papers accepted among 68 submissions: 25% acceptance rate)*

C16 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "Incorporating PVT Variations in System-level Power Exploration of On-Chip Communication Architectures", *IEEE International Conference on VLSI Design (VLSID),* pp. 363-370, *Hyderabad, India,* Jan. 2008.

C15 – S. Pasricha, N. Dutt, "ORB: An On-chip Optical Ring Bus Communication Architecture for Multi-Processor Systems-on-Chip", *IEEE/ACM Asia & South Pacific Design Automation Conference (ASPDAC),* pp. 789-794, *Seoul, Korea,* Jan 2008. *(100 regular papers accepted among 350 submissions: 28.5% acceptance rate)*

C14 – Y. Park, S. Pasricha, F. Kurdahi, N. Dutt, "System Level Power Estimation Methodology with H.264 Decoder Prediction IP Case Study", *IEEE International Conference on Computer Design (ICCD),* pp. 601-608, *Lake Tahoe, CA, USA,* Oct. 2007. (*21% acceptance rate*)

C13 – S. Pasricha, N. Dutt, "On-chip Communication Architecture Synthesis for High Performance MPSoCs", *Semiconductor Research Corporation* (*SRC) TechConnect*, Nov. 2007.

C12 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "System-Level Power-Performance Trade-Offs in Bus Matrix Communication Architecture Synthesis", *IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS),* pp. 300-305, *Seoul, Korea,* Oct 2006. *(46 papers accepted out of 183 submissions: 25% acceptance rate)*

C11 – G. Madl, S. Pasricha, Q. Zhu, L. Bathen, N. Dutt, "Formal Performance Evaluation of AMBA-based System-on-Chip Designs", *6th Annual ACM Conference on Embedded Software (EMSOFT)*, pp. 311-320, *Seoul, Korea,* Oct. 2006. (*29 papers accepted out of 131 submissions: 22% acceptance rate*)

C10 – S. Pasricha, N. Dutt, "COSMECA: Application Specific Co-Synthesis of Memory and Communication Architectures for MPSoC", *IEEE/ACM Design Automation and Test in Europe Conference (DATE),* pp. 1-6, *Munich, Germany,* Mar. 2006. (*233 papers accepted out of 834 submissions: 28% acceptance rate*)

C9 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Constraint-Driven Bus Matrix Synthesis for MPSoC", *IEEE/ACM Asia & South Pacific Design Automation Conference (ASPDAC),* pp. 1-6, Yokohama, Japan,

Jan. 2006. **(Best Paper Award)** *(135 papers accepted out of 432 submissions: 31% acceptance rate)*

C8 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Using TLM for Exploring Bus-based SoC Communication Architectures", *IEEE Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pp. 79-85, *Samos, Greece,* Jul. 2005.

C7 – S. Pasricha, N. Dutt, E. Bozorgzadeh, M. Ben-Romdhane, "Floorplan-aware Automated Synthesis of Bus-based Communication Architectures", *IEEE/ACM Design Automation Conference (DAC*), pp. 565-570, *Anaheim, CA, USA,* Jun. 2005. **(Best Paper Award Candidate)** *(21% acceptance rate)*

C6 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Automated Throughput-driven Synthesis of Bus-based Communication Architectures", *IEEE/ACM Asia South Pacific Design Automation Conference (ASPDAC)*, pp. 495-498, *Shanghai, China*, Jan. 2005. (99 regular papers accepted out of 692 submissions: 14.3% acceptance rate)

C5 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Fast Exploration of Bus-based On-chip Communication Architectures", *IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS)*, pp. 242-247, *Stockholm, Sweden,* Sep. 2004. *(39 papers accepted out of 159 submissions: 24.5% acceptance rate)*

C4 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Extending the Transaction Level Modeling Approach for Fast Communication Architecture Exploration", *IEEE/ACM Design Automation Conference (DAC),* pp. 113-118, *San Diego, CA, USA,* Jun 2004. *(21% acceptance rate)*

C3 – S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt, N. Subramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices", *IEEE Embedded Systems for Real-Time Multimedia (ESTIMEDIA)*, pp. 11-17, Oct. 2003.

C2 – S. Pasricha, A. Veidenbaum, "Improving Branch Prediction Accuracy in Embedded Processors in the Presence of Context Switches", *IEEE International Conference on Computer Design (ICCD),* pp. 526-531, San Jose, CA, USA, Oct. 2003. *(33.4% acceptance rate)*

C1 – S. Pasricha, "Transaction Level Modeling of SoC using SystemC 2.0", *Synopsys User Group Conference (SNUG), Bangalore, India,* May 2002.

Conference Tutorials

TU6 – S. Pasricha, "Silicon Nanophotonics for Future Manycore Chips: Opportunities and Challenges" Half day tutorial at IEEE VLSI Design Conference (VLSID), *Pune, India,* Jan 2018.

TU5 – A. T-Sanial, S. Pasricha, P. Pande, K. Chakrabarty, "3D Integration: Quo Vadis?" *Full day tutorial at IEEE Design Automation and Test in Europe Conference, (DATE), Lausanne, Switzerland,* Mar 2017.

TU4 – S. Pasricha, N. Dutt, L. Benini, "On-Chip Communication Architectures: Buses, Networks-on-Chip, and Beyond", *Full day tutorial at 41st IEEE/ACM International Symposium on Microarchitecture (MICRO), Lake Como, Italy,* Nov. 2008.

TU3 – S. Pasricha, K. Lahiri, N. Dutt, "Modeling, Analysis and Design of Bus-based SOC Communication Architectures", *Half day tutorial presented at IEEE Design Automation and Test in Europe Conference, (DATE), Nice, France,* Apr. 2007.

TU2 – S. Pasricha, K. Banerjee, L. Benini, K. Lahiri and N. Dutt, "SoC Communication Architectures: Technology, Current Practice, Research and Trends", *Full day tutorial presented at IEEE VLSI Design Conference (VLSID), Bangalore, India,* Jan. 2007.

TU1 – S. Pasricha, N. Dutt, "SoC Communication Architectures: Current Practice, Research and Trends", *Half day tutorial presented at IEEE Asia and South Pacific Design Automation Conference (ASPDAC), Yokohama, Japan,* Jan. 2006.

Journal Guest Editorials

GE3 – E. Fusella, M. Nikdast, I. O. Connor, J. Flich, S. Pasricha, "Guest Editors' Introduction: Emerging Networks-on-Chip Designs, Technologies, and Applications", *ACM Journal on Emerging Technologies in Computing Systems (JETC), 2019.*

GE2 – D. Zhu, M. Shafique, M. Lin, S. Pasricha, "Guest Editorial: Special Issue on Low-Power Dependable Computing", *IEEE Transactions on Sustainable Computing (TSUSC), 3(3):137-138, 2018.*

GE1 - Y. Xu, S. Pasricha, "Guest Editor's Introduction: Special Issue on Silicon Nanophotonics for Future Multicore Architectures", *IEEE Design and Test (IEEE D&T), 2014.*

Invited Workshop Talks

W10 – I. Thakkar, S. Pasricha, "Analyzing Voltage Bias and Temperature Induced Aging Effects in Photonic Interconnects for Manycore Computing", *North American Workshop on Silicon Photonics for High Performance Computing (SPHPC), May 2018.*

W9 – S. Pasricha, "Cross-layer Fault Resilience for Silicon Photonic Interconnection Networks", *International Workshop on Cross-Layer Resilience (IWCR), Jul 2016.*

W8 – S. Pasricha, I. Thakkar, "Re-architecting DRAM memory systems with 3D Integration and Photonic Interfaces", *Memory Architecture and Organization Workshop (MeAOW), Oct 2014.*

W7 – S. Pasricha, "Enabling Cross-layer Fault Resilience for On-Chip Networks in SoCs," 2nd *NSF/SRC/DFG International Workshop on Cross-Layer Resilience (IWCR), Jul 2014.*

W6 – M. Oxley, S. Pasricha, H. J. Siegel, and A. A. Maciejewski, "Stochastic-Based Deadline-Aware and Energy-Constrained Robust Static Resource Management," *Workshop on Algorithms and Scheduling Techniques for Exascale Systems, sponsor: Schloss Dagstuhl - Leibniz Center for Informatics, Wadern, Germany, Sep. 2013.*

W5 – S. Pasricha, "Enabling Fault Resilient Interconnection Networks," *NSF/SRC/DFG International Workshop on Cross-Layer Resilience (IWCR), Jul 2013*

W4 – S. Pasricha, "Design Automation Challenges at the Extreme Scale: A System Level Perspective," *NSF/CCC Workshop for Extreme Scale Design Automation (ESDA), Jun 2013*

W3 – S. Pasricha, "Design Automation for Emerging Technologies: An Interconnect Perspective," *NSF/CCC Workshop for Extreme Scale Design Automation (ESDA), Jun 2013.*

W2 – S. Pasricha, S. Bahirat, "Design and Exploration of the PHOTON Hybrid Nanophotonic-electric On-chip Communication Architecture", *IEEE CANDE Workshop,* Oct. 2009.

W1 – S. Pasricha, "Customizing Memories for MPSoCs", *Workshop on Compiler-Assisted System-On-Chip Assembly (CASA),* Oct. 2009.

Invited Seminar Talks

T40 – "Silicon Photonics for Post Moore Communication and Computing," *Invited panel talk at the IEEE/ACM International Symposium on Microarchitecture, Network on Chip Architectures (NoCArc) conference, Oct 2020.*

T39 – "Enabling Smart Underground Mining with an Integrated Context-Aware Wireless Cyber-Physical Framework," *2019 Cyber-Physical Systems Principal Investigators' Meeting, National Science Foundation, Nov 2019.*

T38 – "Green Computing with Geo-Distributed Datacenters," *Invited panel talk at the IEEE Green and Sustainable Computing (IGSC) conference, Oct 2019.*

T37 – "Energy Challenges with Computing: from Internet-of-Things to Datacenters," *Invited seminar at the Energy Institute at Colorado State University, May 2019.*

T36 – "Smart Software for the Internet of Future Things," *Invited seminar at the Distinguished Seminar Series at Washington State University, Pullman, WA, USA, Dec 2018.*

T35 – "Enabling Smart Underground Mining with an Integrated Context-Aware Wireless Cyber-Physical Framework," *2018 Cyber-Physical Systems Principal Investigators' Meeting, National Science Foundation, Nov 2018.*

T34 – "Internet of Future Things," *Invited seminar at Politecnico di Torino, Turin, Italy, Oct 2018.*

T33 – "Securing Photonic NoC Architectures from Hardware Trojans " *IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Torino, Italy, Oct 2018.*

T32 – "Internet of Future Things: How can we get there?" *Colorado State University Monfort Lecture, Apr 2018.*

T31 – "Enabling Smart Underground Mining with an Integrated Context-Aware Wireless Cyber-Physical Framework," *2017 Cyber-Physical Systems Principal Investigators' Meeting, National Science Foundation, Nov 2017.*

T30 – "Energy-Efficient and Robust Middleware Prototyping for Smart Mobile Computing," *IEEE International Symposium on Rapid System Prototyping (RSP), Seoul, Korea, Oct 2017.*

T29 – "Network-on-Chip Architectures: Evolution and Future Challenges," Xilinx, Longmont, CO, May 2016

T28 – "Cross-Layer Fault Resilience for Interconnection Networks in Multi-core SoCs," SRC Annual Review, Apr 2016

T27 – "Illuminating the Future of Multicore Computing with Silicon Nanophotonic NoCs," IEEE VLSI Design Conference, Jan 2016

T26 – "Integrated Photonics in Future Multicore Computing: New Directions in Dependability and Power Efficiency," Keynote, IEEE Second Workshop on Low-Power Dependable Computing (LPDC), Dec 2015.

T25 – Bhavesh Khemka, Dylan Machovec, Howard Jay Siegel, Anthony A. Maciejewski, and Sudeep Pasricha, "Parallel Tasks: Utility and Energy," presented at Durmstrang Program Review, sponsor: Oak Ridge National Laboratory, Hanover, MD, Oct. 2015.

T24 – "Cross-Layer Fault Resilience for Interconnection Networks in Multi-core SoCs," SRC Annual Review, May 2015

T23 – "Multicore Embedded Systems and High Performance Computing Laboratory: Research Spotlight", *ISTeC Industry Advisory Council Meeting, Fort Collins,* Apr 2015.

T22 – Bhavesh Khemka, Ryan Friese, Howard Jay Siegel, Anthony A. Maciejewski, and Sudeep Pasricha, "Utility and Energy," presented at Durmstrang Program Review, sponsor: Oak Ridge National Laboratory, Linthicum, MD, Oct. 2014.

T21 – "Assistive Technologies for Rehabilitation," Department of Occupational Therapy Seminar, Colorado State University, Sep 2014.

T20 – "Cross-Layer Fault Resilience for Interconnection Networks in Multi-core SoCs," SRC Annual Review, May 2014

T19 – "Energy and Reliability Frontiers in Embedded, Mobile, and High Performance Computing," Computer Science/ISTeC Colloquium, Colorado State University, Mar 2014.

T18 – "Job Schedulers and Resource Managers: Utility and Energy," DoE/DoD Quarterly Review, Sep 2013.

T17 – "Cross-Layer Fault Resilience for Interconnection Networks in Multi-core SoCs," SRC e-Kickoff meeting for grant, Jul 2013

T16 – "On-chip Photonic Networks: Trends and Opportunities", *Intel, San Francisco,* Jun 2012.

T15 – "3D ICs: System Level Challenges", *Cadence, San Jose,* Jun 2012.

T14 – "Multi-core Embedded Computing Systems Lab: Research Spotlight", *ISTeC Industry Advisory Council Meeting, Fort Collins,* Nov 2011.

T13 – "Multi-core Embedded Computing Systems Lab: Research Spotlight", *CSU Industry Advisory Board Meeting, Fort Collins,* May 2011.

T12 – "Multi-core Embedded Computing Systems Lab: Research Overview", *AMD, Fort Collins,* Dec. 2010.

T11 – "Multi-core Embedded Computing Systems: Overview and Research Opportunities", *CSU Research Information Session,* Nov. 2010.

T10 – "Multi-core Embedded Computing Systems (MECS) Lab: Research Overview", *Intel, Fort Collins,* Sep. 2010.

T9 – "Networks on Chip and Beyond", *BMAC, CS Department Seminar Series,* Nov. 2009.

T8 – "Trends in On-Chip Communication: Networks on Chip", *DENALI, San Francisco,* Jun. 2009.

T7 – "On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *University of California, Santa Barbara,* Feb. 2008

T6 – "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *University of Florida, Gainsville,* Mar. 2007

T5 – "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *Distinguished Lecture Series, Columbia University,* Mar. 2007

T4 – "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *Colorado State University,* Mar. 2007

T3 – "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *Washington University, St, Louis,* Feb. 2007

T2 – "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *University of Nebraska, Lincoln,* Feb. 2007

T1 – "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip", *ICS Seminar Series, University of California, Irvine*, Jan. 2007.

Research Posters (Non-Conference)

P18 – S. Tiku, S. Pasricha, "SARTHI: A Secure, Accurate, Real-Time, and Heterogeneity-Resilient Indoor Localization Framework for Smartphones", ACM/IEEE Design Automation Conference SIGDA Ph.D. forum, Jun. 2019. **(Best Poster Award)**

P17 – "Enabling Smart Underground Mining with an Integrated Context-Aware Wireless Cyber-Physical Framework," *2017 Cyber-Physical Systems Principal Investigators' Meeting, National Science Foundation, Nov 2017.*

P16 – Y. Raparti, S. Pasricha, "RELAX: Cross-Layer Resource Management for Reliable NoC-based 2D and 3D Manycore Architectures in the Dark Silicon Era", ACM/IEEE Design Automation Conference SIGDA Ph.D. forum, Jun. 2018.

P15 – H. Mahajan, T. Bradley, S. Pasricha, "Engineering Safer Systems in an Increasingly Complex World", Colorado State University Graduate Student Showcase, Nov. 2016.

P14 – S. V. R. Chittamuru, S. Pasricha, "Cross-Layer Framework for Reliable and Energy-Efficient Silicon Photonic NoC Design for Future Many-Core Architectures", ACM/IEEE Design Automation Conference SIGDA Ph.D. forum, Jun. 2016.

P13 – I. Thakkar, S. V. R. Chittamuru, S. Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects", ACM/IEEE Design Automation Conference Work in Progress (WIP), Jun. 2016.

P12 – S. V. R. Chittamuru, S. Pasricha, "Overcoming Data Movement Barriers in Future Many Core Chips with Silicon Nanophotonics", CSU Ventures Innovation Forum, Apr 2016.

P11 – I. Thakkar, S. Pasricha, "Improving the Performance and Power Efficiency of Memory with 3D Stacking and High-Bandwidth Optical Interfacing", CSU Ventures Innovation Forum, Apr 2016.

P10 – D. Dauwe, S. Pasricha, "Overcoming Resource Failures and Sharing Conflicts in Large-scale Datacenters and Supercomputers", CSU Ventures Innovation Forum, Apr 2016.

P9 – V. K. Kukkala, S. Pasricha, "JAMS: Jitter Aware Message Scheduling for FlexRay Automotive Networks", CSU Ventures Innovation Forum, Apr 2016.

P8 – S. Bahirat, S. Pasricha, "Design and Synthesis of Hybrid Nanophotonic NoCs for Future Many-Core Architectures", ACM/IEEE Design Automation Conference SIGDA Ph.D. forum, Jun. 2013.

P7 – N. Kapadia, S. Pasricha, "A Holistic Framework for Multi-objective Synthesis of 2D and 3D NoC-based MPSoCs with Voltage Islands", ACM/IEEE Design Automation Conference SIGDA Ph.D. forum, Jun. 2013.

P6 – N. Kapadia, S. Pasricha, "A Power Delivery Network Aware Framework for Synthesis of 3D Networks-on-Chip", IEEE Computer-Aided Network DEsign CANDE Workshop, Oct. 2011.

P5 – D. Young, J. Apodaca, L. Briceno, J. Smith, S. Pasricha, A. Maciejewski, H. Siegel, S. Bahirat, B. Khemka, A. Ramirez and Y. Zou, "Energy-Constrained Dynamic Resource Allocation in a Heterogeneous Computing Environment", FRCRC First Annual Front Range High Performance Computing Symposium, Oct. 2011. **(Winner of Best Poster Award)**

P4 – S. Bahirat, S. Pasricha, "Design and Exploration of the PHOTON Hybrid Nanophotonic-electric On-chip Communication Architecture", IEEE Computer-Aided Network DEsign CANDE Workshop, Oct. 2009

P3 – S. Pasricha, "COMMSYN: On-Chip Communication Architecture Synthesis for Multi-Processor System-on-Chips", UC Irvine School of Information and Computer Science (ICS) Seminar, May 2007

P2 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Fast Exploration of Bus-based Communication Architectures", CECS ISLPD Open House, Irvine, CA, Aug. 2004

P1 – S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt, N. Subramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices", Southern California Embedded Systems Symposium (SCESS), Irvine, CA, Sep. 2003 **(Winner of 2nd Place SCESS Best Poster Award)**

Press Coverage

A22 – "Sudeep Pasricha honored by world's largest computing society", *Colorado State University Source Magazine, Jul 2019.*

A21 – "And they're off again: CSU chosen for EcoCAR Mobility Challenge", *Colorado State University Source Magazine, Oct 2018.*

A20 – "Monfort Lecture focuses on the 'Internet of Future Things", *Colorado State University Source Magazine, Mar 2018.*

A19 – "EcoCAR 3 secures top-8 finishes and sportsmanship award at Year Three Competition", *Colorado State University Source Magazine, Jun 2017.*

A18 – "EcoCAR 3 Students Drive Innovation", *CSU College Avenue, Mar 2017.*

A17 – "Engineers Bring Tech of the Future to Life", *CSU College Avenue, Mar 2017.*

A16 – "Smartphones Can Help Reduce the Risks of Underground Accidents", *Government Technology, Oct, 2016.*

A15 – "Deep underground, smartphones can save miners' lives", *The Conversation, Oct, 2016.*

A14 – "Underground wireless system may save trapped miners with smart phones, CSU researchers say", *Colorado State University, Collegian newspaper, Aug 30, 2016.*

A13 – "Can you hear me now? CSU research could help miners stay safe", *Colorado State University, Source magazine, Aug 24, 2016.*

A12 – "Home Sweet Mind-Controlled Home", *IEEE Computer, Vol. 49, Iss. 5, pp. 98 – 101, May 2016.*

A11 – "Celebrate! Colorado State award winners", *Colorado State University Source Magazine, Apr 2016.*

A10 – "Brainy students use brain waves to control lights, open doors", *Colorado State University Source Magazine, Mar 2016.*

A9 – "Game on: CSU researchers developing video game-based therapy tool", *Colorado State University Source Magazine, Apr 2015.*

A8 – "Powering down: Researchers reducing energy usage at data centers", *Colorado State University Source Magazine, Mar 2015.*

A7 – "Wastewater Sourced Methane Powers New Wyoming Data Center", *KUNC 91.5 Community Radio for Northern Colorado/NPR digital network, Jan 2015.*

A6 – "CSU professors get $850K for green supercomputers", *Northern Colorado Business Report, Jun 2013.*

A5 – "CSU engineering team to tackle challenge of green supercomputing". *Innovationews, Jun 2013.*

A4 – "Researchers awarded $850K to keep supercomputers from being energy hogs", *Networkworld, Jun 2013.*

A3 – "Grant helps CSU professors design green supercomputers", *Coloradoan, Jun 2013.*

A2 – "CSU EE professor is only Colorado-based recipient of 2013 Air Force Young Investigator Award", *Innovationews, Mar 2013.*

A1 – "AFOSR awards grants to 40 scientists and engineers through its Young Investigator Research Program", *Eurekalert, Jan 2013.*

Patents (patents under review not listed)

PAT1 – S. Pasricha, N. Dutt, M. Ben Romdhane, "Method for the fast exploration of bus-based communication architectures at the cycle-count-accurate-at-transaction-boundaries (CCATB) abstraction", Patent number 7,778,815, Aug. 2010

Published Software

S1 – EXPRESSION: Architecture Description Language (ADL) based Retargetable Compiler-Simulator tool-suite (available at http://www.ics.uci.edu/~aces), 2004.

PhD Forum

PF1 – S. Pasricha, "COMMSYN: On-Chip Communication Architecture Synthesis for Multi-Processor System-on-Chips", IEEE Design Automation and Test in Europe, (DATE), Nice, France, Apr. 2007.

Educational Activities

Ph.D. Students Graduated (Advisor)

2019 *Venkata Yaswanth Raparti,* Ph.D. in Computer Engineering
RELAX: Cross-Layer Resource Management for Reliable NoC-based 2D and 3D Manycore Architectures in the Dark Silicon Era

2018 *Ishan Thakkar,* Ph.D. in Computer Engineering
Design and Optimization of Emerging Interconnection and Memory Subsystems for Future Manycore Architectures

2018 *Daniel Dauwe,* Ph.D. in Computer Engineering
(Co-advised with Prof. H. J. Siegel)
Resource Management for Extreme Scale HPC Systems in the Presence of Failures

2018 *Sai Vineel Reddy Chittamuru,* Ph.D. in Computer Engineering
Reliable, Energy-Efficient, and Secure Silicon Photonic Network-On-Chip Design for Manycore Computing

2017 *Yahav Biran,* Ph.D. in Systems Engineering
(Co-advised with Prof. George Collins)
Cloud Computing Cost and Energy Optimization Through Federated Cloud SoS

2016 *Mark Oxley,* Ph.D. in Electrical and Computer Engineering
(Co-advised with Prof. H.J. Siegel)
Energy- and Thermal-aware Resource Management for Heterogeneous High-performance Computing Systems

2016 *Nishit Kapadia,* Ph.D. in Electrical and Computer Engineering
Design-time and run-time frameworks for multi-objective optimization of 2D and 3D NoC-based multicore computing systems

2015 *Yi Xiang,* Ph.D. in Electrical and Computer Engineering
A Semi-Dynamic Resource Management Framework for Multicore Embedded Systems with Energy Harvesting

2014 *Yong Zou,* Ph.D. in Electrical and Computer Engineering
Reliability-aware and energy-efficient system level design for networks-on-chip

2014 *Shirish Bahirat,* Ph.D. in Electrical and Computer Engineering
Design and synthesis of hybrid nanophotonic-electric network-on-chip architectures

M.S. Thesis Students Graduated (Advisor)

2019 *Blake Troksa,* M.S. in Electrical and Computer Engineering
GPU Accelerated Cone Based Shooting Bouncing Ray Tracing

2018 *Swapnil Bhosale,* M.S. in Electrical and Computer Engineering
High Performance and Energy Efficient Shared Hybrid Last Level Cache Architecture In Multicore Systems

2018 *Ninad Hogade,* M.S. in Electrical and Computer Engineering
Minimizing Energy Costs for Geographically Distributed Heterogeneous Data Centers

2017 *Aditya Khune,* M.S. in Electrical and Computer Engineering
Mobile network-aware middleware framework for energy efficient offloading of smartphone applications

2016 *Pramit Rajkrishna,* M.S. in Electrical and Computer Engineering
An integrated variation-aware mapping framework for finfet based irregular 2D MPSOCs in the dark silicon era

2015 *Eric Jonardi,* M.S. in Electrical and Computer Engineering
(Co-advised with Prof. H.J. Siegel)
A hierarchical framework for energy-efficient resource management in green data centers

2015 *Srinivas Desai,* M.S. in Electrical and Computer Engineering
Design and analysis of energy-efficient hierarchical electro-photonic network-on-chip architectures

2014 *Viney Ugave,* M.S. in Electrical and Computer Engineering
Smart indoor localization using machine learning techniques

2013 *Tejasi Pimpalkhute,* M.S. in Electrical and Computer Engineering
Heterogeneous prioritization for network-on-chip based multi-core systems

2012 *Brad Donohoo,* M.S. in Electrical and Computer Engineering

Machine learning techniques for energy optimization in mobile embedded systems

M.S. Project Students Graduated (Advisor)

2018 *Bharadwaj Gorthy,* Electrical and Computer Engineering

2018 *Varun Kilenje,* Electrical and Computer Engineering

2018 *Ayush Mittal,* Electrical and Computer Engineering

2018 *Zemin Tao,* Electrical and Computer Engineering

2017 *Rohit Kudre,* Electrical and Computer Engineering

2017 *Sai Kiran Koppu,* Electrical and Computer Engineering

2017 *Ebenezer Reniflal,* Electrical and Computer Engineering

2017 *Jingjie Zhu,* Electrical and Computer Engineering

2017 *Manoj Kumar Shivaswami,* Electrical and Computer Engineering

2016 *Haneet Mahajan,* M.S. in Electrical and Computer Engineering

2016 *Onkar Gulvani,* M.S. in Electrical and Computer Engineering

2016 *Surya Vamsi Vemparala,* M.S. in Electrical and Computer Engineering

2016 *Taylor Santiago,* M.S. in Electrical and Computer Engineering

2015 *Dher Basil Mahmood Agha,* M.S. in Electrical and Computer Engineering

2014 *Nanda Kumar Chandrasekar,* M.S. in Electrical and Computer Engineering

2014 *Yuhang Li,* M.S. in Electrical and Computer Engineering

2012 *Miguel Salas,* M.S. in Electrical and Computer Engineering

Current Post-DoC Students (Advisor)

2017- *Shirish Bahirat,* Electrical and Computer Engineering

Current Graduate Students (Advisor)

Ph.D. *Saideep Tiku,* Electrical and Computer Engineering

Ph.D. *Shoumik Maiti,* Electrical and Computer Engineering

Ph.D. *Vipin Kumar Kukkala,* Electrical and Computer Engineering

Ph.D. *Febin Sunny,* Electrical and Computer Engineering

Ph.D. *Joydeep Dey,* Electrical and Computer Engineering

Ph.D. *Asif Mirza,* Electrical and Computer Engineering

Ph.D. *Seth Hughes,* Electrical and Computer Engineering

Ph.D. *Kamil Khan,* Electrical and Computer Engineering

Ph.D. *Ninad Hogade,* Electrical and Computer Engineering

M.S. *Liping Wang,* Electrical and Computer Engineering

M.S. *Chris Langlois,* Electrical and Computer Engineering

M.S. *Jordan Tunnel,* Electrical and Computer Engineering

M.S. *Ravi Teja Jagarlapudi,* Electrical and Computer Engineering

M.S. *Anisha Aswani,* Electrical and Computer Engineering

M.S. *Prathmesh Kale,* Electrical and Computer Engineering

M.S. *Abhishek Balasubramaniam,* Electrical and Computer Engineering

Ph.D. Thesis Committee Member (Graduated)

2018 *Rabeh Ayari,* Ph.D., École Polytechnique De Montréal

2017 *Mozammel Hossain,* Ph.D. in Electrical and Computer Engineering, CSU

2016 *Yishai Statter,* Ph.D. in Electrical and Computer Engineering, CSU

2015 *Ryan Friese,* Ph.D. in Electrical and Computer Engineering, CSU

2014 *Bhavesh Khemka,* Ph.D. in Electrical and Computer Engineering, CSU

2012 *Abdulla Al-Qawasmeh,* Ph.D. in Electrical and Computer Engineering, CSU

M.S. Thesis Committee Member (Graduated)

2019 *Gabe Di Domenico,* M.S. in Mechanical Engineering

2019 *Troy Johnson,* M.S. in Mechanical Engineering

2019 *Matthew Knopf,* M.S. in Mechanical Engineering

2019 *Prerana Ghalsasi,* M.S. in Electrical and Computer Engineering

2016 *Spencer Vore,* M.S. in Mechanical Engineering

2016 *Revathy Rajasree,* M.S. in Mechanical Engineering

2015 *Divyanka Bose,* M.S. in Electrical and Computer Engineering

2015 *Roxie Mcfarland,* M.S. in Occupational Therapy

2015 *Tara Klinedinst,* M.S. in Occupational Therapy

2015 *Alexandra Gisetti,* M.S. in Occupational Therapy

2015 *Mugdha Puranik,* M.S. in Electrical and Computer Engineering

2015 *Mounica Vempa,* M.S. in Electrical and Computer Engineering

2014 *Yusra Obeidat,* M.S. in Electrical and Computer Engineering

2014 *Ajay Sagwal,* M.S. in Electrical and Computer Engineering

2014 *Vamsi Tandrapati,* M.S. in Electrical and Computer Engineering

2014 *Divyanka Bose,* M.S. in Electrical and Computer Engineering

2014 *Hrushikesh Kulkarni,* M.S. in Electrical and Computer Engineering

2014 *Sachin Soman,* M.S. in Electrical and Computer Engineering

2014 Aditi Madabhushi, M.S. in Electrical and Computer Engineering

2013 *Thiyagarajan Chockalingam,* M.S. in Computer Science

2013 *Pritam Shah,* M.S. in Electrical and Computer Engineering

2012 *Shilpa Murthy,* M.S. in Electrical and Computer Engineering

2012 *Chris Ohlsen*, M.S. in Electrical and Computer Engineering

2011 *Saket Doshi*, M.S. in Electrical and Computer Engineering

2011 *Vamshi Basupalli*, M.S. in Computer Science

2011 *Raghunandan M Narasiodeyar*, M.S. in Electrical and Computer Engineering

2010 *Tanveer Pathan*, M.S. in Computer Science

Undergraduate Honors Theses Supervised

2020 *Wes Taylor, EcoCAR4*

2019 *Samuel Havens, AR/VR based Smart Glasses*

2017 *Joel Kraft, Survey of Brain Controlled Interfaces (BCI)*

2017 *Michael Thanh, NoximGUI: An Intuitive Interface for Noxim*

2016 *Kaden Strand, Design and Integration of Control System Architecture for EcoCar3 Advanced Vehicle Technology Competition*

2015 *Rob Kahler, Exploration of Emerging Memory Technologies*

2014 *Ryan Nash, Survey of STT-RAM based Cache Architectures*

2011 *Alan Burgesser, Thermal Aware Computing in Multi-core Systems*

2009 *Michael Ullman, The Past, Present, and Future of Embedded Systems in Musical Instruments*

K-12 Student Projects Supervised

2018 *Amelia Cutchin, Andrew Scott, 'Tender Eats' Android app*

2018 *Lakshya Jaishankar, Intruder Alarm System*

2018 *Xinxin Liu, Smart Security Camera*

2017 *Shreya Pandit, Assistive Technologies in Rehabilitation*

2017 *Tyler Carr, Research Website Design*

2016 *Amita Pandey, Raspberry Pi based Lawn Sprinkler*

2015 *Micah Z, Motion Sensing and Alert System*

2015 *Raymond Chai, Raspberry Pi based Web Server*

2015 *Dylan Ko, Android App Development and Raspberry Pi based Security System*

Undergraduate Senior Design Projects Supervised

2020 Mason Cheshier, JT Bovee, Wes Taylor, *Ecocar CAV*

2020 Joshua Weiser, Yousef Al-Foudari, *GATOR*

2020 Jackson Krebill, Devon Fossceco, *Ecocar Controls*

2020 Tyler Engle, Hussain Ahmed, *Smartphone Indoor Localization*

2020 Tyler Feist, Connor Haden, *Smart Glasses*

2019 Kaitlin (Murphy) Britt, Greyson Kehm, *Thinking Cap*

2019 Sam Havens, Shane Beuning, *Smart Glasses*

2019 Courtney Case, Samual McCallum, Zhaoyang Meng, *Woodward FPGA-based Filter Design*

2019 Lane Barnes, Ethan D. Courtney, Mitch Avis, *Smartphone Indoor Localization*

2019 Shaolong Shi, Haoying Wang, Abdulla Alghfeli, Abdulaziz Alshamsi, *Advanced Driver Assistance Systsems (ADAS)*

2018 Aubrey Davis, Connor Wagener, Ben Gratias, Tyler Fowler, *Smartphone Indoor Localization*

2018 Juhyup Kim, Yi Wang, Alex Segura, Stephen Bellig, *Ecocar3 ADAS*

2018 Jeremy Lazzari, Kevin (Xinzhe) Cao, Eric Vargas, *Ecocar3 Controls*

2017 Elias Fenster, Christian Carrico, *ECC Memory*

2017 John Lynch, Jorden Ham, Conner Jackson, *Linux Drone*

2017 Joel Kraft, Mengjia Yi, Jason Gardner, *Brain Controlled Smart Wheelchair*

2017 Jesus Garcia, Qingruo (Angela) Si, *Ecocar3 Controls*

2017 Veronica Foster, Carter Hough, *Ecocar3 Keysight*

2017 Jordan Tunnel, Derek Isabelle, Drew DeVos, *Ecocar3 ADAS*

2016 Fatimah Alkhonaizi, Justin Howell, Tyler Marts, *Smart Display Monitors*

2016 Bryce Depperman, Daniel Gold, Luke Trostel, *Memory Architecture Design and Exploration*

2016 Bryce Coulson**,** Christian R, Conor Hart, *Games and Therapeutic Tools for Rehabilitation*

2016 Kaden Strand, Katie Wetzel, *EcoCar3 Controls*

2016 Colt Darien**,** Edward Okvath III, Kyle Van Cleave, *Brain Controlled Smart Home*

2016 Alex Banner, Brendan Isbell, Scott Smith, *Advanced Driver Assistance System*

2015 Michael Rowack, Chris Hesser, Corey LeFevre**,** *Serious Games for Rehabilitation*

2015 Marcus Johnson, Rob Kahler, *Memory Architecture Design and Exploration*

2014 Casey Anderson, Laura Imbler, Sam Felton**,** *Puzzle Assembly*

2014 Jacob Thornton, Ryan Nash, Joshua Wallace, *Serious Games for Rehabilitation*

2014 Daniel White, Salem Alaqeel, Jacob Vickers, Lucas Wadman, John Allison, Trevor Pier, *MIMER Robot*

2013 Gregorio Campuzano, Nathan Olson, Alexander Vlahinos, *Augmented Reality Games for Upper Limb Stroke Rehabilitation*

2013 Austin Steingrube, Josh Cecchinelli, *LARRY Autonomous Robot*

2012 Anthony Navarro, Michael Martin, Tyler Kron, *LARVA Drone*

2012 Ryan Bonavida, Ahmad Marafi, *Cloud Offloading for Smartphones*

2012 Jacob Poore, Baris Tevflak, *Upper Limb Stroke Rehabilitation using Augmented Reality*

2012 Sam Fortier, Odunlami Adefisayo, John Fisher, *Engine Systems*

2011 Celia Pietsch, Nick Brantley, Ethyn Feldman, *Wearable Computing*

2011 Alan Burgesser, Steven Dorlac, *Thermal Aware Design of Chip Multiprocessors*

2010 Jonathon Cox, *TUX: Inverted Pendulum*

Undergraduate Vertically Integrated Project (ViP) Students Supervised

2019-20 Drew Rackow, *Ecocar CAV*

2019-20 Zach Fuelberth, *Ecocar CAV*

2019-20 Huanjia Liu, *Ecocar CAV*

2019-20 Kevin Alamo-Perez, *Ecocar CAV*

2018-19 JT Bovee, *Ecocar3 ADAS*

2018-19 Hein Thant, *Ecocar3 ADAS*

2018-19 Xinming Ye, *Ecocar3 ADAS*

2018-19 Wes Taylor, *Ecocar3 ADAS*

2018 Haoying Wang, *Ecocar3 ADAS*

2017 Minjie Shen, *Ecocar3 ADAS*

2017 Yi Wang, *Ecocar3 ADAS*

2017 Juhyup Kim, *Ecocar3 ADAS*

2016 Jordan Tunnel, *Ecocar3 ADAS*

2016 Adam Hicks, *GATOR*

Student Awards

2019 Best Poster Award, IEEE/ACM DAC Ph.D. Forum *(S. Tiku)*

2019 A. Richard Newton Young Student Fellow award at IEEE/ACM DAC 2019 (*A. Mirza*)

2019 A. Richard Newton Young Student Fellow award at IEEE/ACM DAC 2019 (*F. Sunny*)

2017 Dr. Donald Streit Sportsmanship Award, Ecocar3 Competition

2017 IEEE IPDPS Travel Grant (*D. Dauwe*)

2016 CSU Graduate Student Council Travel Grant (*I. Thakkar*)

2016 A. Richard Newton Young Student Fellow award at IEEE/ACM DAC 2016 (*V. Y. Raparti*)

2015 Travel Grant, ACM/IEEE NOCS Conference, 2015 (*V. Y. Raparti*)

2015 Travel Grant, ACM GLSVLSI Conference, 2015 (*S. V. R. Chittamuru*)

2015 Best Senior Design project award, ECE student vote (*Christopher Hesser, Corey Lefevre, Michael Rowack*)

2014 Best Senior Design project award, ECE students and ME Advisory Panel vote (*Daniel White, Salem Alaqeel, Jacob Vickers, Lucas Wadman, John Allison, Trevor Pier*)

2014 1st place, CSU IEEE Open Design Competition, EMG ECG HW/SW (*A. Steingrube*)

2013 1st place, CSU E-days, LARRY Autonomous Vehicle (*A. Steingrube, J. Cecchinelli*)

2013 A. Richard Newton Young Student Fellow award at IEEE/ACM DAC 2013 (*Y. Xiang*)

2013 A. Richard Newton Young Student Fellow award at IEEE/ACM DAC 2013 (*P. Rajakrishna*)

2013 CSU Graduate School Professional Development Travel Grant (*N. Kapadia*)

2012 Student Fellowship Award, IEEE VLSID (*N. Kapadia*)

2012 1st place, CSU E-days, LARVA Drone (*M. Martin, A. Navarro, T. Kron*)

2012 3rd place, CSU E-days, Upper-Limb Stroke Rehabilitation, (*B. Tefvik, J. Poore*)

2012 IEEE Region 5 Best Undergraduate Paper Award (*M. Martin, A. Navarro, T. Kron*)

2011 Young Student Support Program Award at IEEE/ACM DAC (*N. Kapadia*)

2011 NSF Travel Grant, CANDE Workshop (*N. Kapadia*)

2011 Best Paper Award, ACS/IEEE Intl. Conf. on Computer Systems and Applications (*D. Young*)

2011 Best Poster Award, Front Range High Performance Computing Symposium (*D. Young*)

2011 3rd place, CSU E-days, Upper-Limb Stroke Rehabilitation, (*C. Pietsch, N. Brantley*)

2010 Young Student Support Program Award at IEEE/ACM DAC (*S. Bahirat*)

2010 NSF Travel Grant, CANDE Workshop (*S. Bahirat*)

2010 Best Paper Award, IEEE International Symposium on Quality Electronic Design (*S. Bahirat*)

2010 2nd place, CSU E-days, TUX2-Inverted Pendulum (*J. Cox*)

2009 NASA Space Grant Symposium First Place Award (*J. Cox*)

Visiting Scholars

2019	*Sri Harsha Gade*, IIIT, New Delhi, India
2013-2014	*Prof. Myeong Jin Lee*, Korea Aerospace University, Gyeonggi, Korea
2010-2011	*Prof. Kangchul Kim*, Chonnam University, Korea
2010	*Prof. Gu Haiyun*, Shanghai Maritime University, China
2009-2010	*Soohyun Kwon* (PhD student) Kyungpook National University, Korea

Teaching and Evaluation
(Department course evaluation average: 8 out of 10)

Semester	Course	Course Evaluation
Fall 2020	**ECE 581C1** *Embedded Systems and Machine Learning*	- out of 10
Spring 2020	**ECE 554** *Computer Architecture*	- out of 10
Spring 2020	**ECE 452** *Computer Organization and Design*	- out of 10
Fall 2019	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	- out of 10
Spring 2019	**ECE 554** *Computer Architecture*	- out of 10
Spring 2019	**ECE 452** *Computer Organization and Design*	- out of 10
Fall 2018	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.7 out of 10
Spring 2018	**ECE 452** *Computer Organization and Design*	9.8 out of 10
Fall 2017	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.3 out of 10
Spring 2017	**ECE 452** *Computer Organization and Design*	9.3 out of 10
Fall 2016	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	10 out of 10
Spring 2016	**ECE 452** *Computer Organization and Design*	9.6 out of 10
Fall 2015	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.4 out of 10
Spring 2015	**ECE 661** *Advanced Embedded System Design*	9.7 out of 10
Spring 2015	**ECE 452** *Computer Organization and Design*	9.6 out of 10

Fall 2014	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	8.9 out of 10
Spring 2014	**ECE 554** *Computer Architecture*	9.3 out of 10
Spring 2014	**ECE 452** *Computer Organization and Design*	8.9 out of 10
Fall 2013	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.0 out of 10
Spring 2013	**ECE 554** *Computer Architecture*	9.2 out of 10
Spring 2013	**ECE 452** *Computer Organization and Design*	8.7 out of 10
Fall 2012	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.1 out of 10
Spring 2012	**ECE 554** *Computer Architecture*	9.2 out of 10
Spring 2012	**ECE 452** *Computer Organization and Design*	8.7 out of 10
Fall 2011	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.3 out of 10
Spring 2011	**ECE 661** *Advanced Embedded System Design*	9.6 out of 10
Spring 2011	**ECE 452** *Computer Organization and Design*	8.6 out of 10
Fall 2010	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	8.7 out of 10
Spring 2010	**ECE 452** *Computer Organization and Design*	9.6 out of 10
Fall 2009	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	9.4 out of 10
Spring 2009	**CS/ECE 561** *Hardware/Software Design of Embedded Systems*	7.0 out of 10
Fall 2008	**ECE 451** *Digital System Design*	8.8 out of 10

New Courses Designed

2020	CS/ECE581C1 Embedded Systems and Machine Learning
2008-present	CS/ECE 561 Hardware/Software Design of Embedded Systems
2011-present	ECE 661 Advanced Embedded System Design

Professional Development

2019	Participated in the Women and Under-Represented Minorities Special Interest Workshop at NSF (November 2019)

2018 Participated in the Women and Under-Represented Minorities Special Interest Workshop at NSF (November 2018)

2017 Participated in the Women and Under-Represented Minorities Special Interest Workshop at NSF (November 2017)

2015 Participated in Workshop on Embedded and Cyber-Physical Systems Education (WESE)

2014 Participated in Workshop on Embedded and Cyber-Physical Systems Education (WESE)

Professional and University Service

SIG, Conference, Journal, and Newsletter Editorial Boards

2019-2020 Guest Editor, IEEE Design and Test, Special Issue on Design and Management of Mobile Platforms

2019-present Senior Associate Editor, ACM Journal on Emerging Technologies in Computing (JETC)

2018 IEEE Council on Electronic Design Automation (CEDA), Executive Committee

2017-present Guest Editor, ACM Journal on Emerging Technologies in Computing (JETC), Special Issue on Emerging Networks-on-Chip: Designs, Technologies, and Applications

2017-present Associate Editor, IEEE Consumer Electronics Magazine

2016-present Guest Editor, IEEE Transactions on Sustainable Computing (TSUSC), Special Issue on Low Power and Dependable Computing

2016-present Associate Editor, Elsevier Journal of Parallel and Distributed Computing (JPDC)

2016-present Associate Editor, IEEE Transactions on Computer-aided Design (TCAD)

2015-present Associate Editor, IEEE Design and Test (D&T)

2014-2019 Associate Editor, IEEE Transactions on Multi-Scale Computing Systems (TMSCS)

2013-present Associate Editor, ACM Transactions on Embedded Computing Systems (TECS)

2013-2014 Guest Editor, IEEE Design and Test, Special Issue on Silicon Nanophotonics

2012-2016 Editor-in-Chief, ACM Special Interest Group on Design Automation (SIGDA) E-news

2012-2014 Information Director, ACM Transactions on Design Automation of Electronic Systems

2011-2014 Advisory Board, ACM Special Interest Group on Design Automation (SIGDA)

2011 Associate Editor, Embedded Systems & Software, IEEE/ACM Design Automation Conference

2011 Associate Editor, ACM Special Interest Group on Design Automation (SIGDA) E-news

Proposal Review Panels

2012-present National Science Foundation

Conference Steering Committee

2018-present International Heterogeneity in Computing Workshop (HCW)

2018-present North American Workshop on Silicon Photonics for High Performance Computing (SPHPC)

2017-present IEEE International Conference on Smart Electronic Systems (iSES)

2017-present IEEE International Green and Sustainable Computing Conference (IGSC)

2015-2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)

Conference Organizing Committee (General Chair)

2020 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2019 IEEE International Heterogeneity in Computing Workshop (HCW)

2018 IEEE International Conference on Smart Electronic Systems (iSES)

2018 IEEE International Green and Sustainable Computing Conference (IGSC)

2017 IEEE International Conference on Embedded Software and Systems (ICESS)

Conference Organizing Committee (Technical Program Committee Chair)

2019 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2019 ACM/IEEE International Conference on HW/SW Co-design and System Synthesis (CODES+ISSS)

2018 ACM/IEEE International Conference on HW/SW Co-design and System Synthesis (CODES+ISSS)

2018 IEEE International Heterogeneity in Computing Workshop (HCW)

2018 IEEE International Conference on Embedded and VLSI Design (VLSID)

2017 IEEE International Green and Sustainable Computing Conference (IGSC)

2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)

Conference Organizing Committee (Other Chaired Positions)

2021 IEEE/ACM Embedded Systems Week (ESWEEK), *Virtual Conference Chair*

2020 ACM/IEEE International Conference on Computer-Aided Design (ICCAD), *Track Chair*

2020 ACM/IEEE Design Automation Conference (DAC), *Track Chair*

2019 ACM/IEEE International Conference on Computer-Aided Design (ICCAD), *Track Chair*

2019 IEEE Intl' Symp. on High-Performance Computer Architecture, *Student Travel Chair*

2018 ACM/IEEE International Conference on Computer-Aided Design (ICCAD), *Track Chair*

2018 ACM/IEEE Design Automation Conference (DAC), *SIGDA PhD Forum Chair*

2018 ACM Great Lakes Symposium on VLSI (GLSVLSI), *Track Chair*

2017 ACM/IEEE International Symposium on Networks-on-Chip (NOCS), *Finance Chair*

2017 IEEE/ACM Embedded Systems Week (ESWEEK), *Web Chair*

2017 ACM/IEEE Design Automation Conference (DAC), *SIGDA University Demo Chair*

2017 ACM/IEEE Design Automation Conference (DAC), *SIGDA PhD Forum Chair*

2016 ACM/IEEE Design Automation Conference (DAC), *SIGDA University Demo Chair*

2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), *Publicity Chair*

2016 ACM/IEEE International Symposium on Networks-on-Chip (NOCS), *Special Sessions Chair*

2016 ACM Great Lakes Symposium on VLSI (GLSVLSI), *Track Chair*

2015 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), *Publicity Chair*

2015 ACM/IEEE International Symposium on Networks-on-Chip (NOCS), *Special Sessions Chair*

2015 ACM/IEEE Design Automation Conference (DAC), *Track Chair*

2015 ACM Great Lakes Symposium on VLSI (GLSVLSI), *Track Chair*

2015 IEEE Midwest Symposium on Circuits and Systems (MWSCAS), *Publications Chair*

2014 IEEE/ACM Embedded Systems Week (ESWEEK), *Finance Chair*

2014 ACM Great Lakes Symposium on VLSI (GLSVLSI), *Track Chair*

2014 ACM/IEEE Design Automation Conference (DAC), *Track Chair*

2014 University Booth, ACM/IEEE Design Automation Conference (DAC), *Publicity Chair*

2013 ACM/IEEE International Symposium on Networks-on-Chip (NOCS), *Finance Chair*

2012 ACM/IEEE International Conference on Computer-Aided Design (ICCAD) *CADathlon Chair*

2012 IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), *Publicity Chair*

2011 IEEE International Conference on Electronics, Circuits, and Systems, *Track Chair*

2011 ACM/IEEE International Conference on Computer-Aided Design (ICCAD) *CADathlon Chair*

2011 ACM International Conference on HW/SW Co-design and System Synthesis, *Track Chair*

2011 IEEE International Conference on Computer Systems and Applications, *Vice Program Chair*

2011 IEEE International Conference on VLSI Design, *Track Chair*

2010 ACM/IEEE International Conference on Computer-Aided Design (ICCAD) *CADathlon Chair*

2009 IEEE International Conference on VLSI Design, *Track Chair*

2009 ACM/IEEE International Conference on Computer-Aided Design (ICCAD) *CADathlon Chair*

Technical Program Committee (TPC) Member

2021	IEEE/ACM International Conference on Cyber-Physical Systems (ICCPS)
2021	IEEE/ACM Design, Automation and Test in Europe (DATE)
2020	IEEE/ACM Design Automation Conference (DAC)
2020	IEEE International Symposium on Quality Electronic Design (ISQED)
2020	IEEE/ACM Design, Automation and Test in Europe (DATE)
2020	IEEE International Conference on VLSI Design (VLSID)
2019	IEEE International Conference on Computer Design (ICCD)
2019	ACM Great Lakes Symposium on VLSI (GLSVLSI)
2019	IEEE International Symposium on Quality Electronic Design (ISQED)
2019	IEEE/ACM Design, Automation and Test in Europe (DATE)
2019	IEEE International Conference on VLSI Design (VLSID)
2018	IEEE Workshop on Energy-Efficient Big Data Analytics (BigData)
2018	IEEE Workshop on Advances in Parallel and Distributed Comp. Models (APDCM)
2018	ACM Great Lakes Symposium on VLSI (GLSVLSI)
2018	ACM/IEEE International Symposium on Networks-on-Chip (NOCS)
2018	IEEE International Parallel & Distributed Processing Symposium (IPDPS)
2018	IEEE/ACM Design, Automation and Test in Europe (DATE)
2018	IEEE/ACM Design Automation Conference (DAC)
2018	IEEE International Symposium on Quality Electronic Design (ISQED)
2018	IEEE Workshop on Advances in Parallel and Distributed Comp. Models (APDCM)
2017	ACM/IEEE International Symposium on Networks-on-Chip (NOCS)
2017	ACM Great Lakes Symposium on VLSI (GLSVLSI)
2017	IEEE International Symposium on Quality Electronic Design (ISQED)

2017 IEEE/ACM Design Automation Conference (DAC)

2017 IEEE Workshop on Advances in Parallel and Distributed Comp. Models (APDCM)

2017 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2017 IEEE International Parallel & Distributed Processing Symposium (IPDPS)

2017 IEEE International Heterogeneity in Computing Workshop (HCW)

2016 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2016 IEEE International Green and Sustainable Computing Conference (IGSC)

2016 IEEE Workshop on Advances in Parallel and Distributed Comp. Models (APDCM)

2016 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2016 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2016 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2016 IEEE International Symposium on Quality Electronic Design (ISQED)

2016 IEEE International Conference on VLSI Design (VLSID)

2016 Workshop on Exploiting Silicon Photonics for Energy-efficient Heterogeneous Parallel Architectures (SiPhotonics)

2015 IEEE International Workshop on Network on Chip Architectures (NoCArc)

2015 IEEE International Green and Sustainable Computing Conference (IGSC)

2015 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2015 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2015 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2015 IEEE/ACM Design Automation Conference (DAC)

2015 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2015 Workshop on Exploiting Silicon Photonics for Energy-efficient Heterogeneous Parallel Architectures (SiPhotonics)

2015 IEEE International Symposium on Quality Electronic Design (ISQED)

2015 IEEE International Conference on VLSI Design (VLSID)

2014 IEEE International Workshop on Network on Chip Architectures (NoCArc)

2014 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2014 ACM International Workshop on Manycore Embedded Systems (MES)

2014 IEEE International Green Computing Conference (IGCC)

2014 IEEE/ACM Design Automation Conference (DAC)

2014 IEEE International Conference on VLSI Design (VLSID)

2014 Workshop on Exploiting Silicon Photonics for Energy-efficient Heterogeneous Parallel Architectures (SiPhotonics)

2014 IEEE International Symposium on Quality Electronic Design (ISQED)

2014 IEEE/ACM Design, Automation and Test in Europe (DATE)

2013 ACM International Workshop on Manycore Embedded Systems (MES)

2013 IEEE International Workshop on Network on Chip Architectures (NoCArc)

2013 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2013 IEEE International System-on-Chip Conference (SOCC)

2013 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2013 IEEE/ACM Design Automation Conference (DAC)

2013 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2013 IEEE/ACM Design, Automation and Test in Europe (DATE)

2013 IEEE International Symposium on Quality Electronic Design (ISQED)

2013 Interdisciplinary Engineering Education Conference (IEDEC)

2012 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2012 IEEE International Workshop on Network on Chip Architectures (NoCArc)

2012 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2012 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2012 IEEE International Symposium on Quality Electronic Design (ISQED)

2012 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2012 Interdisciplinary Engineering Education Conference (IEDEC)

2012 IEEE/ACM Design, Automation and Test in Europe (DATE)

2011 IEEE International Workshop on Network on Chip Architectures (NoCArc)

2011 IEEE/ACM Design, Automation and Test in Europe (DATE)

2011 IEEE International Symposium on Quality Electronic Design (ISQED)

2011 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2011 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2011 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2011 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2010 IEEE International Workshop on Network on Chip Architectures (NoCArc)

2010 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2010 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2010 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2010 IEEE International Symposium on Quality Electronic Design (ISQED)

2010 IEEE International Conference on VLSI Design (VLSID)

2010 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2009 ACM/IEEE Intl. Conference on HW/SW Co-design and System Synth. (CODES+ISSS)

2009 ACM/IEEE Special Interest Group on Design Automation (SIGDA) DAC PhD Forum

2009 IEEE International Symposium on Quality Electronic Design (ISQED)

2008 IEEE International Symposium on Quality Electronic Design (ISQED)

Conference Technical Session Chair

2020 IEEE/ACM Embedded Systems Week (CASES/ESWEEK)

2020 IEEE/ACM Design Automation Conference (DAC)

2019 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2019 IEEE/ACM Embedded Systems Week (CODES+ISSS/ESWEEK)

2018 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2018 IEEE/ACM Embedded Systems Week (CODES+ISSS/ESWEEK)

2018 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2018 IEEE International Heterogeneity in Computing Workshop (HCW)

2018 IEEE International Conference on VLSI Design (VLSID)

2017 IEEE International Green and Sustainable Computing Conference (IGSC)

2017 IEEE/ACM Embedded Systems Week (CODES+ISSS/ESWEEK)

2017 IEEE/ACM Design Automation Conference (DAC)

2017 IEEE International Conference on VLSI Design (VLSID)

2016 IEEE/ACM Embedded Systems Week (CODES+ISSS/ESWEEK)

2016 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2015 IEEE/ACM Embedded Systems Week (CASES/ESWEEK)

2015 IEEE/ACM Embedded Systems Week (CODES+ISSS/ESWEEK)

2015 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)

2015 IEEE/ACM Design Automation Conference (DAC)

2014 IEEE/ACM Embedded Systems Week (CODES+ISSS/ESWEEK)

2014 2nd NSF/SRC/DFG International Workshop on Cross-Layer Resilience (IWCR)

2014 IEEE International Symposium on Quality Electronic Design (ISQED)

2013 ACM/IEEE International Symposium on Networks-on-Chip (NOCS)

2013 IEEE/ACM Design Automation Conference (DAC)

2013 IEEE International Symposium on Quality Electronic Design (ISQED)

2011 IEEE International Symposium on Quality Electronic Design (ISQED)

2010 IEEE/ACM Intl. Conference on HW/SW Codesign and System Synthesis (CODES+ISSS)

2010 IEEE/ACM Design Automation Conference (DAC)

2009 IEEE International Conference on VLSI Design (VLSID)

2009 IEEE/ACM Intl. Conference on HW/SW Codesign and System Synthesis (CODES+ISSS)

2008 IEEE/ACM Intl. Conference on HW/SW Codesign and System Synthesis (CODES+ISSS)

2007 IEEE International Conference on Computer Design (ICCD)

K-12 Outreach Service

2020-present Poudre School District Computer Science Advisory Committee

2018-present Advisory Board, Fossil Ridge High School STEM Committee

University, College, and Department Service

2019-2020 Faculty Search Committee, Electrical and Computer Engineering

2019-present Department of Electrical and Computer Engineering, Graduate Committee

2019 eSports Working Group, CSU

2017-2019 Digital Measures/FSAS Strategic Committee, WSCOE

2017-2018 Chair, Faculty Search Committee, Electrical and Computer Engineering

2016-2017 Faculty Search Committee, Electrical and Computer Engineering

2015-2016 Faculty Search Committee, Electrical and Computer Engineering

2015 Postdoctoral Search Committee, Mechanical Engineering

2015 COE Awards Committee

2015 Chair, Engineering Network Services (ENS) Services Review

2014-present Chair, Computer Engineering, Department of Electrical and Computer Engineering

2014-2015 Faculty Search Committee, Dept. of Mechanical Engineering

2013-2014 ECE Faculty Representative, ENS Computing Support Specialist search committee

2013-2014 ECE Faculty Representative, Engineering Student Technology Committee (ESTC)

2013-present Department of Electrical and Computer Engineering, Advisory Committee

2013-present Department of Electrical and Computer Engineering, Web Redesign Committee

2013-present Department of Electrical and Computer Engineering, Curriculum Committee

2012-2013 College of Engineering Representative, University Faculty Council

2008-2013 Education Advisory Committee, CSU Information Science and Technology Center (ISTeC)