Ryan G. Kim

CONTACT INFORMATION

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RESEARCH INTERESTS

Design of scalable, fully-adaptive manycore systems assisted by machine learning. This includes machine learning to 1) develop suitable policies for holistic run-time control of the entire manycore system; and 2) accelerate and improve EDA techniques for design-time optimization. Relevant interests include: system design for heterogeneous (CPU/GPU/FPGA) systems; machine/deep learning acceleration through manycore systems; scalable power management using Dynamic Voltage Frequency Scaling (DVFS) and Voltage Frequency Islands (VFI); and on-chip energy-efficient wireless networks, network topology creation using complex network theory, and communication protocols for manycore processors.

[Last Updated: June 2019]

EDUCATION

Ph.D. in Electrical Engineering, Washington State University - May 2016
Dissertation: *Wireless NoC and Voltage Frequency Island Co-Design for Energy-Efficient Many-Core Platforms*
Depth: Computer Engineering, **Breadth**: Microelectronics
Advisors: Prof. Partha Pande (Washington State Univ.) and Prof. Radu Marculescu (Carnegie Mellon Univ.)

B.S. in Computer Engineering, Washington State University - Dec. 2011

EXPERIENCE

Assistant Professor **Aug. 2018 - Present**
Department of ECE, Colorado State University

Postdoctoral Researcher **Mar. 2016 - May 2018**
Department of ECE, Carnegie Mellon University
Supervisor: Prof. Radu Marculescu

- Investigation into fully-adaptive mechanism for manycore systems
- Investigation into user-aware mobile device optimization
- Investigation into machine learning for circuit place and route
- Machine Learning-based power management strategies for Voltage Frequency Island (VFI)-partitioned manycore systems
- Analysis of social interactions on Twitter using Deep Learning algorithms
- Design of network architectures for heterogeneous manycore systems

Graduate Research Assistant **Aug. 2012 - Mar. 2016**
School of EECS, Washington State University
Advisor: Prof. Partha Pratim Pande

- Working on applying machine learning techniques to system-level power management
- Applied the Voltage Frequency Island (VFI) paradigm to create energy-efficient multicore platforms.
- Design of on-chip wireless multicore architectures, specifically mm-wave wireless small-world network-on-chip (mSWNoC).
- Design of adaptive and non-adaptive shortest-path layered routing (ALASH and LASH respectively) to achieve high-throughput on the swNoC architecture.
- Implementation and optimization of dynamic thermal management (DTM) and dynamic voltage and frequency scaling (DVFS) using the ALASH routing strategy.

Graduate Technical Intern **Aug. 2015 - Dec. 2015**
Circuits Research Labs (CRL)
Intel Labs

- Testing and characterization of a low-power research prototype see 6 in Journal Publications
- Software abstraction to interface with the prototype

Graduate Technical Intern **Aug. 2014 - Dec. 2014**
Circuits Research Labs (CRL)
Intel Labs

- Design of a low-power research prototype see 6 in Journal Publications
- Design and FPGA validation of a low-power, low-profile, cutting-edge System on Chip (SoC)

Visiting Researcher **May 2014 - Aug. 2014**
ECE, Carnegie Mellon University
Advisor: Prof. Radu Marculescu

- Design of voltage frequency island (VFI)-specific mSWNoC topologies to optimize energy and performance.
- Modification of the GEM5 system simulator to include a better network-on-chip model to analyze VFI effects on energy and execution time.

Engineering Intern **Oct. 2010 - July 2012**
Digilent Inc.

- Technical support for all customer technical product queries
- Wrote product acceptance test firmware for FPGA and microcontroller boards
- Verified and developed new microcontroller products
- Wrote reference materials for new prototype and production boards
- Created designs to demonstrate the capabilities of new microcontroller and FPGA products.

Journal Publications

1. S. Musavvir, A. Chatterjee, **R.G. Kim**, D.H. Kim, and P.P. Pande, "Inter-Tier Process Variation-Aware Monolithic 3D NoC Architectures," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (**TVLSI**), under review.
2. B.K. Joardar, **R.G. Kim**, J.R. Doppa, P.P. Pande, D. Marculescu, and R. Marculescu, "Learning-Based Application-Agnostic 3D NoC Design for Heterogeneous Manycore Systems," *IEEE Transactions on Computers* (**TC**), vol. 68, no. 6, June 2019.
3. **R.G. Kim**, Janardhan Rao Doppa, Partha Pratim Pande, Diana Marculescu, and Radu Marculescu, "Machine Learning and Manycore Systems Design: A Serendipitous Symbiosis," *IEEE Computer*, vol. 51, no. 7, pp. 66-77, July 2018.
4. W. Choi, K. Duraisamy, **R.G. Kim**, J.R. Doppa, P.P. Pande, D. Marculescu, R. Marculescu, "On-Chip Communication Network for Efficient Training of Deep Convolutional Networks on Heterogeneous Manycore Systems," *IEEE Transactions on Computers* (**TC**), vol. 67, no. 5, pp. 672-686, May 2017. **[IEEE TC Featured Paper of the Month]**
5. **R.G. Kim**, W. Choi, Z. Chen, J.R. Doppa, P.P. Pande, D. Marculescu, R. Marculescu, "Imitation Learning for Dynamic VFI Control in Large Scale Manycore Systems," *IEEE Trans. on Very Large Scale Integr. (VLSI) Syst.* (**TVLSI**), vol. 25, no. 9, pp. 2458-2471, Sept 2017.
6. S. Paul, V. Honkote, **R. Kim**, T. Majumder, P. Aseron, V. Grossnickle, R. Sankman, D. Mallik, T. Wang, S. Vangal, J. Tschanz, V. De, "A Sub-cm^3 Energy-Harvesting Stacked Wireless Sensor Node Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14nm Tri-gate CMOS for Always-On Always-Sensing Applications," *IEEE Journal of Solid State Circuits* (**JSSC**), vol. 52, no. 4, pp. 961-971, Apr 2017.

7. **R.G. Kim**, W. Choi, Z. Chen, P.P. Pande, D. Marculescu, R. Marculescu, "Wireless NoC and Dynamic VFI Co-Design: Energy Efficiency without Performance Penalty," *IEEE Trans. on Very Large Scale Integr. (VLSI) Syst.* (**TVLSI**), vol. 24, no. 7, pp. 2488-2501, July 2016. **[IEEE CAS 2018 VLSI Systems Best Paper]**
8. **R.G. Kim**, W. Choi, G. Liu, E. Mohandesi, P.P. Pande, D. Marculescu, R. Marculescu, "Wireless NoC for VFI-Enabled Multicore Chip Design: Performance Evaluation and Design Trade-offs," *IEEE Trans. on Computers* (**TC**), vol. 64, no. 4, pp. 1323-1336, Apr. 2016. **[IEEE TC Featured Paper of the Month]**
9. J. Murray, **R. Kim**, P. Wettin, P.P. Pande, B. Shirazi, "Performance Evaluation of Congestion-Aware Routing with DVFS on a Millimeter-Wave Small World Wireless NoC," *ACM Journal on Emerging Technologies in Computing Syst.* (**JETC**), vol. 11, no. 2, Article 17, Nov. 2014.
10. P. Wettin, **R. Kim**, J. Murray, X. Yu, P.P. Pande, A. Ganguly, and D. Heo, "Design Space Exploration for Wireless NoCs Incorporating Irregular Network Routing," *IEEE Trans. on Computer-Aided Design of Integr. Circuits and Syst.* (**TCAD**), vol.33, no.11, pp.1732,1745, Nov. 2014.

Conference Publications

11. B.K. Joardar, **R.G. Kim**, J.R. Doppa, and P.P. Pande, "Design and Optimization of Heterogeneous Manycore Systems Enabled by Emerging Interconnect Technologies: Promises and Challenges," in *Design, Automation & Test in Europe Conference & Exhibition (**DATE**)*, 2019. [**Special Session**]
12. **R.G. Kim**, J.R. Doppa, and P.P. Pande, "Machine Learning for Design Space Exploration and Optimization of Manycore Systems," in *International Conference on Computer-Aided Design (ICCAD)*, 2018. [**Special Session**]
13. J.R. Doppa, **R.G. Kim**, M. Isakov, M. Kinsy, H. Kwon, T. Krishna, "Adaptive Manycore Architectures for Big Data Computing," in *Networks-on-Chip (**NoCS**), 2017 Eleventh IEEE/ACM International Symposium on*, vol., no., pp., 19-20 Oct. 2017. [**Special Session**]
14. B.K. Joardar, W. Choi, **R.G. Kim**, J.R. Doppa, P.P. Pande, D. Marculescu, R. Marculescu, "3D NoC-Enabled Heterogeneous Manycore Architectures for Accelerating CNN Training: Performance and Thermal Trade-offs," in *Networks-on-Chip (**NoCS**), 2017 Eleventh IEEE/ACM International Symposium on*, vol., no., pp., 19-20 Oct. 2017.
15. W. Choi, K. Duraisamy, **R.G. Kim**, J.R. Doppa, P.P. Pande, R. Marculescu, D. Marculescu, "Hybrid Network-on-Chip Architectures for Accelerating Deep Learning Kernels on Heterogeneous Manycore Platforms." *Compilers, Architecture and Synthesis for Embedded Systems, 2016 International Conference on (**CASES**)*, vol., no., Oct. 2016.
16. S. Paul, V. Honkote, **R. Kim**, T. Majumder, P. Aseron, V. Grossnickle, R. Sankman, D. Mallik, S. Jain, S. Vangal, J. Tschanz, V. De, "An Energy Harvesting Wireless Sensor Node for IoT Systems Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14nm Tri-Gate CMOS," *2016 IEEE Symposium on VLSI Circuits (**VLSI-Circuits**)*, 2016.
17. P.P. Pande, **R.G. Kim**, W. Choi, Z. Chen, D. Marculescu, and R. Marculescu. 2015. "The (Low) Power of Less Wiring: Enabling Energy Efficiency in Many-Core Platforms Through Wireless NoC." *In Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**)*. [**Invited Paper**]
18. W. Choi, S. Hajiamini, **R.G. Kim**, A. Rahimi, N. Hezarjaribi, P.P. Pande and B. Shirazi, "Improving EDP in Wireless-Enabled Multicore Chip Via DVFS Pruning," *Midwest Symposium on Circuits and Systems (**MWSCAS**)*, vol., no., pp.1-4, 2-5 Aug. 2015.
19. K. Duraisamy, **R.G. Kim**, W. Choi, G. Liu, R. Marculescu, D. Marculescu, Partha Pratim Pande, "Energy Efficient MapReduce with VFI-enabled multicore Platforms," *Design Automation Conference (**DAC**)*, vol., no., pp.1-6, 8-12 June 2015.

20. K. Duraisamy, **R.G. Kim**, P.P. Pande, "Enhancing Performance of Wireless NoCs with Distributed MAC Protocols," *Quality Electronic Design (**ISQED**), 2015 16th International Symposium on*, vol., no., pp.406,411, 2-4 March 2015.
21. **R. Kim**, G. Liu, P. Wettin, R. Marculescu, D. Marculescu, P.P. Pande, "Energy-Efficient VFI-Partitioned Multicore Design Using Wireless NoC Architectures," *Compilers, Architecture and Synthesis for Embedded Systems (**CASES**), 2014 International Conference on*, vol., no., pp.1,9, 12-17 Oct. 2014.
22. **R. Kim**, J. Murray, P. Wettin, P.P. Pande, and B. Shirazi, "An Energy-Efficient Millimeter-Wave Wireless NoC with Congestion-Aware Routing and DVFS," *Networks-on-Chip (**NoCS**), 2014 Eighth IEEE/ACM International Symposium on*, vol., no., pp.192,193, 17-19 Sept. 2014.
23. P. Wettin, **R. Kim**, J. Murray, P.P. Pande, and B. Shirazi, "Thermal Hotspot Reduction in mm-Wave Wireless NoC Architectures," *Quality Electronic Design (**ISQED**), 2014 15th International Symposium on*, vol., no., pp.645,652, 3-5 March 2014.
24. P. Wettin, J. Murray, **R. Kim**, X. Yu, P.P. Pande, and D. Heo, "Performance Evaluation of Wireless NoCs in Presence of Irregular Network Routing Strategies," *Proceedings of IEEE Design, Automation and Test in Europe (**DATE**), 2014*, vol., no., pp.1,6, 24-28 March 2014.

Other Publications

25. **Ryan Gary Kim**, "Wireless NoC-Enabled Energy Efficient Multicore Chip Design," 2015 Design Automation Conference SIGDA PhD Forum.

Students Advised

- Mohadeseh (Shadi) Manafi Avari (PhD): 2019-Present

Teaching Experience

CSU ECE580B9: Manycore Systems Design Using Machine Learning **Spring 2019**
Instructor

CSU ECE251: Introduction to Microprocessors **Spring 2019**
Instructor

CMU 18-651: Networked Cyber-Physical Systems **Spring 2018**
Instructor/Project Mentor

CMU 18-755: Networks in the Real World **Fall 2016, Fall 2017**
Project Mentor

- Advised two-person groups in the class to investigate open-ended research problems related to complex networks in the real world.

Awards

- Best paper award: 2018 Very Large Scale Integration Systems best paper award
- Washington State University EECS Outstanding PhD Student in Computer Engineering, 2015
- Alfred Suksdorf Scholarship, Washington State University, 2012-2013
- Cougar Academic Award Recipient, Washington State University, 2008-2011
- David H. Schrader Scholarship, Washington State University School of EECS, 2008-2011
- President's Honor Roll, 2008-2011

Professional Service

Organizing Committee Member
- NOCS Publicity Chair 2019

Technical Program Committee Member
- CODES+ISSS: 2019
- CASES: 2019
- NOCS: 2017, 2018, 2019
- HiPC: 2019

Journal Reviewer: IEEE TC, IEEE TVLSI, IEEE TMSCS, IEEE TCAD, IEEE TCAS, IEEE D&T, IEEE ESL, IEEE CL, IEEE CAL, ACM TECS, ACM TODAES; Elsevier Integration; Hindawi VLSI Design
Conference Reviewer: DAC, ICCAD, IGCC, CASES, ISCAS

Invited Talks

- CMU/GTech Machine Learing in Science and Engineering (MLSE) Symposium 2018 - Machine Learning-Inspired Manycore Chip Design: Interconnect Architectures to Power Management