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Fabrication, performance and parasitic parameter extraction of 850 nm high-speed vertical-cavity lasers

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Abstract
High-speed, oxide-confined, polyimide-planarized 850 nm vertical-cavity surface emitting lasers (VCSELs) with different aperture sizes were fabricated and characterized. Comprehensive small signal measurements and analysis were conducted. The VCSELs exhibit intrinsic, parasitic and thermal maximum bandwidth limitations of 42.3 GHz, 21.5 GHz and 17.6 GHz, respectively. Devices with a 10 μm oxide aperture exhibited a maximum modulation bandwidth of 15.3 GHz, limited by thermal effects, and a modulation current efficiency factor (MCEF) of 9.2 GHz mA$^{-1/2}$. A VCSEL equivalent circuit model which incorporates the frequency dependence of the polyimide dielectric permittivity and loss is presented. A genetic algorithm (GA) was utilized to extract the parasitic circuit elements from measured microwave reflection coefficients (S_{11}) over a frequency range of 50 MHz to 20 GHz for different device sizes at different bias currents. Good agreement between extracted and calculated parasitic circuit element values was obtained. Several modifications to the device's fabrication steps and structure are suggested to further improve the device's output power and modulation bandwidth.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The demands for higher data throughput and interconnect densities in high-end computing systems are growing rapidly due to increasing chip speed and larger numbers of processors. However, current *PCB* technology faces several challenges, such as power consumption and electromagnetic interference. Optical connections will be one of the major alternatives for upgrading connection performance. AlGaAs-based 850 nm vertical-cavity surface emitting lasers (VCSELs) have been widely investigated as light sources for medium-/short-range optical interconnections ranging from the local area networks (LANs) down to the chip-to-chip links due to their low cost and small size, which allow a high-density 2D array, low power consumption, high performance and simple integration with systems. VCSEL modulation bandwidth can be increased by optical injection [1] or external modulation [2], but direct modulation is particularly attractive to maintain simple electrical, mechanical and optical system interfaces.

The relaxation oscillation frequency and parasitic circuit effects are considered the main factors affecting the VCSEL modulation response [3]. The intrinsic bandwidths of VCSELs, as demonstrated by analyzing damping in CW-driven devices [4] or time domain relaxation oscillations in gain-switched lasers [5] were 58 GHz and 70 GHz, respectively. However, extrinsic factors including parasitic circuit elements, high junction temperatures and multi-mode operation have prevented VCSELs from reaching their intrinsic capabilities. Thus, to realize VCSELs with higher modulation bandwidths, these extrinsic limiting factors need

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to be evaluated for the current structures and reduced in future structures.

Many researchers have reported methods for reducing the parasitic circuit effects such as parasitic resistances and capacitances associated with VCSELs. Various approaches to reduce the VCSEL's series resistances (top and bottom mirrors) and capacitances (junction, oxide and pad) are reported in [3, 4, 6–8]. Another factor that was observed to limit the maximum bandwidth of VCSELs is the number of transverse modes [9]. Higher modulation bandwidth was obtained from devices that operated in a single mode for an extended range above threshold [4]. While there are many interrelated factors that may contribute to single-mode operation such as current distribution, gain-mode overlap, spatial hole burning and the optical loss of higher order modes, one of the essential VCSEL fabrication parameters that can promote signal-mode operation is oxide aperture diameter, that is, making the active diameter small enough to allow only single-mode operation. Keeping this in mind, and since the laser diode bandwidth varies as $(I - I_{\text{th}})^{1/2}$, the laser must be biased at a current I several times the threshold current (I_{th}) in order to reach high frequencies. As a result, the current density (J_{th}) at which these devices operate is very high given the small oxide aperture needed for single-mode operation, which in turn produces significant junction heating. Recently, researchers have reported other techniques, such as the use of a multi-oxide layer and a micro-machined surface relieved structure [10, 11], or the incorporation of a photonic crystal pattern with an oxide-confined VCSEL structure [12].

In this paper, top-emitting, high-speed, oxide-confined, polyimide-planarized 850 nm VCSELs with different oxide aperture sizes were fabricated and characterized. The reported devices incorporate epitaxial mirror designs and p-type substrates for low series resistances [13] as well as photo-definable low-K polyimide for passivation, planarization and parasitic pad capacitance reduction [14]. The intrinsic, thermal and parasitic bandwidth limitations were investigated. Devices with a 10 μm oxide aperture exhibited a maximum thermally limited −3 dB modulation bandwidth of 15.3 GHz at a current density of 6.4 kA cm^{-2} with an intrinsic bandwidth potential of 42.3 GHz. Such a low current density should improve reliability [15–17]. A VCSEL equivalent circuit model which includes the frequency dependence of the polyimide dielectric permittivity and loss is presented, while such a dependence was ignored in previously reported VCSEL circuit models [18]. A genetic algorithm (GA) was used to extract the parasitic circuit elements from the measured microwave reflection coefficients.

The VCSEL layer structure and fabrication are reported in section 2, which also presents the basic static laser characteristics. Section 3 deals with measurements of the small signal modulation response (S_{21}) and microwave reflection coefficients (S_{11}), and determination of the bandwidth limitation mechanism. To further improve the devices' performance, this section along with section 4 also presents several suggested modifications to the presented device's fabrication steps and structure. In section 4, we present an equivalent circuit model for the VCSEL structure, which also includes the parasitic parameter extraction using GA. Finally, section 5 presents summary and conclusions.

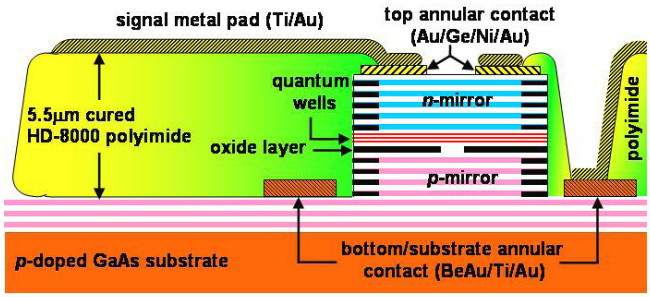

Figure 1. Cross-sectional view of an 850 nm oxide-confined polyimide-planarized VCSEL ready for testing.

2. Layer structure, fabrication and basic static characteristics

Top-emitting, high-speed, 850 nm VCSEL diodes were fabricated using an epitaxial structure grown on a p-doped substrate [13] by metal-organic chemical vapor deposition (MOCVD). The inverted polarity, i.e. p-type bottom mirror and n-type top mirror, VCSEL configuration permits simple fabrication of common anode VCSEL arrays that can be driven by circuits that employ open collector npn transistors which offer better performance than pnp transistors. Furthermore, placing the n-type mirrors above the active region (quantum wells), where the direction of the current is mainly lateral, reduces the total resistance of VCSELs with annular contacts which improves the device performance in terms of modulation bandwidth, power efficiency and internal heating. The active region consists of three GaAs quantum wells (QWs) with $Al_{0.2}Ga_{0.8}As$ spacers. The n-mirror above the active region consists of a 25-period, silicon-doped ($\sim 1 \times 10^{18}$ cm^{-3}) alternating sequence of $Al_xGa_{1-x}As$ ($x = 0.92$) and $Al_yGa_{1-y}As$ ($y = 0.16$) distributed Bragg reflector (DBR) layers for high optical reflectivity. The carbon-doped ($\sim 1 \times 10^{18}$ cm^{-3}), 35-period p-mirror below the active region also employs $Al_xGa_{1-x}As/Al_yGa_{1-y}As$ DBRs with Al fractions similar to the top n-mirrors except for a single low-index quarter wavelength ($\lambda/4$) layer adjacent to the optical cavity with $Al_{0.98}Ga_{0.02}As$ composition to increase its oxidation rate relative to the other DBR layers. The n-DBR was terminated with a phase-matching heavily doped ($\sim 2 \times 10^{19}$ cm^{-3}) GaAs layer to reduce the contact resistance.

The detailed processing steps to fabricate the VCSEL of which the cross-section is shown in figure 1 are described as follows. A processing sequence using several photomasks (mesa formation, top and bottom annular contacts, polyimide planarization, metal interconnects) was used to fabricate oxide-confined, polyimide-planarized VCSELs with coplanar wave-guide probe pads. Using a load-locked, chemically assisted ion beam etching (*CAIBE*) system, fabrication began by etching the surrounding semiconductor into the bottom, p-doped DBRs to form cylindrical (~ 5 μm height) post

structures with different diameters and exposed side walls for oxidation. Subsequent selective lateral wet oxidation of the high-Al-content $Al_{0.98}Ga_{0.02}As$ oxidation layer provides current confinement and lateral index guiding to the lasing mode. The sample was oxidized at 440 °C under flowing nitrogen, which bubbled through water at 90 °C [19] resulting in active area (oxide aperture) diameters of 10, 12 and 14 μm for devices with mesa diameters of 31, 33 and 35 μm respectively. To form the annular n-type top contact, a four-level Au/Ge/Ni/Au contact was evaporated in sequence using an e-beam evaporator at 10^{-6} Torr pressure. Before depositing the bottom annular p-type contact, the sample was soaked in an HCl/H_2O solution to remove the oxide layer formed on the etched surface during the oxidation process. This step will help reduce the bottom contact ohmic resistance. The BeAu (pre-alloyed)/Ti/Au contact was evaporated onto the partially etched p-DBR bottom mirror to form the p-type bottom contact which is connected to the substrate. Contacts were annealed at 420 °C in a nitrogen (N_2) ambient.

After contact formation, HD-8000 photo-definable polyimide (cyclic-chain polymers) was used for field insulation and device planarization due to its high inherent thermal stability, and excellent electrical and mechanical properties. One potential disadvantage of polyimide is its moisture absorption [20]. Utilizing polyimide for planarization offers lower pad capacitance than conventional silicon oxide (SiO_2, $\kappa = 3.9$) or silicon nitride (Si_3N_4, $\kappa = 7.5$) passivation since it has a relatively low dielectric constant ($\kappa = 3.4$) and can readily produce thick layers. In this case, the polyimide was cured by prolonged baking at elevated temperatures in a N_2 ambient as recommended by the manufacturer using a programmable temperature-controlled curing furnace which resulted in a thickness of about 5.5 μm. Finally, a 125 μm pitch ground-signal-ground pad configuration of Ti/Au was deposited for metal interconnects and coplanar waveguide probe pads. Here, we present the response for a 10 μm diameter aperture laser, which had the best performance, and occasionally present results for larger diameter aperture devices for comparison where applicable.

DC characteristics of the fabricated VCSELs with different oxide aperture sizes were measured at room temperature using a probe station, a four-channel HP 4145A semiconductor parameter analyzer, and a silicon photodiode with a 100 mm^2 active area and ~0.6 A W^{-1} responsivity at 850 nm wavelength. The threshold voltage, threshold current (I_{th}) and a series resistance (R_s) for VCSELs with a 31 μm mesa diameter and 10 μm diameter oxidation aperture were 1.45 V, 0.9 mA, and 69 Ω, respectively. The maximum slope efficiency (η_{slope}) above threshold is 0.12 W A^{-1} with a maximal output optical power of 0.74 mW at $I \sim 17I_{th} =$ 15 mA after which typical thermal rollover of the output optical power due to local heating is observed. The threshold current and maximum output power increased and R_s and η_{slope} decreased with increasing active area diameter. Devices with an active area diameter of 14 μm resulted in an I_{th}, a maximum output power and a series resistance of 1.5 mA, 1.4 mW (at $I \sim 17I_{th} = 25$ mA), 50 Ω and 0.11 W A^{-1}, respectively.

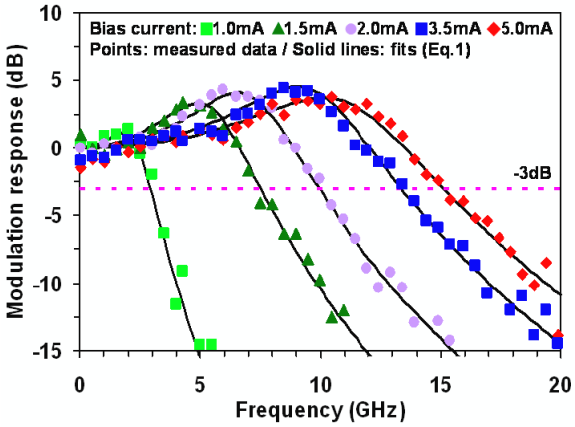

Figure 2. Measured small signal modulation response at different drive currents (points). Solid lines are fits using the three-pole transfer function (equation (1)).

The low slope efficiency and output power is due to the large number of top n-DBR mirror pairs. In recently reported results [21], the epitaxial structure with the p-side up was used to fabricate 9 μm aperture VCSELs with a η_{slope} of 0.78 W A^{-1} and a maximum output optical power of 9 mW. Compared to our design, it is believed that the reduced number of top DBR pairs, the utilization of modulation doping to reduce resistive heating and the incorporation of binary rather than ternary compositions in the bottom DBR to reduce the thermal resistance in [21] lead to better performance including the frequency response which will be discussed in section 3.

3. Dynamics and bandwidth limitations

The small signal response of the fabricated VCSELs was measured using a probe station equipped with a 20 °C constant temperature stage and high-speed air co-planar microprobe (Cascade Microtech ACP-40), 2 m of the multimode fiber, a NIST-calibrated, high-speed New Focus photodiode and attached New Focus amplifier, an HP 4145 semiconductor parameter analyzer and a calibrated HP8510*B* vector network analyzer (VNA). The bare-end fiber was actively aligned above the device under test using an *x*–*y*–*z* positioning stage to obtain maximum dc optical power.

The VCSEL's modulation response (S_{21}) and microwave reflection coefficient (S_{11}) were measured at various bias currents (I) over a frequency range up to 20 GHz. S_{21} and S_{11} measurements were terminated for each device when there was no noticeable increase in the measured 3 dB bandwidth with further increase in I. The modulation response characteristics for a 10 μm diameter aperture laser are presented here. The microwave reflection coefficient results will be reported and discussed in section 4. Figure 2 shows the frequency modulation (intensity modulation) response of a VCSEL with a 10 μm diameter active area at several bias current levels.

The maximum modulation bandwidth (f_{3dB}) is 15.3 GHz when biased at $I \sim 5.4I_{th}$ (5 mA) at room temperature.

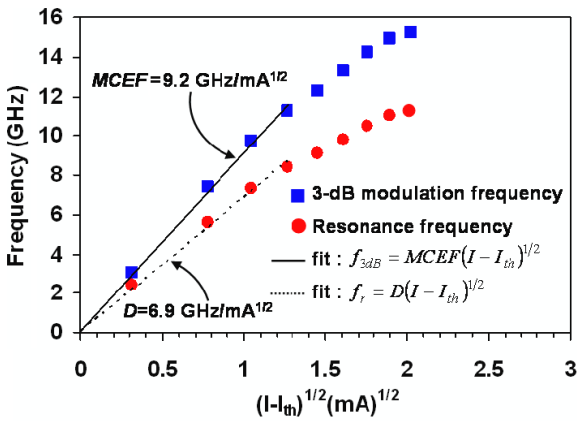

Figure 3. 3 dB modulation (squares) and resonance (circles) frequencies as a function of the square root of the current above threshold for VCSELs with a 10 μm active diameter. Linear fits from which the MCEF and D-factor were obtained are also shown.

The maximum bandwidth did not increase with further bias. At smaller bias currents, the device exhibits smaller -3 dB modulation frequencies. Bias currents of $1.1I_{\text{th}}$ (1 mA), $2.2I_{\text{th}}$ (2 mA) and $3.9I_{\text{th}}$ (3.5 mA) yielded -3 dB bandwidths of 3 GHz, 9.7 GHz and 13.3 GHz, respectively. The modulation response curves in figure 2 also reveal that the resonance peaks flattened and broadened with increasing I due to the increase in damping phenomenon [22]. The low bias current densities, such as 6.4 kA cm^{-2} necessary for the 15.3 GHz bandwidth in the 10 μm active diameter device, should improve reliability as higher current densities increase the VCSEL's internal temperature and accelerate device degradation [15–17]. Previously published VCSEL modulation bandwidths of 16.3 [23] and 15.2 GHz [24] for oxide-confined devices, 14.5 GHz for an implanted device [25], 21.5 GHz for an oxide- and implant-confined device [4] and 22 GHz for a tapered oxide aperture [26] required bias current densities of 50, 27.8, 22.2, 30 and 46 kA cm^{-2}, respectively. However, at these high current densities, the reliability of VCSELs is limited since the failure rate of VCSELs is proportional to the bias current density squared [18]. More recently, devices reported in [21] demonstrated a modulation bandwidth of 20 GHz at a current density of 11 kA cm^{-2}.

In figure 3 the measured VCSEL's 3 dB modulation frequency as a function of the square root of the current above threshold is shown. At low bias currents, the modulation bandwidth increases in proportion to the square root of the current above threshold as expected from the conventional rate equation analysis. The modulation bandwidth increases steadily to 12.3 GHz when biased at $I \sim 3.3I_{\text{th}}$ (3 mA) for a 10 μm oxide aperture device and then begins to deviate from linearity at high bias currents due to the reduction of the gain and differential gain as a result of device self-heating as will be concluded later in this section.

The modulation current efficiency factor (MCEF), which is related to the fundamental device properties (internal quantum efficiency (η_i), modal volume (V_a), group velocity (v_g) and differential gain ($\mathrm{d}n/\mathrm{d}g$)), was determined from the slope of the 3 dB frequency versus $(I - I_{\text{th}})^{1/2}$ (solid line in figure 3) MCEF $= f_{3\text{dB}}/(I - I_{\text{th}})^{1/2}$. The 10 μm active diameter device displayed a MCEF of 9.2 GHz mA$^{-1/2}$. Larger devices resulted in lower MCEF, where 12 μm and 14 μm active diameter devices exhibited MCEFs of 6.5 and 5.4 GHz mA$^{-1/2}$, respectively.

In order to determine which mechanism causes the modulation bandwidth to saturate with further bias ($I > 5$ mA) as shown in figure 3, the resonance frequency (f_r), parasitic roll-off frequency (f_r) and damping rate (γ) were extracted at each bias point by fitting the three-pole transfer function approximation to the measured modulation response [22]:

$$H(f) = \frac{f_r^2}{f_r^2 - f^2 + j\gamma(f/2\pi)} \cdot \frac{1}{1 + j(f/f_p)}. \qquad (1)$$

The first part of equation (1) can be directly derived by small-signal analysis of the rate equations above threshold, yielding a two-parameter modulation transfer function characterized by f_r and γ. The second part of equation (1) models the electrical chip parasitics by a single parasitic pole. The advantage of this procedure, compared to other techniques like the subtraction method [27], is that parasitics are allowed to vary over bias in this model which is the case in VCSELs. This allows us to estimate the effect of the three different frequency response limiting mechanisms previously reported in a VCSEL [7, 9, 18, 21]: the thermal saturation of the resonance frequency ($f_{\text{3dB,thermal}}$), the intrinsic damping of the resonance peak ($f_{\text{3dB,intrinsic}}$) and the parasitic-like roll-off ($f_{\text{3dB,parasitics}}$). This is carried out by calculating the corresponding 3 dB frequency limits that each of these mechanisms will impose on the modulation bandwidth in the absence of the other two [22, 28]:

The damping rate is proportional to the square of the resonance frequency [18]:

$$\gamma = Kf_r^2 + \gamma_o, \qquad (2)$$

where γ_o is the damping coefficient offset. The relation expressed in equation (2) assumes that the photon lifetime (τ_p), transport factor (χ), gain compression factor (ε), v_g and $\mathrm{d}n/\mathrm{d}g$ are all independent of bias current. The K-factor in equation (2), which determines the maximum 3 dB intrinsic modulation bandwidth set by damping in the absence of thermal and parasitic limitations as expressed by equation (3) [22], is found from the slope of the damping rate plotted against the resonance frequency squared [22] at several bias currents as shown in figure 4:

$$f_{\text{3dB,intrinsic}} = (2\pi\sqrt{2})/K. \qquad (3)$$

This yields a K-factor of $K = 0.21$ ns which in conjunction with a damping coefficient offset at a zero resonance frequency intercept of $\gamma_{\text{o}} = 13$ ns corresponds to an intrinsic bandwidth limit of $f_{\text{3dB,intrinsic}} = 42.3$ GHz (equation (3)). Deviations from expected linearity at low resonance frequencies (i.e. low bias) might be due to the increasing fraction of spontaneous emission into the lasing modes.

The thermal limit to the 3 dB modulation bandwidth is calculated by plotting the extracted values of the resonance frequency against the square root of the bias current above

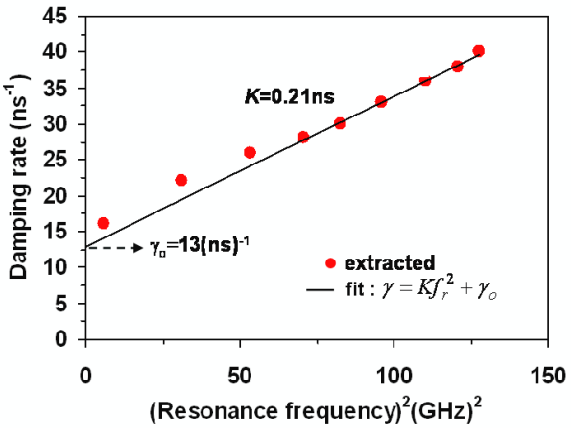

Figure 4. Damping rate as a function of the resonance frequency squared for a 10 μm active diameter device at different bias currents. Also shown is a linear fit to damping rate data from which the *K*-factor is realized.

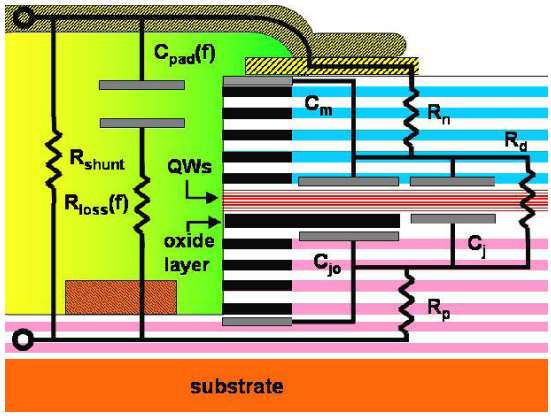

Figure 5. Schematic cross-section of fabricated oxide-confined VCSEL with superimposed equivalent circuit.

threshold as illustrated in figure 4, where due to thermal effects, a clear saturation of the resonance frequency with further bias is observed and reaches a maximum value of $f_{r,\max} = 11.3$ GHz. With no damping and parasitics, the thermally limited modulation bandwidth is given by equation (4) and corresponds to a maximum thermal 3 dB bandwidth limit of $f_{3\text{dB,thermal}} = 17.6$ GHz [22, 29]:

$$f_{3\text{dB,thermal}} = \sqrt{1+\sqrt{2}}\, f_{r,\max}. \tag{4}$$

The maximum extracted parasitic bandwidth limit ($f_{3\text{dB,parasitic}} = f_{p,\max}$) was found to be 21.5 GHz, which is larger than the calculated electrical *RC*-limited bandwidth of 13.5 GHz obtained from equivalent circuit analysis as described in section 4, since the intrinsic resonance improves the response at high frequencies. Consequently, a comparison between $f_{3\text{dB,thermal}} = 17.6$ GHz, $f_{3\text{dB,intrnsic}} = 42.3$ GHz and $f_{3\text{dB,parasitic}} = 21.5$ GHz demonstrates that the thermal effects represent the major limitation to the device bandwidth. The combined effect resulted in a maximum measured 3 dB modulation bandwidth of 15.3 GHz.

It is believed that the current devices' performance is thermally limited due to the devices' poor heat sinking as a result of using polyimide for mesa wrapping, which has a thermal conductivity of 0.002 W cm^{-1} K^{-1} [30]. Wrapping mesas with plated copper, which has a thermal conductivity of 4.01 W cm^{-1} K^{-1}, should improve device heat sinking. Furthermore, using the self-aligned process reported in [31] allows smaller mesa diameters for a given aperture size, thus decreasing mesa parasitic capacitance as well as the distance for heat to flow to the sidewall heat sink. This is expected to improve both the thermal and parasitic limits to the device performance which should lead to VCSELs with bandwidths greater than 21.5 GHz.

Finally, the rate at which f_r increases with I above I_{th} is quantified by the *D*-factor, which is associated with device properties (η_i, V_a, v_g, dn/dg and χ), and equals the slope of f_r versus $(I - I_{\text{th}})^{1/2}$ (dashed line in figure 3). The 10 μm active diameter devices displayed a *D*-factor of 6.9 GHz mA$^{-1/2}$. Devices with 12 μm and 14 μm active diameters exhibited *D*-factors of 4.6 and 3.8 GHz mA$^{-1/2}$, respectively.

4. Equivalent circuit analysis and parameter extraction

As the secondary bandwidth limitation that keeps the current devices from reaching their estimated intrinsic response limit is due to the electrical parasitic circuit elements, it is appropriate in this paper to present an equivalent circuit model for the VCSEL structure shown in figure 1. The model consists of the parasitic circuit elements associated with the physical features of the VCSEL structure that impede the modulated signal from reaching the VCSEL active area at high frequency and thus limiting its modulation bandwidth. The equivalent circuit allows us to investigate the relative influence of each parasitic parameter by itself on the device performance and aids in the design of impedance-matching circuits. Figure 5 shows a schematic cross-section of the fabricated oxide-confined VCSEL with a superimposed equivalent circuit. This model included the following parameters: $C_{\text{pad}}(f)$ denotes the pad capacitance between the metal pad on the polyimide and the bottom p-mirror stack; $R_{\text{loss}}(f)$ represents the polyimide dielectric losses; R_{shunt} characterizes the resistance of the dielectric material at dc or low frequency due to the leakage current in the pad capacitor, which is usually on the order of multi-giga ohms and was assumed to be so large that it had a negligible effect on the model; a parallel combination of a capacitance C_j and a resistance R_d represents the active region; C_{jo} and C_m represent the mesa regions with single and multiple oxidized layers, respectively; and R_n and R_p correspond to the upper n-type and lower p-type mirror resistance along with the top and bottom contact resistance, respectively.

The calculated reflection coefficient $S_{11\text{cal}}(f)$ of the circuit model driven from a VNA with an output impedance of $Z_{\text{VNA}} = 50\ \Omega$ and the total impedance $Z_T(f)$ are expressed as

$$S_{11\text{cal}}(f) = \frac{Z_T(f) - Z_{\text{VNA}}}{Z_T(f) + Z_{\text{VNA}}} \tag{5}$$

$$Z_T(f) = \frac{Z_m(f) Z_p(f)}{Z_m(f) + Z_p(f)}. \tag{6}$$

Table 1. Extracted and calculated values of C_T and C_p at zero bias current and low frequency.

	Equivalent circuit parasitic capacitance (fF)						
	Calculated					Extracted	
Mesa/active area diameter (μm)	C_j	C_{jo}	C_m	C_T[a]	C_p[b]	C_T	C_p
31/10	53.3	133.7	5.7	192.9	69.4	170.6	74.8
33/12	76.7	148.9	5.9	231.5	69.4	210.5	73.3
35/14	104.4	165.5	6.4	276.3	69.4	244.1	76.4

[a] $C_T = C_j + C_{jo} + C_m$.
[b] All devices have the same contact pad.

The mesa impedance $Z_m(f)$ and pad impedance $Z_p(f)$ are

$$Z_m(f) = R_m + (1/R_d + \mathrm{j}2\pi f C_T)^{-1} \quad (7)$$

$$Z_p(f) = R_{\mathrm{loss}}(f) + (\mathrm{j}2\pi f C_{\mathrm{pad}}(f))^{-1}, \quad (8)$$

where R_m, C_T, $R_{\mathrm{loss}}(f)$ and $C_{\mathrm{pad}}(f)$ represent mirror total series resistance ($R_n + R_p$), combined mesa capacitance ($C_j + C_{jo} + C_m$), polyimide dielectric loss and pad capacitance, respectively.

In previously reported VCSEL circuit models used for parasitic parameter extraction [14, 18, 32], the frequency dependence of the material dielectric permittivity (ε_r) and R_{loss} was ignored, and thus fixed values for C_{pad} and R_{loss} were used. Based on a study reported by the author and collaborators in [33], the functional dependence of ε_r and R_{loss} on frequency, which was approximated by a Gaussian function with fitting parameters, is included in the model presented here:

$$C_{\mathrm{pad}}(f) = C_p \varepsilon_r(f) \quad (9)$$

$$\varepsilon_r(f) = (1 - \varepsilon_\infty/\varepsilon_{\mathrm{LF}}) \cdot \mathrm{e}^{-\left(\frac{f^2}{f_o^2}\right)} + \varepsilon_\infty/\varepsilon_{\mathrm{LF}} \quad (10)$$

$$R_{\mathrm{loss}}(f) = R_{\mathrm{LF}} \cdot \mathrm{e}^{-\left(\frac{f^2}{f_1^2}\right)}, \quad (11)$$

where $C_p = \varepsilon_o \varepsilon_{\mathrm{LF}} A_p/d$ is the pad capacitance at low frequency, ε_{o} is the free space permittivity (8.85×10^{-14} F cm^{-1}), A_p is the pad capacitor area, d is the polyimide thickness, $\varepsilon_{\mathrm{LF}}$ is the polyimide dielectric constant at low frequency (3.9), f is the operating frequency, ε_∞ is the polyimide dielectric constant at high frequency (2.7), R_{LF} is the resistance associated with the dielectric loss at low frequency, and f_o and f_1 are fitting parameters (103 GHz, 75 GHz).

The pad capacitance C_p and combined mesa capacitance C_T values were estimated from simple geometrical considerations illustrated in figure 5. All the three different device sizes have similar pads with an area of ~11,055 μm^2 and a polyimide planarization layer thickness of 5.5 μm with a relative permittivity of $\varepsilon_{\mathrm{LF}} = 3.9$ (provided by the vendor at 1 kHz) which resulted in a calculated pad capacitance of $C_p =$ 69.4 fF. In a similar way, the total mesa capacitance for 10 μm, 12 μm and 14 μm active diameter VCSELs was estimated at zero bias to be 192.9 fF, 231.5 fF and 276.3 fF, respectively.

The genetic algorithm (GA), which is an excellent search procedure for finding a best fit inspired by population genetics [34], was utilized to extract the measured values of the equivalent circuit elements (C_p, R_{LF}, C_T, R_d and R_m) for different device sizes by fitting both the real and the imaginary parts of the calculated $S_{11\mathrm{cal}}(f)$ using equation (5) to those of the measured $S_{11\mathrm{meas}}(f)$ data at several bias currents. Computationally, the implementation of a typical GA is reported in [34]. Figure 6 shows measured and fitted S_{11} data for 10 μm and 14 μm oxide aperture VCSELs at bias currents of 5 mA and 12 mA, respectively. Measured and fitted data at other bias currents and for the 12 μm devices were omitted for clarity. The convergence of the fitting values to reasonable values was enhanced by assigning a range of initial values for R_m, R_{LF}, C_p, C_T and R_d based on either previously reported values for similar structure and size or estimations from simple geometrical considerations [14, 18, 31, 32]. Finally, all the circuit parameters were allowed to vary about these values to minimize the error. The resulting extracted values of C_T and C_p along with the calculated values of C_j, C_{jo}, C_m, C_T and C_p at low bias and low frequency, which are listed table 1, are in good agreement. The difference between estimated and extracted values may be due to uncertainty in the oxide aperture diameter, error in the oxide dielectric constant and thickness, and neglecting the junction depletion capacitance and the narrow depletion region below the thin oxide aperture. The deduced values of R_m at all bias currents were 42 Ω, 35 Ω and 30 Ω for 10 μm, 12 μm and 14 μm oxide aperture VCSELs, respectively. An average value of 5 Ω was extracted for R_{LF} for all device sizes at all bias currents.

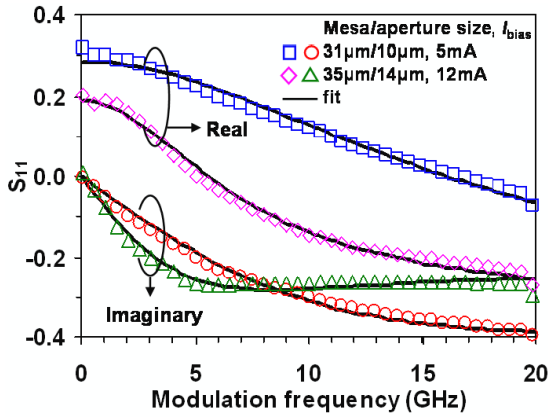

Figure 6. Measured (points) and fitted (solid line) S_{11} data for 10 μm and 14 μm oxide aperture VCSELs at bias currents of 5 mA and 12 mA respectively.

As mentioned earlier, C_T represents the total capacitance of the active region C_j and the mesa regions with single and multiple oxidized layers C_{jo} and C_m, respectively.

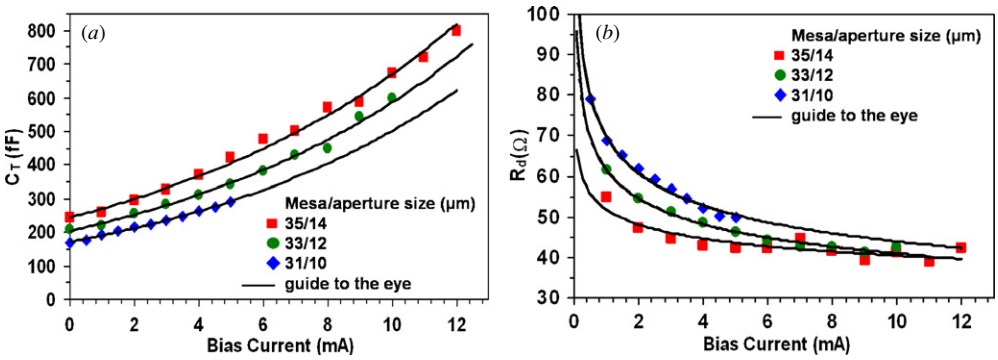

Figure 7. (*a*) Extracted values (points) of (*a*) the total mesa capacitance and (*b*) the active region resistance at different bias currents for different device sizes. Solid lines are guide to the eye.

The extracted values of C_T for different device sizes at different bias currents are shown in figure 7(*a*), where the total capacitance increases with size and drive current. The active region capacitance C_j represents depletion and diffusion capacitances C_{dep} and C_{dif}, respectively. The depletion capacitance dominates C_j only at small bias and is approximated by a parallel plate capacitor. Thus, the calculated values of C_j listed in table 1 at low bias represent C_{dep} where the diffusion capacitance was not included. At strong bias, the diffusion capacitance associated with charge storage dominates and increases with bias as demonstrated by the extracted values in figure 7(*a*). In figure 7(*b*), the extracted values of R_d for different device sizes at different bias currents are shown. The active region resistance decreases as the bias current increases. The observed decrease in the VCSEL's active region resistance provides better impedance matching to an ordinary 50 Ω source. Such a decrease in R_d agrees well with the theory and is justified as follows. The active region resistance is a combination of a dc resistance (R_{dc}) and diffusion or ac resistance (R_{dif}). R_{dc} is constant at bias currents above threshold, while R_{dif} depends on bias current ($\sim$26 mV/I_{bias}).

Finally, open-circuit time constant circuit analysis was used to calculate the electrical *RC*-limited bandwidth, $f_{\text{3dB,RC}} = (2\pi(\tau_T + \tau_p))^{-1}$, where $\tau_T = C_T[R_d \| (R_m + Z_{\text{VNA}})]$ which is the time constant associated with the C_T and $\tau_p = C_p[R_{\text{loss}} + ((R_m + R_d) \| Z_{\text{VNA}})]$ which is the time constant associated with C_p. For a 10 μm active diameter device biased at 5 mA, the extracted values of C_T, C_p, R_{loss}, R_m and R_d were 292 fF, 68 fF, 3.5 Ω, 42 Ω and 50 Ω, respectively, and resulted in a maximum parasitic bandwidth limit of $f_{\text{3dB,RC}} =$ 13.5 GHz, which is lower than the extracted $f_{\text{3dB,parasitic}} =$ 21.5 GHz obtained by fitting the three-pole transfer function to the measured S_{21} as described and discussed in section 3.

5. Summary and conclusion

We have fabricated and characterized high-speed oxide-confined 850 nm VCSELs that demonstrate excellent performance. The modulation bandwidth of VCSELs with typical size pads is as high as 15.3 GHz at a low current density of 6.4 kA cm^{-2}, which is 36% less than the industrial current density benchmark for reliability (10 kA cm^{-2}). An investigation of the analog modulation characteristics of oxide-confined 850 nm VCSELs showed that thermal effects impose a major limitation followed by parasitic effects. Both effects combined prevent presented devices from reaching their estimated potential intrinsic bandwidth limit of 42.3 GHz. The implementation of genetic algorithm resulted in good agreement between calculated and extracted parasitic circuit element values. Future incorporation of techniques reported in [10, 31] to reduce the parasitic capacitance, in [11, 12] to suppress the higher order transverse modes, and in [19–21, 31] to reduce the thermal resistance, as well as the optimization of heterostructure designs for high gain and differential gain, directly modulated 40 Gb s^{-1} VCSELs should be realized.

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