Low Thermal Resistance, High Speed, Top Emitting 980nm VCSELs

A. N. AL-Omari, *Member, IEEE*, G. P. Carey , S. Hallstein, J. P. Watson, G. Dang, and K. L. Lear, *Member, IEEE*

***Abstract*— Increasing copper plated heatsink radii from 0 to 4 μm greater than the mesa in vertical-cavity surface emitting lasers (VCSELs) reduced the measured thermal resistance for a range of device sizes to values 50% lower than previously reported over a range of device sizes.. For a 9 μm diameter oxide aperture the larger heatsink increases output power and bandwidth by 131% and 40% respectively. The lasers exhibit a 3-dB modulation frequency bandwidth up to 9.8 GHz at 10.5 kA/cm^2. The functional dependence of thermal resistance on oxide aperture diameter indicates the importance of lateral heat flow to mesa sidewalls.**

***Index Terms*—Semiconductor laser diodes, heatsinks, thermal management, modulation bandwidth, 3-dB frequency, VCSEL**

I. INTRODUCTION

HIGHER MODULATION bandwidth vertical cavity surface emitting lasers (VCSELs) are important components for increasing the bit rate of low cost data communications systems. In addition to electrical parasitic circuit effects and intrinsic laser dynamics, thermal effects can also saturate VCSEL modulation bandwidth at the high bias currents required for higher speeds [1]. More effective heatsinking approaches are required to diminish thermally induced bandwidth saturation in VCSELs which typically exhibit high thermal impedances. The authors' prior work [2] used evaporated Au and plated Cu heatsinks to reduce the thermal impedance of 10 μm diameter oxide aperture, top-emitting, 850 nm devices to 2.0 °C/mW and accordingly increase the bandwidth by up to 12% compared to separately fabricated samples without metal heatsinks. This paper reports a better controlled experiment using varying sizes of plated Cu heatsinks yielding much lower thermal impedances. For example the thermal impedance of a 9-μm diameter oxide aperture, top-emitting, 980 nm VCSEL was reduced to 1.0 °C/mW resulting in a 40% bandwidth increases.

II. FABRICATION

Top-emitting, high-speed, 980 nm VCSELs were fabricated from a metal–organic chemical vapor deposition (MOCVD) grown AlGaAs structure on an *n*-type substrate. The active region contains three 80 Å InGaAs quantum wells centered on the anti-node of the 1-λ cavity with $GaAs_{0.955}P_{0.045}$ used for strain-balancing as 100 Å barriers between the wells and for the spacer material before and after the wells. The p-mirror above the active region employs a 17 period, C-doped $Al_{0.08}Ga_{0.92}As/Al_{0.95}Ga_{0.05}As$ distributed Bragg reflector (DBR) except for a single low index ~λ/4 layer adjacent to the cavity with 98% Al content. The p-DBR was terminated with a phase matching GaAs p^{++} ($2x10^{20}cm^{-3}$) contact layer. The 37 period n-mirror below the active region is Si-doped.

Oxide-confined VCSELs with coplanar wave-guide probe pads on polyimide were fabricated using a six photomask process sequence. First, a 4 μm deep etch in a Trion inductively coupled plasma system defined cylindrical mesas 20 to 36 μm in diameter. The etch was terminated at the 4th mirror pair below the active region as determined with an in-situ laser reflectometer. Next, the 15 mm x 15 mm sample was wet-oxidized in a 6 cm diameter, 380 °C quartz tube furnace with 30 sccm of N_2 and 90°C water steam for 8 minutes to form oxide apertures. The $Al_{0.98}Ga_{0.02}As$ layer oxidation rate was ~1.0μm/minute resulting in the oxide extending in 8.5 μm from the mesa sidewall yielding oxide aperture diameters from 3 to 19 μm depending on mesa size. After oxidation, annular *p*-type contacts of Ti-Au (200 /1500) Å were evaporated on top of the mesas after removing the surface oxide using HF-H_2O (1:10) solution. Immediately before depositing the bottom *n*-type contact, the sample was soaked in HCl-H_2O (1:1) solution to remove any $Al_{0.95}Ga_{0.05}As$ or oxide layer formed on the $Al_{0.08}Ga_{0.92}As$ surface in the contact region. AuGe(pre-alloyed)-Ni-Au with thicknesses of (1000/300/500) Å were evaporated onto the partially etched bottom mirror to form the *n*-type contact which is electrically connected to the substrate. Contacts were alloyed for 30 seconds at 440 °C.

After contact formation, 1000 Å of PECVD SiN_x was deposited to electrically insulate all the mesa sidewalls from metal heatsinks. Vias in the SiN_x were etched for the top and bottom metal contacts. Photosensitive positive tone polyimide was spun on the sample for planarization and lithographically patterned to remove the polyimide everywhere except under the bond/probe pads and the interconnect bridge to the p-type contact to reduce pad capacitance [3]. Subsequent curing at 350 °C for 30 minutes in N_2 resulted in a polyimide thickness of 5 μm. The final processing step was to form electroplated Cu heatsinks of varying outer diameters over the mesas along with probe pads on the neighboring polyimide covered regions. The use of Cu rather than Au was motivated by cost and thermal conductivity [2]. After depositing a seed layer of Ti-Au with thicknesses of (200/800) Å on the entire sample, photoresist was patterned to define open areas for

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A.N.AL-Omari and K.L.Lear are with the Electrical and Computer Engineering Department, Colorado State University, Fort Collins, CO 80523 USA, (e-mail: ahmad@engr.colostate.edu, kllear@engr.colostate.edu)

G. P. Carey, S. Hallstein, and J.P. Watson, are with Novalux, Inc. Sunnyvale, CA 94086 USA.

G. Dang is with U.S. Army Research Laboratory, Adelphi, MD 20783 USA.

electroplating. Approximately 2 µm of Cu was plated directly on the seed layer in a Cu bath at room temperature and a current density of J~18 kA/cm^2. After stripping the photoresist, the seed layer was removed by etching back the Au and Ti using a commercial Au-etchant and buffered HF respectively. Annular plated heatsinks with an outer radii of 0, 2, and 4 µm greater than the mesa diameter, referred to as the heatsink overlap, were plated in adjacent positions (separated by 250µm) on the sample. Heatsinks with zero overlap did not cover the mesa sidewalls as shown for a completed device in Fig. 1(a), while ones with non-zero overlap covered the sidewall and a portion of the lower mirror surrounding the mesa as shown in Fig. 1(b). The inset in Fig. 1 shows a top view of the device structure including coplanar waveguide probe pads. Fig. 2. shows a cross-section along AA' of Fig. 1 (b).

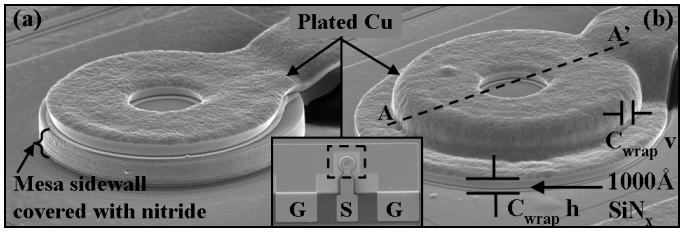

Fig. 1. SEM photograph of a 26-µm mesa diameter electroplated with ~2µm thick copper with (a) 0 µm and (b) 4 µm overlap. The inset shows a top view of the device structure including coplanar waveguide probe pads.

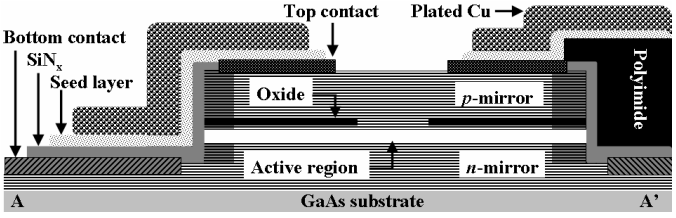

Fig. 2. A cross-section along AA' of Fig. 1 (b).

III. MEASUREMENTS AND DISCUSSION

Room temperature DC characterization of completed VCSELs with varying heatsink overlaps for oxide aperture diameters from 7 to 15 µm showed that increased heatsink overlap significantly reduces thermal resistance (R_{th}) and increases maximum output power for all sizes. Fig. 3 compares the continuous-wave (CW) light output vs. current (*L-I*) and voltage (V) characteristics of two VCSELs with heatsink overlaps of 0 and 4 µm, where both had identical mesa and oxide aperture diameters of 26 and 9 µm, respectively. The I-V characteristics of the two devices are essentially identical, indicating a minimal thermal impact on the 72Ω series resistance. To our knowledge, the 131% increase in the maximum power output is the highest ever reported as a result of improved heatsinking. Previous publications presented improvements in VCSEL maximum output power of 60% accomplished by plating 8.5µm of Au on the 120x120µm^2 pads around 8µm pillars [4] and 107% by attaching 20µm diameter VCSELs to a Cu substrate after

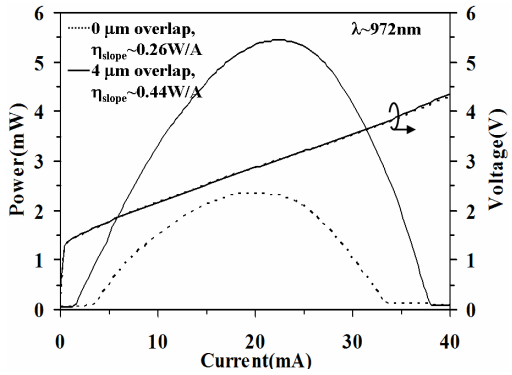

Fig.3. CW *L-I* and voltage characteristics for a 26-µm mesa diameter VCSEL with a 9-µm of oxide-aperture diameter.

GaAs substrate removal resulting in a 20% reduction in R_{th} [5]. The observed dependence of R_{th} on device size with and without sidewall heatsinking further illuminates the role of lateral heat flow in VCSELs. Using $\delta\lambda/\delta T \approx 0.07nm/K$ [6], R_{th} of the devices was determined by measuring the wavelength dependence of the laser spectra as a function of the electrical input power [4] for a range of device diameters. Fig. 4 shows R_{th} as a function of the active diameter. Extension of the heatsink over the mesa reduces R_{th} by approximately 20% for a range of device sizes, comparable to the more complex process in [5]. For active diameters greater than 7 µm, the Cu plated heatsinks with 2 µm overlap gave a 50% reduction in R_{th} compared to the best known previously published results. Fig. 4 also summarizes other reported R_{th} of VCSELs that were fabricated using various techniques [2, 5] and shows the amount of improvement achieved in lowering the devices R_{th}.

The measured size dependence of R_{th} with and without overlap approximately follows the simple analytical estimation $R_{th}=1/(2\xi d)$ [6] for heat spreading from a uniform temperature disc on a homogenous, isotropic, semi-infinite substrate where d is the active diameter and ξ is the substrate thermal conductivity. Although the sample structure is significantly more complicated than the idealized disc geometry, the good fit motivates parameterization using ξ to allow comparison of various sized devices. Using a best fit to our data, we obtainξ =0.41 and 0.53 W/cm.K for 0 and 2µm of Cu-plated overlap respectively. The difference in the effective thermal conductivities indicates sidewall heatsinks increase lateral heat

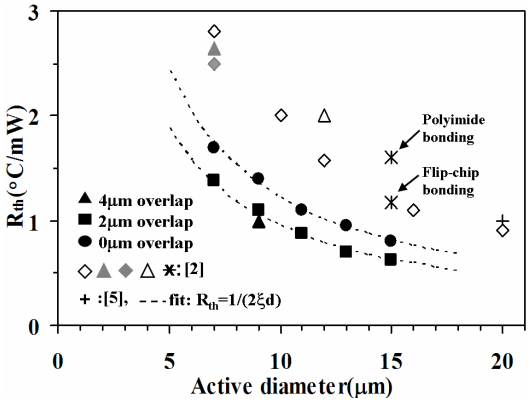

Fig. 4. VCSEL's thermal resistance as a function of the active diameter.

flow since the thermal resistance of the VCSEL mirror stacks is anisotropic [7]. Thus with sufficient heatsink overlap on the substrate and sidewall heatsinking, more heat flows laterally though the mirrors to the Cu-plated sidewalls and from there into the substrate via the heatsink overlap rather than going through the bottom mirror to the substrate.

In addition to the improvement in DC and thermal properties, the increased heatsink overlap also significantly improves VCSEL bandwidth. Frequency response was measured on wafer using the same apparatus described in [2]. As shown in Fig. 5, 9-μm lasers with 4μm heatsink overlaps exhibit 9.8-GHz maximum 3-dB bandwidths when biased at I_b=6.7 mA. The 4μm overlap increased the 3-dB bandwidths by 40% in comparison to zero overlap heatsinks. The increase in bandwidth due to sidewall heatsinking for the 980 lasers reported here is much larger than a previously reported 12% increase in the 3-dB bandwidths for similar λ=850 nm devices with and without Cu-heatsinks [2]. The Cu-plating in that case is believed to have suffered from quality, density and adhesion issues. Since higher current densities increase the internal temperature of the devices and otherwise accelerate device degradation independent of junction temperature, the low bias current densities, such as 10.5 kA/cm^2 necessary for the 9.8-GHz bandwidth in the 9-μm diameter device, should improve device reliability [8]. Previously published VCSEL modulation bandwidths of 8.5 [9] and 9.75GHz [10] required bias current densities of 10.5 and 20 kA/cm^2 respectively.

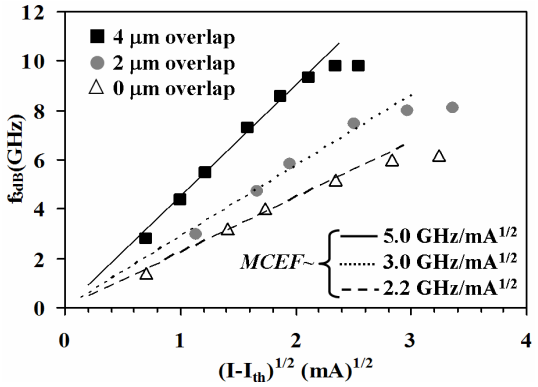

Fig.5. VCSEL 3-dB modulation frequency as a function of the square root of the current above threshold.

In Fig. 5 the bandwidth increases as expected with bias current up to a limit where it saturates. The solid and dashed lines are theoretical fits using $f_{3dB}=(MCEF)(I-I_{th})^{1/2}$, where MCEF is the modulation current efficiency factor. The trend of higher MCEF with larger overlap was expected due to the increased photon density, gain, and differential gain at lower junction temperatures, but the factors affecting the saturated bandwidth are less clear. Non-zero heatsink overlaps result in an additional parasitic capacitance between the heatsink and lower mirror that adds to the total pad capacitance. The horizontal and vertical parasitic capacitance ($C_{wrap\,h}$, $C_{wrap\,v}$) for a 9-μm active diameter Cu-plated device shown in Fig. 1(b) were estimated to be ~224 fF and ~16 fF based on geometrical calculations with the 1000 Å nitride layer serving as the dielectric. PSpice simulations, which also include a ~22fF parasitic pad capacitance, indicate purely electrical circuit effects would allow a maximum f_{3dB} of 12.4 GHz for the 4μm overlap. Smaller overlaps and corresponding lower capacitance would give higher electrical bandwidths in a trend opposite to the measured bandwidth, indicating the devices are not electrical bandwidth limited. Thus the bandwidth saturation is attributed to thermal effects perhaps combined with gain partitioning between modes to be examined in further detail in the future. The optimum overlap will balance the tradeoff in capacitance and thermal impact on overall bandwidth.

IV. CONCLUSIONS

Variation in the outer diameter of Cu-plated heatsinks is seen to have a major effect on thermal impedance and thus temperature dependent DC and AC properties of top-emitting VCSELs. Lasers of this type with the lowest published thermal resistances to date have been developed using wafer-scalable processes that do not require soldering to external heatsinks or other hybrid processes. It appears that the application of these Cu-plated heatsinks to epitaxial structures designed to provide higher MCEF and prolonged single mode operation should enable significantly higher bandwidths than those demonstrated in this work and potentially higher than any previously demonstrated in VCSELs.

ACKNOWLEDGMENT

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