

VCSELs With a Self-Aligned Contact and Copper-Plated Heatsink

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Abstract—Top-emitting, 850-nm vertical-cavity surface-emitting lasers with a self-aligned top contact and evaporated gold or plated copper heatsink were fabricated and characterized. Thermal resistance was reduced by 44%, and output power and bandwidth were increased by 38% and 12%, respectively. The fabricated devices exhibit a 3-dB modulation frequency bandwidth up to 16.3 GHz at 10 kA/cm².

Index Terms—Au, Cu, modulation bandwidth, parasitic capacitance, semiconductor lasers, thermal management, three-decibel (3-dB) frequency, vertical-cavity surface-emitting lasers (VCSELs).

I. INTRODUCTION

AS THE bit rates of high-speed data transmission systems increase, the direct modulation bandwidth of vertical-cavity surface-emitting lasers (VCSELs) is becoming a significant constraint. VCSELs exhibit large thermal impedances due to their small sizes and poor thermal conductivity of the distributed Bragg reflectors (DBRs) [1]–[3]. The resultant high junction temperature is one of the factors that currently limit the frequency response of VCSEL technology. Such a temperature rise diminishes both the gain and differential gain leading to lower resonance frequencies and is believed to be a significant contribution to the modulation bandwidth saturation. There have been a number of studies on the benefit of improved heat-sinking for VCSELs [4]. Most have focused on achieving higher output powers but have not examined the benefits of better thermal management for VCSEL modulation bandwidth which is examined in this letter.

II. FABRICATION

Top-emitting self-aligned high-speed 850-nm VCSELs were fabricated from a metal–organic chemical vapor deposition grown AlGaAs structure on a p-type substrate [5]. Details about the epitaxial structure are presented in [1]. Device fabrication began with the formation of an annular n-type contact by evaporating Pd–Ge–Ti–Pt with thicknesses of (500/1000/250/300) Å. The contact and a smaller diameter photoresist feature protecting the aperture served as an etch mask for cylindrical mesas. The contact outer diameter, and thus mesa diameter, is 18–28 μm. The contact has a 4-μm width giving contact aperture sizes of 10–20 μm. Mesas were etched to a depth

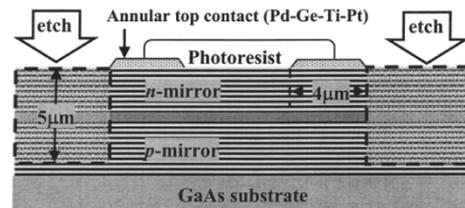


Fig. 1. Contact and a smaller diameter photoresist feature protecting the aperture served as an etch mask for cylindrical mesas.

of 5 μm, stopping in the bottom mirror, using a load-locked Trion inductively coupled plasma dry-etching system. As shown in Fig. 1, the use of the contact to define the outer perimeter of the mesa etch mask results in a device mesa that is self-aligned to the contact. The self-aligned process allows smaller mesa diameters for a given aperture size, thus decreasing mesa capacitance as well as the distance for heat to flow to the sidewall heatsink. To form the current aperture and provide lateral index guiding to the lasing mode the sample was wet-oxidized in a 380 °C steam environment for 20 min. The oxidation rate was ~0.2 μm/min for the Al_{0.98}Ga_{0.02}As layer resulting in the oxide extending in 4 μm from the mesa sidewall. After lithography for the bottom p-type contact, the sample was soaked for 15 s in a HCl–H₂O (1 : 1) solution to remove any Al_{0.92}Ga_{0.08}As surface or any oxide layer formed on the Al_{0.16}Ga_{0.84}As surface. BeAu(pre-alloyed)-Ti–Au with thicknesses of (500/300/700) Å were then evaporated onto the partially etched bottom mirror to form the contact to the p-type substrate. Contacts were alloyed for 30 s at 420 °C. After contact formation, 200 nm of silicon nitride (Si₃N₄) was deposited using plasma-enhanced chemical vapor deposition to electrically insulate the mesa sidewall from later metallic coatings. Vias in the Si₃N₄ were etched for the top and bottom metal contacts. A photosensitive polyimide was spun on the sample for planarization and lithographically patterned to remove the polyimide everywhere except under the bond/probe pads and the interconnect bridge to the n-type contact. Subsequent curing at 350 °C for 30 min in a nitrogen atmosphere resulted in a polyimide thickness of 5.5 μm. Polyimide planarization lowers interconnect and pad capacitance beyond that obtained with conventional oxide or nitride passivation since it has a lower dielectric constant and readily allows much thicker layers [6].

The final processing steps were varied to compare the thermal impact of three different structures. Ti–Au with thicknesses of (200/3000) Å were evaporated on the first sample including the mesa sidewall for a heatsink, metal interconnects, and coplanar waveguide probe/bond pads. A second sample was electroplated with ~2 μm of Cu after depositing a seed layer of Ti–Cu with thicknesses of (200/500) Å. The seed layer was removed by

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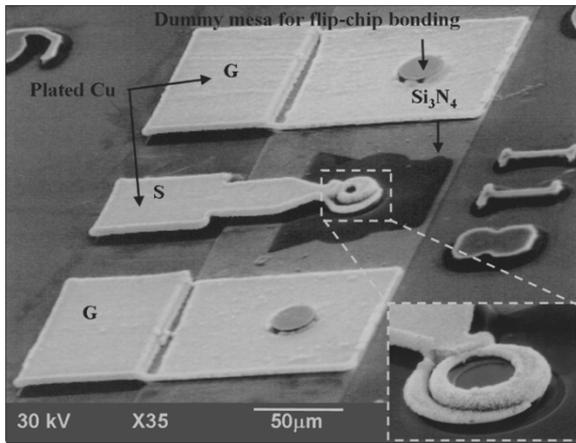


Fig. 2. SEM photograph of an 18- μm mesa diameter electroplated with copper.

etching back the Cu and Ti using a commercial Cu-etchant, Microtech 85, and buffered HF, respectively. Cu rather than Au plating was chosen due to copper's higher thermal conductivity ($4.01 \text{ W/cm} \cdot \text{K}$) and lower cost ($\sim \$24/\text{m}^2 \cdot \mu\text{m}$) compared to gold ($3.17 \text{ W/cm} \cdot \text{K}$, $\sim \$3520/\text{m}^2 \cdot \mu\text{m}$). Fig. 2 shows a scanning electron microscope (SEM) photograph of a high-speed Cu-plated VCSEL at the completion of fabrication with a magnified view of the mesa in the inset. A third baseline sample had been fabricated earlier with polyimide, which has a thermal conductivity of $0.002 \text{ W/cm} \cdot \text{K}$ [7], rather than metal, covering the mesa sidewall [1]. All of the devices were fabricated from material within 20 mm of the center of a single 75-mm diameter, epitaxial wafer.

III. MEASUREMENTS AND DISCUSSION

DC characteristics of completed VCSELs were measured using a probe station, an HP 4145A semiconductor parameter analyzer, and a silicon photodiode with a $10 \times 10 \text{ mm}^2$ active area and $\sim 0.6\text{-A/W}$ responsivity at $\lambda = 850 \text{ nm}$. Fig. 3 shows the continuous-wave (CW) light output–current (L – I) characteristics of Au-wrapped, Cu-plated, and polyimide-wrapped devices. The Au-wrapped and the Cu-plated heat spreading layers increase the output power at $10 \text{ mA} \approx 13I_{\text{th}}$ from 0.66 to 0.76 and 0.91 mW, respectively. VCSELs were all chosen to have the same size, 10- μm diameter, oxide apertures. Minimal device heating occurs at threshold, so the average threshold current densities of the samples are assumed to be the same. The observed $\pm 14\%$ variation in threshold current corresponds to a variation of $\pm 0.7 \mu\text{m}$ in diameter due to oxide aperture nonuniformity.

The samples with metal near the sidewalls showed reduced thermal resistance for a range of device diameters. Using $\delta\lambda/\delta T \approx 0.07 \text{ nm/K}$ [8], the thermal resistance (R_{th}) of the devices was determined by measuring the wavelength dependence of the laser spectra as a function of the electrical input power [4]. Fig. 4 shows the thermal resistance as a function of the active diameter. Au-wrapped and Cu-plated heat spreading layers reduce R_{th} by 25% and 44%, respectively, for a range of device sizes. A 20% reduction in R_{th} was previously reported [9] by attaching 20- μm -diameter VCSELs to a Cu substrate after GaAs substrate removal. The measured size dependence

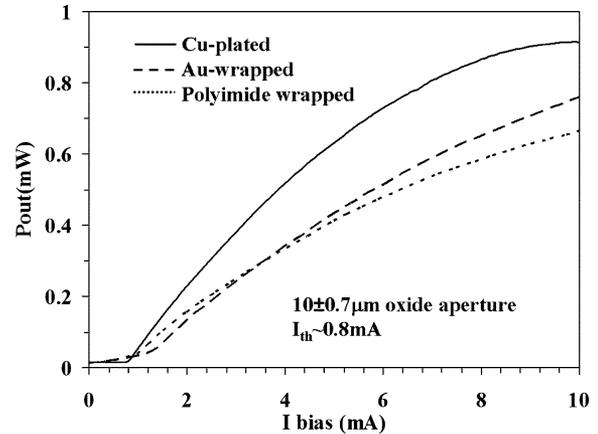


Fig. 3. CW L – I characteristics.

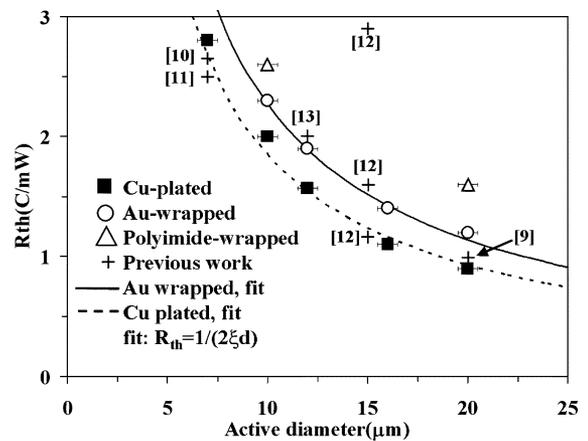


Fig. 4. VCSEL's thermal resistance as a function of the active diameter.

of thermal resistance approximately follows the simple analytical estimation $R_{\text{th}} = 1/(2\xi d)$ [8] for heat spreading from a uniform temperature disc on a homogenous isotropic semi-infinite substrate, where d is the active diameter and ξ is the substrate thermal conductivity. Although the sample structure is more complicated than the idealized disc geometry, the good fit motivates parameterization using ξ to allow comparison of various sized devices. Using a best fit to our data, we obtain $\xi = 0.22 \text{ W/cm} \cdot \text{K}$, $0.27 \text{ W/cm} \cdot \text{K}$, and $\sim 0.17 \text{ W/cm} \cdot \text{K}$ for Au-wrapped, Cu-plated, and polyimide-wrapped devices, respectively. As predicted, the DBR alloy scattering reduces ξ [8] compared to GaAs and AlAs which have $\xi = 0.45$ and $0.9 \text{ W/cm} \cdot \text{K}$. Fig. 4 also summarizes other reported thermal resistances of VCSELs that were fabricated using various techniques [9]–[13]. Improvements in the quality, density, and adhesion of the electroplated copper should result in further reduction in thermal resistance.

The ac measurement apparatus consisted of a probe station equipped with a room-temperature vacuum chuck and Cascade Microtech air coplanar probes, $\sim 2 \text{ m}$ of graded index multimode fiber, a high-speed Discovery Semiconductor DSC30S photodiode attached to a JSTD-02K200-40-10P MITEQ amplifier, an HP 4145 semiconductor parameter analyzer, and an Agilent 8722ET vector network analyzer with 40-GHz bandwidth. The system modulation response S_{21} was measured for VCSELs at various bias currents over a frequency range of 50 MHz to

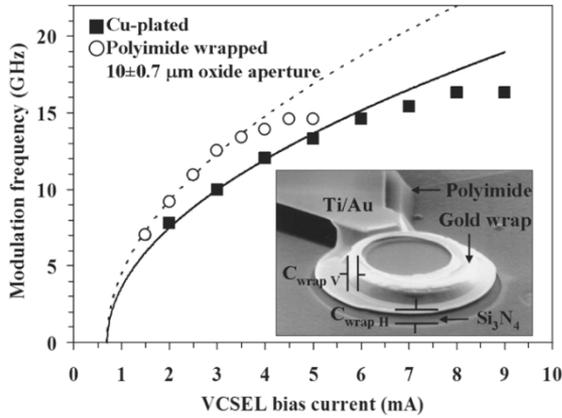


Fig. 5. VCSEL 3-dB modulation frequency at various bias currents.

40 GHz from which the 3-dB frequencies were obtained. As shown in Fig. 5, polyimide-wrapped and Cu-plated 10- μm diameter aperture lasers exhibit maximum 14.6- and 16.3-GHz 3-dB bandwidths when biased at 4.5 and 8 mA, respectively. Larger devices exhibit smaller 3-dB frequencies. The moderate bias current densities, such as $9.5 \pm 1.3 \text{ kA/cm}^2$ necessary for the 16.3-GHz bandwidth in the 10- μm -diameter device, should improve reliability [14]. Previously published VCSEL modulation bandwidths of 16.3 [15] and 15.2 GHz [16] for oxide-confined devices, 14.5 GHz for an implanted device [17], and 21 GHz for an oxide and implant confined device [18] required bias current densities of 50, 27.8, 22.2, and 30 kA/cm^2 , respectively.

It is apparent from Fig. 5 that as the bias current increases, the -3-dB modulation frequency also increases until a certain limit, and then the modulation frequency saturates. The solid line is a theoretical fit using $f_{3\text{dB}} = (\text{MCEF})(I - I_{\text{th}})^{1/2}$, where MCEF is the modulation current efficiency factor. The 3-dB bandwidth for polyimide-wrapped and Cu-plated devices saturates at $6I_{\text{th}}$ and $11I_{\text{th}}$, respectively. The best fit results in an MCEF of 8.2 and 7.0 $\text{GHz/mA}^{1/2}$ for the polyimide-wrapped and Cu-plated device, respectively. The lower MCEF of the Cu-plated device was unexpected and is under further investigation. An even higher thermally limited 3-dB bandwidth would be expected from the lower thermal resistance Cu-plated device if its MCEF were increased and capacitance is reduced.

Due to the overlap of the wrapped Au and plated Cu which extends to about 6 μm around the mesa, a new parasitic capacitance that adds to the total pad capacitance exists. The combined horizontal and vertical parasitic capacitance ($C_{\text{wrap } h}$, $C_{\text{wrap } v}$) for a 10- μm active diameter Au-wrapped device shown in the inset of Fig. 5 were estimated to be $\sim 230 \text{ fF}$ for both devices. Calculations indicated that the purely electrical circuit effects would allow a maximum $f_{3\text{dB}}$ of 15.6 GHz which is very close to the measured value. Thus, it is believed that the Au-wrapped and the Cu-plated VCSELS are limited by electrical parasitics rather than thermal effects. PSpice simulations indicate a modified design which allows Au and Cu to extend to only 2 μm around the mesa is expected to have an electrical 3-dB bandwidth of 63 GHz, but such a structure should still significantly reduce thermal resistance and, thus, improve the overall bandwidth.

IV. CONCLUSION

We have demonstrated the effect of a heat sinking layer on the performance of high-speed VCSELS. A Cu-plated heat spreading layer reduced the thermal resistance and increased both the output power and the maximum 3-dB frequency. The self-aligned process allowed smaller mesa diameters for a given aperture size, thus decreasing the distance for heat to flow to the sidewall as well as mesa parasitic capacitance. It is believed that the Cu-plated VCSELS reported here are limited by electrical parasitics rather than thermal effects. The tradeoff between thermal impedance and parasitic capacitance reduction needs to be optimized by appropriate design of the heatsink geometry. By limiting the plated Cu extension to 2 μm , simulations indicate the purely electrical circuit effects would allow a maximum 3-dB bandwidth of $\sim 63 \text{ GHz}$.

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