SEE NEXT PAGE

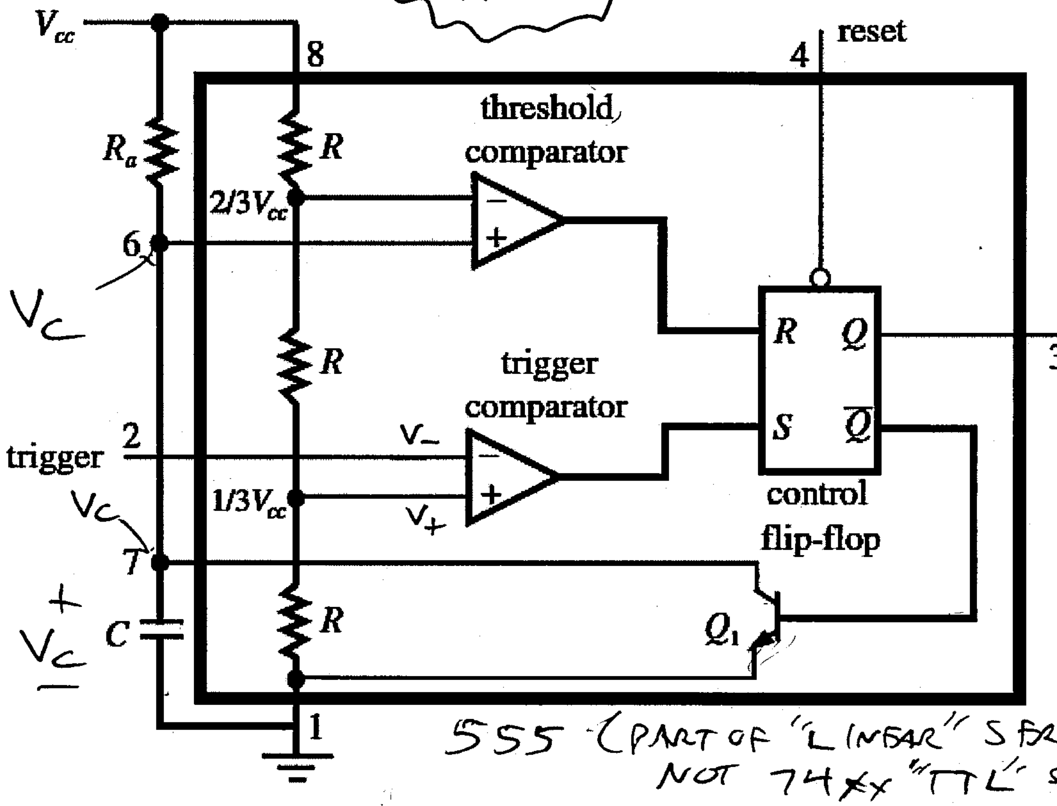
CAN ALSO BE DONE ~~WITH~~: 74123

↓

"ONE SHOT"

trigger = ↓

output = ⎍




555 (PART OF "LINEAR" SERIES NOT 74xx "TTL" SERIES)

**Figure 6.42** (p. 241)

HAS NO EFFECT DURING CAP. CHARGING

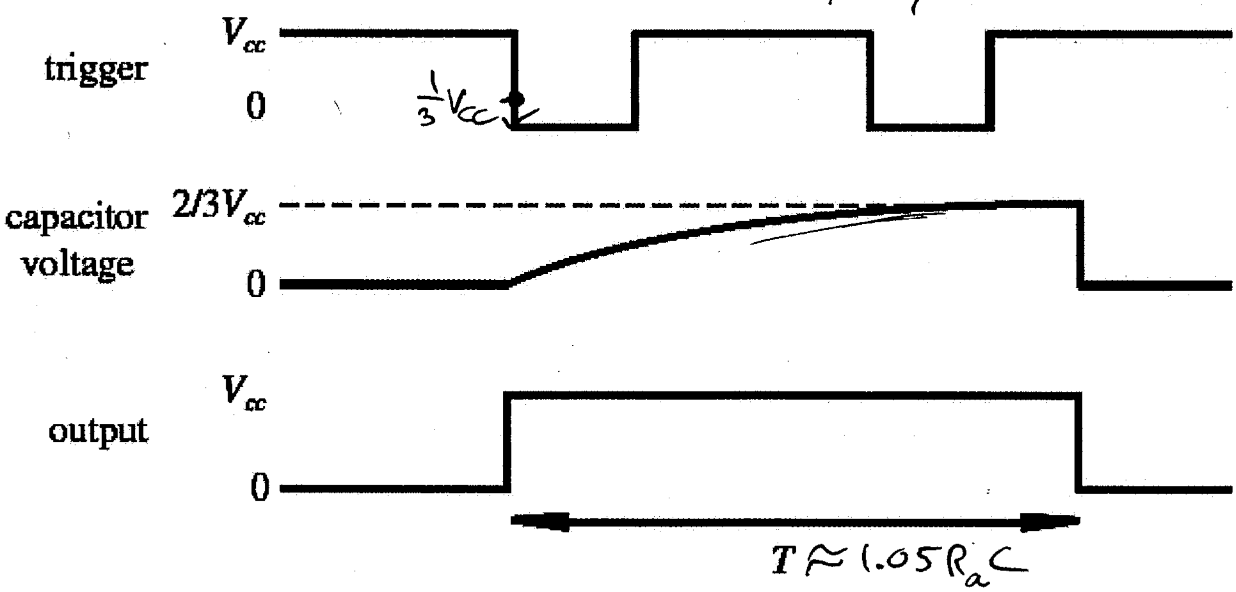



**Figure 6.43** (p. 242)

# FG.42

COMPARATOR : OUTPUT $= \begin{cases} 1 & V_+ > V_- \\ 0 & V_+ < V_- \end{cases}$

$$\overbrace{V_c}^{V_+} > \overbrace{\tfrac{2}{3}V_{cc}}^{V_-} \Rightarrow R=1 \Rightarrow Q=0,\ \overline{Q}=1$$

$Q_1$: ON $\Rightarrow$ CAPACITOR DISCHARGE ($V_c = 0$)

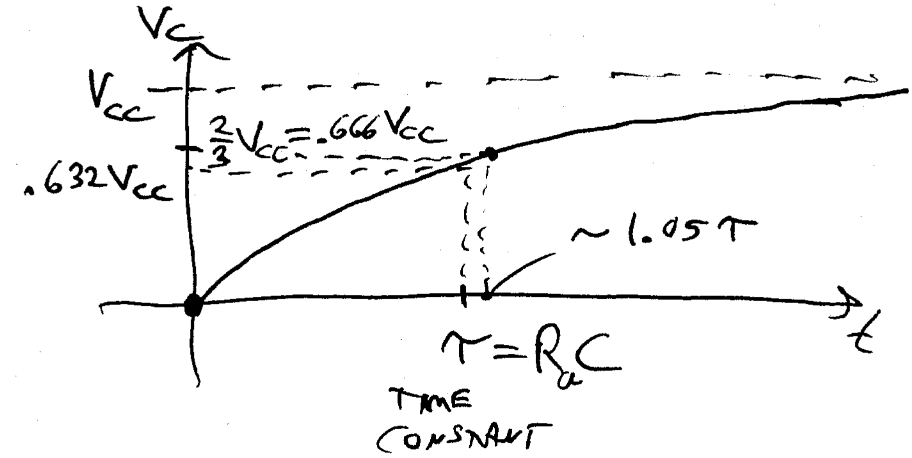
$$\overbrace{\text{trigger}}^{V_-} < \overbrace{\tfrac{1}{3}V_{cc}}^{V_+} \Rightarrow S=1 \Rightarrow Q=1$$

$\Rightarrow \overline{Q}=0 \Rightarrow Q_1$: OFF

$\Rightarrow$ CAPACITOR CHARGES

## EXTERNAL $R_a$-C CIRCUIT

CHARGES AS
A FIRST-ORDER
SYSTEM



SEE
- COURSE POLICIES
- HOW TO DO WELL
  - SAMPLE EXAM (LEAVE UP)
  - GRADING
  - REVIEW TOPICS

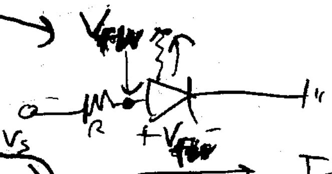
[ • GO THROUGH SAMPLE QUESTIONS (SEE HIGHLIGHTS) ]

SKIP

# ME307 - Exam I Review Topics

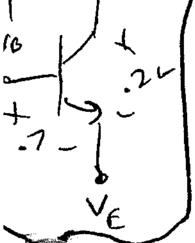
reading assignments covered: Chapters 1, 2, 3, 6; Appendix A
(see the syllabus for section details)

1. mechatronic and measurement systems
2. basic electric circuits
    a. KVL, KCL
    b. Ohm's Law — $V = IR$, $V_A - V_B$
    c. voltage division — $V_1 = \frac{R_1}{R_1+R_2} V_s$
    d. current division — $I_1 = \frac{R_2}{R_1+R_2} I_s$
    e. equivalent resistance — $R_s = R_1 + R_2$, $R_p = \frac{R_1 R_2}{R_1+R_2}$
    f. capacitor — $V = \frac{1}{C} q$, $\int I\,dt$
    g. inductor — $V = L \frac{dI}{dt}$
3. ac circuits
    a. complex impedance — $\frac{-j}{\omega C}$, $j\omega L$; $Z_C, Z_L$ provided if needed
    b. waveform terminology — $\omega$, f, T, $\phi$, $V_{pp}$, $V_m$, dc offset
    c. phasor analysis — $r_1\angle\phi_1 \cdot r_2\angle\phi_2 = r_1 r_2 \angle(\phi_1+\phi_2)$; $r_1\angle\phi_1 / r_2\angle\phi_2 = \frac{r_1}{r_2}\angle(\phi_1-\phi_2)$
        i. rectangular form
        ii. complex form
4. diodes
    a. forward and reverse bias
    b. real vs. ideal
    c. flyback protection
    d. LEDs — $V_{fbv}$



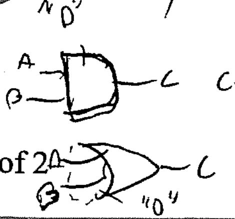
$I = \frac{V_s - V_{fbv}}{R}$ fbv: forw. bias volt.

5. transistors — ON (CE connection)
    a. saturation and cutoff
    b. circuit analysis — OFF (CE open circuit)



$V_E + .7$, $V_C = V_E + .2$

6. digital circuits
    a. terminology — A=10, B=11 ..., F=15
    b. number systems (binary, hex, BCD) — $29_{10} = 11101_2 = 1D_{16}$; $16+8+4+1$; $1\cdot16 + 13\cdot16^0$; $= 0010\,1001_{BCD}$ (2, 9)
    c. gates (AND, OR, INV, and varieties)
    d. Boolean algebra and basic identities
    e. De Morgan's Laws — OR $\overline{A+B} = \overline{A}\cdot\overline{B}$; AND $\overline{A\cdot B} = \overline{A}+\overline{B}$
    f. logic circuit design
        i. deriving a Boolean expression from a truth table



C=1 IFF A=1 AND B=1
C=1 IF A=1 OR B=1
C=0 IF A=0 AND B=0

(sum-of-products, product-of-sums)

ii. simplification of Boolean expressions

iii. De Morgan all-AND and all-OR realizations

g. logic circuit analysis

i. Boolean expression

ii. truth table

iii. timing diagram

h. flip-flops

i. RS, JK, D, T

ii. preset and clear

iii. level and edge triggering

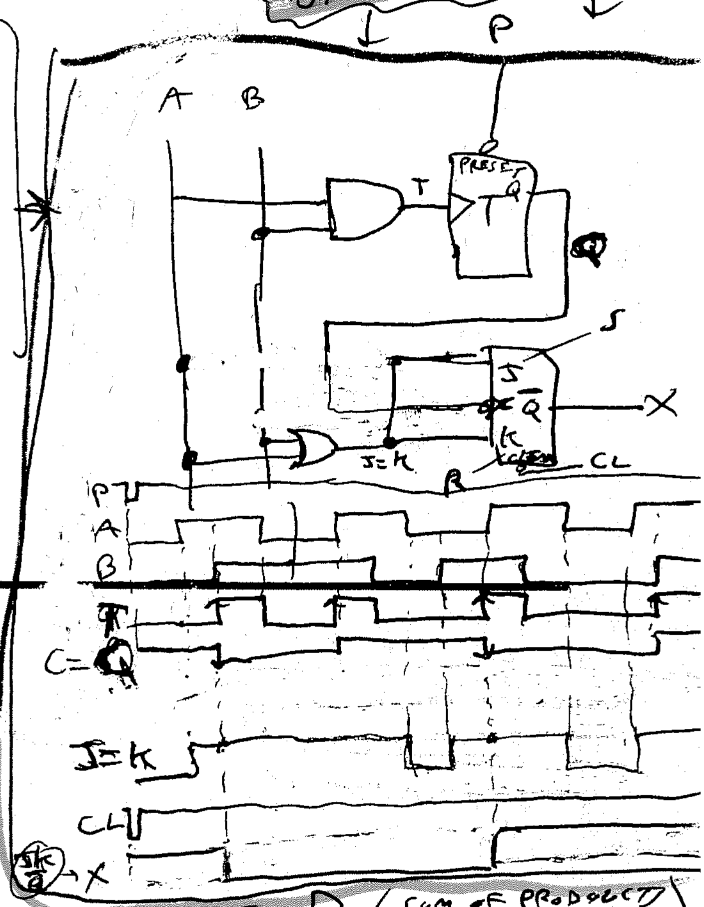
7. miscellaneous

a. reading assignments

b. homework assignments

c. Lab exercises

ONLY IF HAVE TIME




EX) CAR BUZZER EXAMPLE

| | door A | seat belt B | ignition C | X |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 0 |
| 7 | 1 | 1 | 1 | 0 |

$2^3 = 8$ COMBOS

FEWEST 1's ⇒ SOP (SUM OF PRODUCTS FOR "1 STATE" OF EACH 1-OUTPUT ROW)

$$X = \underbrace{(\bar{A}\cdot\bar{B}\cdot C)}_{\text{row } 1} + \underbrace{(\bar{A}\cdot B\cdot C)}_{\text{row } 3} + \underbrace{(A\cdot\bar{B}\cdot C)}_{\text{row } 5}$$

$$= \bar{A}C\underbrace{(\bar{B}+B)}_{1} + A\cdot\bar{B}\cdot C$$

$$= C\cdot(\bar{A} + A\bar{B}) = C\cdot(\bar{A}+\bar{B})$$

$$= C\cdot\left(\overline{\bar{\bar{A}}\cdot\bar{\bar{B}}}\right)$$

$$= C\cdot\overline{A\cdot B}$$

D... MOR...

| A | B | $\bar{A} + A\bar{B}$ | $\bar{A}+\bar{B}$ |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |