Logout Syllabus Jesse Wilson

Close your browser to end your session. (http://www.acns.colostate.edu/single-sign-on-using-shibboleth/#1471272725675-5603b487-ebab)

ECE545 FPGA Signal Processing and Software-Defined Radio

Fall 2021
Lectures: 9:00 AM -- 9:50 AM, Mon/Wed/Fri, Wagar 231
Instructor: Jesse Wilson
Email: jesse.wilson@colostate.edu (mailto:jesse.wilson@colostate.edu)
MS Teams Messaging: Wilson,Jesse
Phone: 970-491-3706
Office Hours: by appointment.

https://calendar.google.com/calendar/embed?src=rkbgfgh2ibfgnf5p6ccu2lf344%40group.calendar.google.com&ctz=America%2FDenver (https://calendar.google.com/calendar/embed?src=rkbgfgh2ibfgnf5p6ccu2lf344%40group.calendar.google.com&ctz=America%2FDenver)

ECE545 FA2021

Today | **October 2021** | Print | Week | **Month** | Agenda

Sun	Mon	Tue	Wed	Thu	Fri	Sat
26	27 13: FIR/RAG pipe	28	29 14: FIR with Dist HW06 RAG filter	30	Oct 1 PROJECT PROPOS REVIEW	2
3	4 EXAM 2: FIR	5	6 15: IIR and feedb HW07 RAG FIR ir	7	8 16: HDL challeng	9
10	11 17: IIR architectu	12	13 18: IIR lookahea HW08: IIR Filter	14	15 19: Parallel IIR o	16
17	18 20: Adaptive filte	19	20 REVIEW	21 HW: Look-ahead	22 EXAM 3: IIR	23
24	25 21: Comm syster	26	27 22: Sample rate HW: CORDIC or a	28	29 23: Polyphase FI	30
31	Nov 1 24: Cascaded int	2	3 25: Phase-locked HW: polyphase F	4	5 26: Analog/digita PROJECT PROGRE	6

Events shown in time zone: Mountain Time - Denver

Calendar

COURSE OBJECTIVES:

The student successfully completing this course will be able to:

- Distinguish FPGA vs microprocessor-based DSP implementation, explain tradeoffs between them, and select an architecture by weighing power consumption, bandwidth, and development effort considerations.
- Identify and explain consequences of analog/digital conversion of radio-frequency signals, such as aliasing and effective bit gain from oversampling.
- Distinguish and select between and fixed-point and floating-point arithmetic, depending on design objectives, and utilize IEEE math libraries to implement basic operations in either format.
- Construct and test in Verilog or VHDL the basic signal processing components: Numerically-controlled oscillator (NCO), mixers, finite- and infinite-impulse response filters (FIR, IIR), adaptive filters, and cascaded integrator-comb downsampling and upsampling (CIC) filters.
- Explain the Fast-Fourier Transform, identify how its implementations on an FPGA differs from on a DSP microprocessor, and construct it in Verilog or VHDL.

- Configure and make use of commercially-available intellectual property (IP) blocks to speed up DSP implementation.
- Configure and integrate on-chip soft CPU to reduce development time of functionality better suited to microprocessors (e.g. configuration, control, serial communications)
- Design and build all the digital elements of a basic communications system, including amplitude modulation of an NCO-generated carrier, transmission through a simulated channel, and demodulation with a digital downconverter (DDC).
- Engage in continued learning beyond this course, to be able to design and implement FPGA-based DSP systems with more sophisticated components (e.g. wavelets, spread-spectrum coding, real-time video processing)

PREREQUISITES: ECE311, ECE312, ECE451

REQUIRED BACKGROUND KNOWLEDGE:

- VHDL or Verilog experience
- Binary arithmetic and computer number systems
- Linear systems concepts, e.g. convolution, Fourier series, ...
- Digital filters, z transform, etc.

REQUIRED MATERIALS:

- *Digital Signal Processing with Field Programmable Gate Arrays,*4th ed. by Uwe Meyer-Baese. Springer, 2014. Hardcopy recommended. PDF can be downloaded from on-campus computers at **https://link.springer.com/book/10.1007%2F978-3-642-45309-0 (https://link.springer.com/book/10.1007%2F978-3-642-45309-0)** or off-campus through the **CSU Library Proxy (https://lib2.colostate.edu/help/plugins/proxy-url-converter.html)** .
- MATLAB software.
- Xilinx Vivado Design Suite or Altera Quartus. (ENS installation pending)
- A Verilog or VHDL textbook (search CSU library website; there are a few options with online e-book access).

Canvas : canvas.colostate.edu will have the syllabus, links, homework, course grades and other postings. It is your responsibility to check the calendar under the Index tab each week for new postings.

COURSE TOPICS: The planned topics for this course are:

Weeks 1-3	**Introduction**: FPGA technology, VHDL/Verilog review, FPGA vs DSP processors, Digital logic timing, Binary arithmetic	**Exam 1** on 9/13/2021
Week 4-6	**Finite impulse response filters**: Theory, z-transforms, FPGA implementation, Reduced adder graph, IP core usage	**Exam 2** on 10/1/2021