ECE102 - Digital Circuit Logic - Fall 2024

Instructor: Prof. Mahdi Nikdast (http://www.engr.colostate.edu/~mnikdast/)

Email: Mahdi.Nikdast@colostate.edu

Teaching Assistants: Mr. Zheyi Qin (Zheyi.Qin@colostate.edu), Ms. Zahra Ghanaatian (Zahra.Ghanaatian@colostate.edu), and Mr. Dylan Schepanski (Dylan.Schepanski@colostate.edu).

Office Hours:

Instructor	**Time**	Location
Prof. Nikdast **(Online)**	**Friday:** **11 AM – 11:45 AM** **Monday:** **4:00 PM – 4:30 PM**	Join **Zoom** Meeting https://zoom.us/j/91452296885?pwd=QjlfE6vPWTpYd8gWH4hUkgs3xQCoBL.1 Meeting ID: 914 5229 6885 Passcode: 221013
Mr. Qin	**Monday:** **10:40 AM – 11:30 AM** **Monday:** **4:30 PM – 5 PM** **Thursday:** **5 PM – 6 PM**	**In person in C207.**
Ms. Ghanaatian	**Thursday:** **12 PM – 1 PM**	**In person in C207.**
Mr. Schepanski	**Wednesday;** **12 PM – 2 PM**	**In person in C207.**

Lectures: Tuesday, Thursday 11 AM – 12:15 PM. **Scott Room 101.**

Labs: https://www.engr.colostate.edu/ECE102/Fall2024/labs.htmll

Objectives: To understand the concepts of digital logic and learn methods and tools for the design of digital circuits.

Prerequisites: Major in ECE or prior approval.

The official home page for ECE102 is **Canvas**. Students are expected to visit the official home page **frequently** for class handouts, assignments, and important announcements!

Grading Policy: The grade will be based on

Homework (**Every week**)	20%
Labs (**12+1 in total**)	25%
iClicker Quizzes	10%
Midterm 1 (**September 26, 2024**)	15%
Midterm 2 (**November 12, 2024**)	15%
Final Exam (**Dec 11, 2024; 6:20 PM – 8:20 PM; Scott Room 101)**	15%

The +/- grading scheme will be used, with the scale

>95%	90-94%	85-89%	80-84%	75-79%	70-74%	65-69%	55-64%	40-54%	<40%
A+	A	A-	B+	B	B-	C+	C	D	F

iClicker Quizzes: During the lectures (and mostly at the beginning of each lecture), there will be several **in-class quizzes using iClickers**. **iClicker quizzes cover the material taught on the same day of the lecture OR to review materials delivered in the previous lecture. Therefore, it is important to attend the lectures, while considering the safety of others in case of sickness, to take part in iClicker quizzes, which account for 10% of the final course grade.** In case of sickness, you can contact the instructor **before** the lecture to be excused from the iClicker questions. **Each student can miss up to three iClicker sessions without any penalty. Online students** will receive an online quiz every month instead of in-class iClicker quizzes.

Homework Procedures: Homework assignments are due online (**must be submitted on Canvas as pdf**). Selected questions from each homework assignment will be graded. However, turn in **ALL** of the assigned problems. All assigned problems are equally important for the development of your understanding of the subjects of digital logic. To receive full credit for your homework, show **ALL** reasonable steps in solving the problem. Written solutions will be available online after the due date of the homework. **Make sure the file you submit to Canvas is readable, otherwise the course grader will NOT grade your assignment.**

Late Policy: Quizzes and Exams must be taken as scheduled in order to receive credit. Late homework **will NOT** be accepted unless its lateness is due to circumstances beyond your control (**official** proof is required). To receive full credit, lab reports **must be submitted online through Canvas** on/before the date due. Late lab reports will be accepted, but points will be deducted from the score (see penalties below).

Lab Assignments and Attendance: Laboratory assignments are a very important component of this course. You will learn to design and develop digital logic circuits, and by the end of the semester, will be able to design sophisticated digital circuits. We use a set of digital tools used by professional engineers, which may appear a bit intimidating at first. After the first two to three labs, you will become comfortable with the tools and will be on your way to designing some interesting circuits.

- **You must pass EVERY lab assignment with score > 60% to pass the course.**
- **Lab board: Online students** will receive the board required in the lab from CSU (please watch out for an email from Mr. Brayan Trejo (trejo@colostate.edu) for shipping information. Students in **in-person lab sessions** will receive the lab board (do **NOT** purchase online).

- **Lab attendance (online and in-person): Mandatory (TAs will record participation)**. In rare situations when you cannot attend your scheduled lab session due to circumstances beyond your control, you **must** obtain clearance in advance from your lab instructor (TA). In such a case, you can attend another lab section during that same week **ONLY IF YOU GET APPROVAL FROM YOUR TA**. Remember that all lab projects must be completed with a passing grade in order to pass the course **(i.e., >60%**).
- **Conduct in the lab:** Students are expected to maintain a professional working atmosphere in the lab (online and in person), which includes not disturbing other students or groups, not talking loudly, and following additional instructions provided by Teaching Assistants. **Use of cellphones (for voice or texting) is not allowed. No food or drinks allowed in C207. TAs are responsible to report any misconduct or unprofessional behavior to the instructor for further actions.**
- **Prelab:** Prelabs should be checked at **the beginning of corresponding lab sessions**. This prelab must be included in your lab reports every week.
- **Demonstration of hardware circuits & Submitting Project reports:** You may submit the hardware demo any time before the start date of the next project for your lab section (**online students:** Please see **Lab Demo Instructions** on Canvas). **All the lab demos must be presented in person during the lab sessions (or online through YouTube for online students --- Please see the Online Demo Instructions).**
- **Policy on collaboration with other students:** Design alone, build alone, write alone, and submit individually prepared reports and circuits. It is fine to talk, give advice, receive advice, but do your own work.
- **Grading policy:** The grading differs from one lab project to the other. An example would be: hardware circuit: 30%, required technical items in the report: 40%, memo text: 20%, instructor discretion: 10%. A neatness bonus of 5% may be assigned. **In addition, you must be able to answer all the questions asked by your TA.**

- **Penalties:** Penalties will be assessed for each lab report (except where specifically allowed): -15% for missing the lab session, -5% for missing prelab, **-5%-per-day for late submission**, and -10% for not following Banana memo format (https://www.engr.colostate.edu/ECE102/FALL2024/LABS/preparingmemo.html).

Conduct and Nature of Exams: You will be allowed to use one double-sided page of notes, prepared by you, during the three exams. Exams will be straightforward BUT will demand the kind of preparation only possible through continual, daily study.

Instructional Objectives: Given during class, these are the bases of all exam questions and homework assignments. For this reason, **consistent class attendance is very important**.

Textbook: Fundamentals of Logic Design, by Charles H. Roth published by Cengage Learning. The latest is the 7th Edition. Sixth, fifth or fourth editions are acceptable. Some of these earlier editions were published by Thompson Publishing Co. Be aware that there are differences in chapter, page and problem numbers of the different editions. CSU Bookstore carries a paperback version containing the necessary chapters of the 7th edition at a lower price compared to the regular version. It is not critical to have the text during the first week.

Tutoring: The course's Graduate Teaching Assistants (TAs) will be available for drop-in consultation as well as help sessions at times listed on the website.

Academic Integrity: This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (http://www.conflictresolution.colostate.edu/academic-integrity) and the Student Conduct Code (http://www.conflictresolution.colostate.edu/conduct-code). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services**. My policy is that of zero tolerance.** Minor first infraction in HWs and Lab reports will lead to a zero score **(-40%** for Lab assignments) as well as one letter level (e.g., A to B) reduction in the course grade. Project or Major or repeated infractions in HWs and Lab reports will result in "**F**" grade for the course as well as reporting to the Dean's Office. Any misconduct in an exam (e.g., cheating) will lead to a zero score for that exam, and very likely, course failure.

All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one's own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken.

Diversity Statement: As the instructor in ECE102, I am deeply committed to helping build an inclusive culture in the classroom, in the Department of Electrical and Computer Engineering, in the Walter Scott, Jr. College of Engineering, and at CSU. Each individual brings diversity to our class in the identities they hold, the ways they think, their interests and skills, their background and past experiences. To me, inclusion means not only accepting these differences, but embracing them and understanding that we can leverage these differences to be better engineers.

My goal for this class is to create an environment where we do not discriminate against individuals because of their identities (e.g., race, ethnicity, sex, gender identity, sexual orientation, religion, nationality, age, levels of ability). It is also important to understand that even when we hold egalitarian beliefs, we can hold implicit or unconscious biases that can also influence the way we treat others or approach engineering design. It is my expectation that students in this class will:

1. Adhere to the CSU Principles of Community https://diversity.colostate.edu/principles-of-community/;
2. Work in teams in ways that recognize the contributions of all team members and provide all team members the opportunity to learn;
3. Examine their own behaviors and refrain from acting in biased ways;
4. Reflect on the ways bias can influence engineering work;
5. Speak with the professor when biased behaviors may occur from other students, their TAs, and the professor;
6. Be sensitive to context and acknowledge that hurtful comments can sometimes be inadvertent, but they still have an impact.

CSU Has Resources to Help

Many of us are struggling. CSU is a community that cares. You are not alone. CSU Health Network Counseling Services has trained professionals who can help. Your student fees provide access to a wide range of support services. Call Counseling Services at (970) 491-6053, and they will work together with you to find out which services are right for you.
Visit https://health.colostate.edu/about-counseling-services (Links to an external site.) to learn more and https://health.colostate.edu/mental-health-resources/ (Links to an external site.) for additional student mental health and well-being resources. If you are concerned about a friend or peer, use Tell Someone by calling (970) 491-1350 or visiting https://supportandsafety.colostate.edu/tell-someone/ (Links to an external site.) to share your concerns with a professional who can discreetly connect the distressed individual with the proper resources. Rams Take Care of Rams. Reach out and ask for help if you or someone you know if having a difficult time.

CSU Syllabus Resources and Policies: https://tilt.colostate.edu/syllabus-resources-and-policies/

Topics (Dates/Topics may change with reasonable notice**):**

Week	**Course Objectives**	**Readings**
W1 (Aug. 19)	**Introduction to ECE102 and digital systems** - State the differences between analog and digital systems	N/A
W2 (Aug. 26)	**Binary representation of information** - Define the term “positional number system” - Represent numbers in decimal, binary, octal and hexadecimal notations and convert from one notation to the other	Ch. 1

	- Add, subtract, multiply and divide binary numbers - Represent numbers in sign-magnitude, one's complement and two's complement forms - Carry out addition and subtraction, and identify overflow conditions - Represent numbers in binary coded decimal format (BCD) - Represent characters using ASCII format	
W3 (Sep. 2) W4 (Sep. 9) -	**Boolean Algebra and Combinational Logic** - Define the basic logic operations (AND, OR, NOT) - Evaluate Boolean expressions - Derive the logic function implemented by a combinational logic circuit - Use Laws and Theorems of Boolean Algebra to simplify logic expressions - Find the complement of a Boolean expression using DeMorgan's Law - Find the dual of a Boolean expression - State and use the Negative Logic Theorem - Use Consensus theorem to simplify logic expressions - Implement Boolean expressions using 2-level networks (SOP, POS)	Ch. 2 Ch. 3
W5 (Sep. 16)	- Convert functional specifications (written in English) to logic expressions - Convert specifications written in English to a truth table - Write a logic expression as a minimum POS, minimum SOP, canonical POS and a canonical POS - Design logic circuits to add/subtract two's complement numbers - Obtain minterm and maxterm expansions (using m/M notations or in algebraic form) from a truth table or an algebraic expression - Convert a minterm expansion it a maxterm expansion and vice versa - Use m/M notation to obtain product/sum of logic expressions - Find the minterm and maxterm expansions of F', F.G, F+G where F, G are Boolean functions Hardware for Arithmetic - Design logic circuits to add/subtract two's complement numbers - Design an array multiplier for binary integers	Ch. 4
W6 (Sep. 23)	- Use don't care terms to simplify logic expressions - Represent 3,4,5 and 6 variable functions using K-maps	Ch. 5

	- Represent expressions given in SOP, POS, maxterm or minterm form on K-maps - Obtain minimum POS and SOP expansions using K-map - Design multiple output circuits using K-maps - Represent 5 and 6 variable functions using K-maps and obtain minimum SOP, POS	
	Midterm 1 (September 26, 2024)	
W7 (Sep. 30)	- Implement logic functions using multilevel networks - Derive alternative gate symbols for basic logic gates - Implement logic functions using basic 2-level forms (NAND-NAND, AND-OR etc.) - Convert networks from one form to another	Ch. 7
W8 (Oct. 7)	- Implement logic functions using only NOR gates or only NAND gates - Describe the operation of tri-state logic gates, multiplexers and decoders - Implement logic functions using multilevel networks - Design multiple-output circuits - Implement combinational logic expressions using multiplexers, decoders, ROMS and programmable logic	Ch. 8 Ch. 9
	Sequential Circuits	
W9 (Oct. 14)	- Describe the operation of S-R, T, D, and J-K latches and flip-flops	Ch. 11
W10 (Oct. 21)	- Draw timing diagrams of circuits containing latches and flip-flops - Draw the circuit diagram, and describe the operation of registers, shift registers, cyclic shift registers, etc.	Ch. 12
W11 (Oct. 28)	- Analyze Moore and Mealy type sequential networks, i.e., given a sequential circuit, - Derive the state graphs/ state tables of a given sequential circuit	Ch. 13
W12 (Nov. 4)	- Draw timing diagrams corresponding to given input waveforms - Derive Moore and Mealy type state diagrams to meet given specifications - Synthesize Moore & Mealy circuits to meet given specifications using D, T, J-K and/or S-R flip-flops	Ch. 14 Ch. 15
W13 (Nov. 11)	- Identify equivalent states and reduce state diagrams to minimum number of states	
W14 (Nov. 18)	- Determine whether two state diagrams are equivalent - Use Alphanumeric Notation in state graphs	

	- Verilog
	Midterm 2 (November 12, 2024)
W15 (Nov. 25)	**Enjoy your fall break!** 😊
W16 (Dec. 2)	Review
Wednesday –	**Final Exam**
December 11, 2024	**6:20 PM to 8:20 PM**
	Scott room 101

Lab Assignments and Instructions:

- It is essential to read the assignment before the lab and be ready to begin when you come to the lab.
- Report is due in a week.

- Official lab webpage: https://www.engr.colostate.edu/ECE102/Fall2024/labs.html.

Lab Schedule:

L01: Monday, 2:00 PM – 3:40 PM (TA: Zheyi Qin)
L03: Thursday 8:00 AM – 9:40 AM (TA: Dylan Schepanski)
L04: Thursday 3:00 PM – 4:40 PM (TA: Zheyi Qin)
L05: Friday 9:00 AM – 10:40 AM (TA: Zahra Ghanaatian)
L06: Wednesday 8:00 AM – 9:40 AM (TA: Dylan Schepanski)
L07: Monday 9:00 AM – 10:40 AM (TA: Zheyi Qin)
L08: Friday 11 AM – 12:40 PM (TA: Zahra Ghanaatian)

Week	**Project Description**
Aug 19 - Aug 23	Lab 0: Introduction Creating an Engineering Network Account
Aug 26 - Aug 30	Lab 1: Introduction to Altera DE board and Quartus II Design Software
Sep 2 - Sep 6	Lab 2: Schematic Entry, Timing Diagrams and Functional Simulation using Quartus II
Sep 9 - Sep 13	Lab 3: Design, Simulation and Verification of Combinational Circuits
Sep 16 - Sep 20	Lab 4: Two's Complement Adder Subtractor Design
Sep 23 - Sep 27	Lab 5: The Arithmatic Logic Unit
Sep 30 - Oct 4	Lab 6: The Seven Segment Display

Oct 7 - Oct 11	Lab 7: BCD to Seven Segment Display
Oct 14 - Oct 18	Lab 8: Accumulator Based Tally Unit
Oct 21 - Nov 1	Lab 9: Register Bank and Shift Registers
Nov 4 - Nov 8	Lab 10: Design of Counters
Nov 11 - Nov 15	Lab 11: Encryption Unit
Nov 18 - Nov 22	Lab 12: Nanoprocessor
Nov 25 - Nov 29	**Fall Break**
Dec 2 - Dec 6	(Demo Time)