ECE 571/575 Course Syllabus: Spring 2021
VLSI System Design and Experiments

Instructor: Dr. Ryan G. Kim
Office Location: Engineering C201G (I will not be in much this semester due to COVID-19)
Email: Ryan.G.Kim@colostate.edu
Office Hours: Wed 11:00 – Noon or by appointment

Lab TA: Lekha Rane
Email: Lekha.Rane@colostate.edu
Office Hours: TBD

Class Lectures: Tuesdays and Thursdays 2:00 – 3:15 PM	Online on Zoom
Lab – S01: Friday 2:30 – 4:15 PM	Engr C205
Lab – S02: Wednesday 3:30 – 5:15 PM	Engr C205
Lab – S10: TBD	Online on Zoom

Required Text: **CMOS VLSI Design**, Neil H.E. Weste and David Money Harris, Fourth Edition.

Course Description: ECE 571 is a senior level as well as an entry level graduate three credit lecture course on VLSI design. ECE 575 is the corresponding one credit lab course required to be taken concurrently. The purpose of these courses is to provide students with opportunities to learn and practice the entire process of VLSI chip design. There is a substantial amount of design work associated with the lectures and labs. Students will go through various design stages from logic and circuit design and simulation to layout and design verification. All the design activities will be carried out using Cadence design tools. Up to 4 design labs are scheduled concurrent with the lectures. Students are required to submit a design report and to participate in design reviews.

Prerequisites: ECE451 (Digital System Design)

Grading:
The following is the grading breakdown for each major component:

- Midterm Exams 20%
- Final Exam 35%
- Labs 25%
- Homework Assignments 15%
- Class Participation & Quizzes 5%

Grading Scale:
While lower cutoffs may be used, the following grade cut-offs are guaranteed:

A	A-	B+	B	B-	C+	C	D
93	90	87	83	80	77	70	60

Course Outline:

Week	Topic
1	Introduction, MOS transistors
2	MOS transistors
3	CMOS Layout. CMOS Fabrication
4	CMOS Fabrication. Delay and Optimization
5	Delay and Optimization
6	Delay and Optimization. Power
7	Power. Interconnect
8	Interconnect. Midterm
9	Combinational Logic
10	Combinational Logic. Sequential Logic, Timing Analysis, and Metastability
11	Sequential Logic, Timing Analysis, and Metastability
12	Sequential Logic, Timing Analysis, and Metastability. Clocking and Clock Systems
13	Robustness. Test, Debug, and Verification
14	Test, Debug, and Verification
15	Review

Academic Integrity:

This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (http://www.conflictresolution.colostate.edu/academic-integrity) and the Student Conduct Code (http://www.conflictresolution.colostate.edu/conduct-code). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services.

All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one's own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken. My policy is that of zero tolerance. Minor first infraction in HWs will lead to a zero score as well as one letter level (e.g. A to B) reduction in the course grade. Major repeated infractions in HWs will result in "F" grade for the course as well as reporting to the Dean's Office.