ECE 480A4: Digital Logic Synthesis

IN

Boolean Algebra

- Understand fundamentals of Boolean logic and algebra

Logic Gates and Circuits

- Understand representation of logic as gate-level schematics, and logic circuit implementations

Algorithms and Optimization

- Understand algorithms and data structures
- Understand differences between tractable and intractable problems
- Has basic knowledge of algorithms/methods to solve optimization problems

Programming Language and HDL

- Has (basic) knowledge of a programming language (e.g., Python) and HDL

Pre-requisites

- ECE102 with a minimum grade of C

Concepts:

- Overview of logic synthesis
- Introduction to VLSI CAD and design automation flow
- Hardware description language (HDL)
- Binary decision diagram
- Satisfiability
- Two-level logic minimization (exact and heuristic methods)
- Multi-level logic synthesis (including algebraic techniques)
- Boolean decomposition
- Delay optimization (including timing analysis)
- Sequential logic optimization (including two- and multi-level encoding)
- Technology mapping
- Physical synthesis (standard cell mapping and technology mapping on FPGAs)
- New directions in logic synthesis

Applications:

- Complex but optimized digital computers and systems

Tools:

- HDL compilation and synthesis
- Boolean SAT tools
- Two-level and multi-level optimization tools (e.g., ESPRESSO)
- ABC (A System for Sequential Synthesis and Verification)

OUT

Algorithms for Logic Synthesis and Optimization

- Understand, design, and apply algorithms for digital logic minimization

Design Verification and Tools

- Understand modern approaches to logic design and verification of digital circuits

Technology Mapping

- Understand technology-mapping to both ASICs and FPGAs

Design Automation Flow

- Use a variety of design and simulation tools to design and validate complex logic circuits

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