



MAHDI NIKDAST

Associate Professor

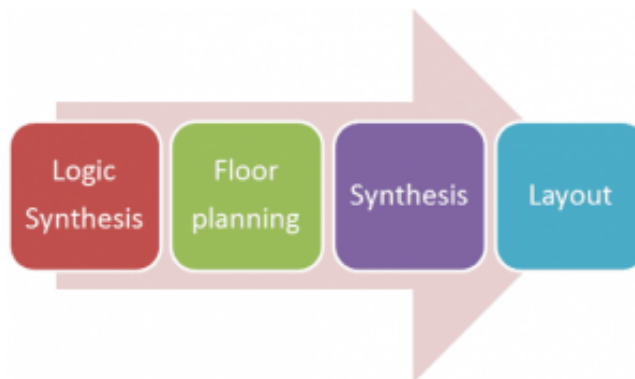
Electrical and Computer Engineering

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Digital Logic Synthesis – ECE445



Instructor: Prof. Mahdi Nikdast (E-mail: Mahdi.Nikdast@colostate.edu).

Office Hours: **ONLINE** on Zoom! Mondays from 11 AM to 12 PM. Check Canvas for the Zoom call info!

Course Assistant: Ebad Taheri (E-mail: Ebad.Taheri@colostate.edu). Office hours: Fridays from 1 PM to 1 PM. Check Canvas for the MS Team call info!

Lectures: Tuesday and Thursday, 2:00 PM – 3:45 PM, Rm 108, Walnut.

Course on Canvas: Click [here](#)

Course Summary

What is Logic Synthesis?

Logic synthesis is the process of converting a high-level description of design (usually defined using a hardware description language) into an optimized gate-level representation. Logic synthesis uses a standard cell library which have simple cells, such as basic logic gates like and, or, and nor, or macro cells, such as adder, muxes, memory, and flip-flops.

Course Description

This course educates students on how to extract gate-level circuits from high-level hardware description languages (HDL) and apply top-down design methodology to optimize the designs to achieve better power, performance, timing, and area. Advanced concepts in logic optimization, simulation and testing, and synchronous and asynchronous circuits, as well as a comprehensive review of HDL will be covered.

Course Learning Objectives

Here is a summary of ECE445 learning objectives:

- 1) Study hardware description language (HDL) and extract gate-level circuits from high-level hardware description languages;
- 3) Explore electronic design automation (EDA) solutions for the design and optimization of digital systems;

2) Study and Apply design optimization methods (e.g., top-down design methodologies to optimize the designs) to digital systems;

3) Study two-level and multi-level logic synthesis;

4) Examine and study timing analysis, physical design, physical synthesis, test, and verification.

Course Textbook and Materials

- Instructor will provide notes and slides during each lecture;
- **Textbook:** G. D. Hachtel and F. Somenzi, Logic Synthesis and Verification Algorithms. ISBN: ISBN-13: 978-0387310046.

Course Logistics and Grading Policy

Homework Assignments	30%
In-Class Quiz and Activities	10%
Midterm Exam I (Project)	20%
Midterm Exam II	20%
Final Exam	20%

The +/- grading scheme will be used, with the following scale

>95%	90 – 94%	85 – 89%	80 – 84%	75 – 79%	70 – 74%	65 – 69%	55 – 64%	40 – 54%	<40%
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A+	A	A-	B+	B	B-	C+	C	D	F
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Homework Assignments Procedure, Submission Policy

Homework Assignments: To receive full credit for your homework, show all reasonable steps in solving problems. All the homework assignments should be uploaded electronically on Canvas.

Late Submission Policy: Late homework **will not be accepted** unless the lateness is due to circumstances beyond your control (**official proof [e.g., medical note] is required**).

Instructions to submit your files: All the submitted files should be in PDF format on Canvas.

Academic Integrity

This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (<http://www.conflictresolution.colostate.edu/academic-integrity>) and the Student Conduct Code (<http://www.conflictresolution.colostate.edu/conduct-code>). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services.

All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one's own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken. My policy is that of **zero tolerance**. Minor first

infraction in HWs and presentations will lead to a zero score as well as one letter level (e.g. A to B) reduction in the course grade. Project or Major or repeated infractions in HWs and presentations will result in “F” grade for the course as well as reporting to the Dean’s Office.

Diversity Statement

As the instructor in ECE445, I am deeply committed to helping build an inclusive culture in this classroom, in the Department of Electrical and Computer Engineering, in the Walter Scott, Jr. College of Engineering, and at CSU. Each individual brings diversity to our class in the identities they hold, the ways they think, their interests and skills, their background and past experiences. To me, inclusion means not only accepting these differences, but embracing them and understanding that we can leverage these differences to be better engineers.

My goal for this class is to create an environment where we do not discriminate against individuals because of their identities (e.g., race, ethnicity, sex, gender identity, sexual orientation, religion, nationality, age, levels of ability). It is also important to understand that even when we hold egalitarian beliefs, we can hold implicit or unconscious biases that can also influence the way we treat others or approach engineering design. It is my expectation that students in this class will:

1. Adhere to the CSU Principles of Community
<https://diversity.colostate.edu/principles-of-community/>;
2. Work in teams in ways that recognize the contributions of all team members and provide all team members the opportunity to learn;
3. Examine their own behaviors and refrain from acting in biased ways;
4. Reflect on the ways bias can influence engineering work;
5. Speak with the professor when biased behaviors may occur from other students, their TAs, and the professor;

6. Be sensitive to context and acknowledge that hurtful comments can sometimes be inadvertent but they still have an impact.

Important information for students (added based on CSU regulations):

Masks are required inside university buildings. You must also meet university vaccine or exemption requirements.

All students are expected and required to report to the COVID Reporter (<https://covid.colostate.edu/reporter/>) when:

- You suspect you have symptoms of COVID, regardless of whether or not you are vaccinated and even if your symptoms are mild
- You have tested positive for COVID through a non-CSU testing site, such as home test or test at a pharmacy
- You believe you may have been exposed to COVID go to the COVID Reporter and follow the guidance under “I believe I have been in close contact with someone who has COVID-19.” This guidance will depend upon your individual circumstances

You will not be penalized in any way for reporting symptoms or concerns.

Do not ask me as your instructor to report for you. It is your responsibility to report through the COVID Reporter promptly.

As your instructor I may not ask you about vaccination status or if you have COVID but you may freely volunteer to send me information from a public health official - if you have been asked to isolate or quarantine.

When you complete the COVID Reporter, the CSU Public Health office is notified. Once notified, that office will contact you and, depending upon each situation, will

conduct contact tracing, initiate any necessary public health requirements and notify you if you need to take any steps.

If you do not have internet access to fill out the online COVID-19 Reporter, please call (970) 491-4600.

For the latest information about the University's COVID resources and information, including FAQs about the spring semester, please visit the **CSU COVID-19 site** <https://covid.colostate.edu/>.

CSU Has Resources to Help

Many of us are struggling. CSU is a community that cares. You are not alone. CSU Health Network Counseling Services has trained professionals who can help. Your student fees provide access to a wide range of support services. Call Counseling Services at (970) 491-6053, and they will work together with you to find out which services are right for you. Visit <https://health.colostate.edu/about-counseling-services> (Links to an external site.) (Links to an external site.) to learn more and <https://health.colostate.edu/mental-health-resources/> (Links to an external site.) (Links to an external site.) for additional student mental health and well-being resources. If you are concerned about a friend or peer, use Tell Someone by calling (970) 491-1350 or visiting <https://supportandsafety.colostate.edu/tell-someone/> (Links to an external site.) (Links to an external site.) to share your concerns with a professional who can discreetly connect the distressed individual with the proper resources. Rams Take Care of Rams. Reach out and ask for help if you or someone you know is having a difficult time.

Topics (Dates/Topics may change with reasonable notice. Important dates are in **red**)

Week	Lecture Topics	Reading	HW
W1 (Jan. 15)	Introduction to Logic Synthesis Part I	Ch. 1, 2	HW1
W2 (Jan. 22)	Introduction to Logic Synthesis Part II	Ch. 3	-
W3 (Jan. 29)	HDL (Verilog) Free Online Course (50 minutes) from Intel (Click here). MIT Course on HDL (Click Here).	-	HW2
W4 (Feb. 5)	Quine-McCluskey Method (Summary)	Ch. 4	-
W5 (Feb. 12)	Binary Decision Diagram	Ch. 6	-
W6 (Feb. 19)	Satisfiability	Ch. 5	HW3
W7 (Feb. 26)	Two-Level Logic Synthesis	Ch. 4, 5	-
W8 (March 4)	Midterm 1: Design a SAT/BDD Solver	-	-
W9 (March 11)	<u>No Classes (Enjoy your spring break!)</u>	-	-
W10 (March 18)	Multi-Level Logic Synthesis Part I	Ch. 10, 11	HW4
W11 (March 25)	Multi-Level Logic Synthesis Part II	Ch. 10, 11	-

W12 (April 1)	Multi-Level Logic Synthesis Part II	Ch. 10, 11	–
W13 (April 8)	Midterm 2 (take-home exam)	Ch. 10, 11	–
W14 (April 15)	DC Extraction	–	HW5
W15 (April 22)	Technology Mapping	Ch. 13	–
W16 (April 29)	Physical Synthesis	–	–
May 7, 2024	Final Exam (take-home exam)	–	–

OPEN POSITIONS

I am always looking for motivated students to join our research group. Please [click here](#) for more information.

Current Students at CSU: There are several research opportunities for undergraduate and graduate research in our group. Please [click here](#) for more information.

LATEST NEWS

January 2024: I will be giving an invited talk at 2024 Optica Advanced Photonics Congress in Quebec City, Canada!

January 2024: I will be giving an invited talk at an NSF-sponsored workshop on “Intelligent Photonic Devices and Systems” at University of Utah!

December 2023: Paper on optical PUF using contra-directional couplers is accepted at OFC 2024!

December 2023: Paper on in-sensor optical computing (OISA) is accepted at DATE 2024!

December 2023: Paper on photonic memory (COMET) is accepted at DATE 2024!

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