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Title: Computer Aided Design for Signal and Power Integrity Modeling in High Speed VLSI Design

Abstract:
With the increase in packaging density and signal speeds in VLSI systems, distributed effects arising in passive components such as high speed interconnects and power distribution networks are the main contributors of signal and power degradation at chip, package and board levels. As a result, computer aided design strategies targeting modeling and simulation of such high speed systems are a critical aspect for VLSI designers. However, the computational demands of capturing the distributed nature of such components are a major bottleneck facing traditional circuit solvers. In this presentation I will present innovative numerical algorithms to address this challenge based on my research over the last six years.