CSU ECE Department Seminar Series – Spring 2007

[Please also see ECE Seminar Series web page at http://www.engr.colostate.edu/ece/seminars.shtml for other seminars scheduled (so far) for this semester.]

The Department of Electrical and Computer Engineering at Colorado State University is pleased to present a seminar by

Sudeep Pasricha, Ph.D. Student, University of California - Irvine

Title: "COMMSYN: On-chip Communication Architecture Synthesis for Multi-Processor Systems-on-Chip"

Thursday, March 8, from 10:00 – 11:00 a.m., LSC 220-2

Abstract: Multi-processor systems-on-chip (MPSoC) are highly sophisticated embedded systems that consist of one or more programmable processors running software, memory modules for data storage and other hardware components connected together via an on-chip communication infrastructure. Such MPSoC architectures represent heterogeneous systems offering flexible parallel processing resources for the implementation of emerging applications in the multimedia, networking, aeronautics, automotive and telecommunication domains. One of the most time-consuming activities in a typical MPSoC design cycle is the exploration and implementation of its on-chip communication architecture, since inter-component communication has a critical impact on system performance, power consumption, reliability and overall cost.

In this talk, I will discuss an innovative framework (COMMSYN) that I have developed to automate the process of exploration and synthesis of on-chip communication architectures for MPSoC architectures. The framework accepts a high-level communication constraint graph of the system as input and generates an enhanced architecture model with hardware/software components interconnected via a well defined communication infrastructure, while satisfying multiple design constraints, including power, performance, cost and area. I will describe in detail how the framework comprehensively synthesizes communication architecture topology and protocol parameters while satisfying multiple designer constraints, and show results of applying COMMSYN on industrial-strength MPSoC examples. I will wrap up with a snapshot of some of the other novel features in COMMSYN which make it state-of-the-art, such as physical implementation awareness during synthesis and support for co-synthesis with the memory architecture.

Bio: Sudeep Pasricha is a Ph.D. candidate affiliated with the Center for Embedded Computer Systems at the University of California, Irvine, working with Prof. Nikil Dutt. Sudeep's research interests include design automation and CAD for embedded multi-processor systems-on-chip (MPSoC), system-level modeling languages and methodologies, networks-on-chip (NoC), middleware for distributed systems and

computer architecture. He has given several tutorials on the topic of on-chip communication architecture design at leading conferences, and his research on the exploration and design of on-chip communication architectures is being actively used in industry, at Fujitsu and Conexant. He received a Best Paper Award Nomination at the Design Automation Conference (DAC) in 2005 and a Best Paper Award at the Asia and South-Pacific Design Automation Conference (ASP-DAC) in 2006.

Refreshments will be served.

Please contact Prof. Branislav Notaros, notaros@colostate.edu, with any questions.