



Abell Endowment Distinguished Lecture  
in Computer Engineering,  
in conjunction with the Electrical and  
Computer Engineering Seminar  
Series and the Computer Science  
Department Seminar Series

## “Parallex: An Innovative Execution Model for Exascale Computing”

by

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**Monday October 1, 2012**

Reception at 10:30 a.m.

Lecture at 11 am, Location: CSB 130

**Abstract:** For nearly two decades MPPs and commodity clusters have excelled due to the exponential growth of processor performance and the ubiquity of the MPI programming interface that mapped applications on to resources. Processor core performance is no longer increasing significantly due to the flat-lining of clock rates because of power limitations and the saturation of ILP through exhaustion of processor complexity. With heterogeneous node architectures comprising multicore sockets in combination with GPU accelerators, MPI and its underlying Communicating Sequential Processes (CSP) execution model are no longer sufficient or even appropriate for parallel application programming of future HPC systems. Ad hoc methods of combining different levels of programming models provide short-term examples of the potential of such systems but at the expense of programmability, portability, and efficiency. Throughout the remarkable trillion X history of digital electronic computing, the field has experienced at least five distinct phases; CSP the most recent. Each was driven by technology trends requiring new architectures and new programming models; often with a change in

underlying paradigm as well. Clusters and MPPs that dominate the field of HPC are entering such a phase shift requiring a new paradigm for guiding the programming of new parallel algorithms and governing the design of future cluster nodes. This presentation identifies the challenges facing HPC architecture and programming and describes a new execution model, ParalleX, which may provide a strategy for addressing them. Using the experimental runtime software system, HPX-3, which serves as a reference implementation for ParalleX, results from several parallel applications have exhibited dramatic scaling characteristics through advanced flow control methods. The implications for a future HPC paradigm will be considered that may enable Exascale computing by the end of this decade.

**Biography:** Dr. Thomas Sterling holds the position of Professor of Informatics and Computing at the Indiana University (IU) School of Informatics and Computing as well as serving as Chief Scientist and Associate Director of the PTI Center for Research in Extreme Scale Technologies (CREST). He also is an Adjunct Professor at the Louisiana State University (LSU) and CSRI Fellow at Sandia National Laboratories. Since receiving his Ph.D from MIT in 1984 as a Hertz Fellow Dr. Sterling has engaged in applied research in fields associated with parallel computing system structures, semantics, and operation in industry, government labs, and academia. Dr. Sterling is best known as the "father of Beowulf" for his pioneering research in commodity/Linux cluster computing. He was awarded the Gordon Bell Prize in 1997 with his collaborators for this work. He was the PI of the HTMT Project sponsored by NSF, DARPA, NSA, and NASA to explore advanced technologies and their implication for high-end system architectures. This three-year project involved a dozen institutions and 50 researchers to investigate superconducting logic, holographic storage, optical networks, and Processor-In-Memory components. Other research projects included the DARPA DIVA PIM architecture project with USC-ISI, the Cray Cascade Petaflops architecture project sponsored by the DARPA HPCS Program, and the Gilgamesh high-density computing project at NASA JPL. Thomas Sterling is currently engaged in research associated with the ParalleX advanced execution model for extreme scale computing. This work is to devise a new model of computation establishing the foundation principles to guide the co-design for the development of future generation Exascale computing systems by the end of this decade. His research has been conducted through several projects sponsored separately by DOE, NSA, DOD, NSF, DARPA, NASA and Microsoft. Dr. Sterling is the co-author of six books and holds six patents.

**Please contact Prof. HJ Siegel ([H.J.Siegel@colostate.edu](mailto:H.J.Siegel@colostate.edu)) with any questions.**