ECE102 - Digital Circuit Logic - spring 2021

Instructor: Prof. Mahdi Nikdast (http://www.engr.colostate.edu/~mnikdast/)
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Teaching Assistants: Ms. Gunjan Mahindre, Mr. Febin Sunny, and Mr. Shreyas Shende

(Please see the Schedule pdf file on Canvas for all the office hours and Zoom links)

Lectures: Tuesday, Thursday 12:30 - 13:45. Online from January 19th

Labs: https://www.engr.colostate.edu/ECE102/Spring21/labs.html

Objectives: To understand the concepts of digital logic and learn methods and tools for the design of digital circuits.

Prerequisites: Major in ECE or prior approval.

URL: The official home page for ECE102 is Canvas. Students are expected to visit the official home page frequently for class handouts, homework assignments, lab assignments, and important announcements!

Grading Policy: The grade will be based on

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<tbody>
<tr>
<td>Homework (Every week)</td>
<td>25%</td>
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<tr>
<td>Labs (13 in total)</td>
<td>25%</td>
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<tr>
<td>Midterm 1 (February 25, 2021)</td>
<td>15%</td>
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<tr>
<td>Midterm 2 (April 8, 2021)</td>
<td>15%</td>
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<tr>
<td>Final Exam (May 12, 2021)</td>
<td>20%</td>
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The +/- grading scheme will be used, with the scale

<table>
<thead>
<tr>
<th>Grade</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>&gt;95%</td>
<td>90-94%</td>
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<tr>
<td>90-89%</td>
<td>85-84%</td>
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<tr>
<td>80-79%</td>
<td>75-74%</td>
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<tr>
<td>70-69%</td>
<td>65-64%</td>
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<tr>
<td>60-59%</td>
<td>55-54%</td>
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<tr>
<td>&lt;50%</td>
<td>40-49%</td>
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Homework Procedures: Homework assignments are due online (must be submitted on Canvas). Selected questions from each homework assignment will be graded. However, turn in ALL of the assigned problems. All assigned problems are equally important for the development of your understanding of subjects of digital logic. To receive full credit for your homework, show ALL reasonable steps in solving the problem. Written solutions will be available online after the due date of the homework. Make sure the file you submit to Canvas is readable, otherwise the course grader may NOT grade your assignment.

Late Policy: Quizzes and Exams must be taken as scheduled in order to receive credit. Late homework will NOT be accepted unless its lateness is due to circumstances beyond your control.
(official proof is required). To receive full credit, lab reports must be submitted online through Canvas on/before the date due. Late lab reports will be accepted, but points will be deducted from the score (see penalties below).

**Lab Assignments and Attendance:** Laboratory assignments are a very important component of this course. You will learn to design and develop digital logic circuits, and by the end of the semester, will be able to design sophisticated digital circuits. We use a set of digital tools used by professional engineers, which may appear a bit intimidating at first. After the first two to three labs, you will become comfortable with the tools and will be on your way to designing some interesting circuits.

- You must pass EVERY lab assignment with score > 60% to pass the course.
- Lab board (online students): Online students can purchase the board required in the lab (DE0-CV FPGA Board (Part Number P0192)) from the following sources: terasic.com and Digi-Key Electronics (If purchased from terasic.com, students can qualify for academic pricing). Students in in-person lab sessions will receive the lab board (do NOT purchase online).
- Lab attendance (online and in-person): Highly Encouraged. In rare situations when you cannot attend your scheduled lab session due to circumstances beyond your control, you must obtain clearance in advance from your lab instructor (TA). In such a case, you can attend another lab section during that same week ONLY IF YOU GET APPROVAL FROM YOUR TA. Remember that all lab projects must be completed with a passing grade in order to pass the course (i.e., >60%).
- Conduct in the lab: Students are expected to maintain a professional working atmosphere in the lab (online and in-person), which includes not disturbing other students or groups, not talking loudly, and following additional instructions provided by Teaching Assistants. Use of cellphones (for voice or texting) is not allowed. No food or drinks allowed in C207. TAs are responsible to report any misconduct or unprofessional behavior to the instructor for further actions.
- Prelab: Prelabs should be checked at the beginning of corresponding lab sessions. This prelab must be included in your lab reports every week.
- Demonstration of hardware circuits & Submitting Project reports: You may submit the hardware demo any time before the start date of the next project for your lab section (Please see Lab Demo Instructions on Canvas). All the lab demos must be submitted online through YouTube (please see the Demo Instructions).
- Policy on collaboration with other students: Design alone, build alone, write alone, and submit individually prepared reports and circuits. It is fine to talk, give advice, receive advice, but do your own work.
- Grading policy: The grading differs from one lab project to the other. An example would be: hardware circuit: 30%, required technical items in the report: 40%, memo text: 20%, instructor discretion: 10%. A neatness bonus of 5% may be assigned.
- Penalties: Penalties will be assessed for each lab report (except where specifically allowed): -5% for missing prelab, -2.5%-per-day for late submission, and -10% for not following Banana memo format.
**Conduct and Nature of Exams:** You will be allowed to use one double-sided page of notes, prepared by you, during the three exams. Exams will be straightforward BUT will demand the kind of preparation only possible through continual, daily study.

**Instructional Objectives:** Given during class, these are the bases of all exam questions and homework assignments. For this reason, **consistent class attendance is very important.**

**Textbook:** Fundamentals of Logic Design, by Charles H. Roth published by Cengage Learning. The latest is the 7th Edition. Sixth, fifth or fourth editions are acceptable. Some of these earlier editions were published by Thompson Publishing Co. Be aware that there are differences in chapter, page and problem numbers of the different editions. CSU Bookstore carries a paperback version containing the necessary chapters of the 7th edition at a lower price compared to the regular version. It is not critical to have the text during the first week.

**Tutoring:** The course's Graduate Teaching Assistants (TAs) will be available for drop-in consultation as well as help sessions at times listed on the website.

**Academic Integrity:** This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (http://www.conflictresolution.colostate.edu/academic-integrity) and the Student Conduct Code (http://www.conflictresolution.colostate.edu/conduct-code). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services. **My policy is that of zero tolerance.** Minor first infraction in HWs and Lab reports will lead to a zero score (-40% for Lab assignments) as well as one letter level (e.g., A to B) reduction in the course grade. Project or Major or repeated infractions in HWs and Lab reports will result in “F” grade for the course as well as reporting to the Dean’s Office. Any misconduct in an exam (e.g., cheating) will lead to a zero score for that exam, and very likely, course failure.

All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one’s own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken.

**Diversity Statement:** As the instructor in ECE102, I am deeply committed to helping build an inclusive culture in this classroom, in the Department of Electrical and Computer Engineering, in the Walter Scott, Jr. College of Engineering, and at CSU. Each individual brings diversity to our class in the identities they hold, the ways they think, their interests and skills, their background and past experiences. To me, inclusion means not only accepting these differences, but embracing them and understanding that we can leverage these differences to be better engineers.

My goal for this class is to create an environment where we do not discriminate against individuals because of their identities (e.g., race, ethnicity, sex, gender identity, sexual orientation, religion, nationality, age, levels of ability). It is also important to understand that even when we hold
egalitarian beliefs, we can hold implicit or unconscious biases that can also influence the way we treat others or approach engineering design. It is my expectation that students in this class will:

1. Adhere to the CSU Principles of Community https://diversity.colostate.edu/principles-of-community/;
2. Work in teams in ways that recognize the contributions of all team members and provide all team members the opportunity to learn;
3. Examine their own behaviors and refrain from acting in biased ways;
4. Reflect on the ways bias can influence engineering work;
5. Speak with the professor when biased behaviors may occur from other students, their TAs, and the professor;
6. Be sensitive to context and acknowledge that hurtful comments can sometimes be inadvertent but they still have an impact.

Important information for students: All students are expected and required to report any COVID-19 symptoms to the university immediately, as well as exposures or positive tests from a non-CSU testing location. If you suspect you have symptoms, please fill out the COVID Reporter (https://covid.colostate.edu/reporter/). If you know or believe you have been exposed, including living with someone known to be COVID positive, or are symptomatic, it is important for the health of yourself and others that you complete the online COVID Reporter. Do not ask your instructor to report for you. If you do not have internet access to fill out the online COVID-19 Reporter, please call (970) 491-4600. You will not be penalized in any way for reporting. If you report symptoms or a positive test, you will receive immediate instructions on what to do, and CSU’s Public Health Office will be notified. Once notified, that office will contact you and most likely conduct contact tracing, initiate any necessary public health requirements and/or recommendations and notify you if you need to take any steps.

For the latest information about the University’s COVID resources and information, please visit the CSU COVID-19 site: https://covid.colostate.edu/.
**Topics** (Dates/Topics may change with reasonable notice):

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<tr>
<th>Week</th>
<th>Course Objectives</th>
<th>Readings</th>
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<tr>
<td>W1 (Jan. 19 – Jan. 22) <strong>Delivery: Online+Live</strong></td>
<td>Introduction to ECE102 and digital systems - State the differences between analog and digital systems</td>
<td>N/A</td>
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<td>W2 (Jan. 25 – Jan. 29) <strong>Delivery: Online+Live</strong></td>
<td><strong>Binary representation of information</strong> - Define the term “positional number system” - Represent numbers in decimal, binary, octal and hexadecimal notations and convert from one notation to the other - Add, subtract, multiply and divide binary numbers - Represent numbers in sign-magnitude, one's complement and two's complement forms - Carry out addition and subtraction, and identify overflow conditions - Represent numbers in binary coded decimal format (BCD) - Represent characters using ASCII format</td>
<td>Ch. 1</td>
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<td>W3 (Feb. 1 – Feb. 5) <strong>Delivery: Online+Live</strong> W4 (Feb. 8 – Feb. 12) <strong>Delivery: To be Confirmed!</strong></td>
<td><strong>Boolean Algebra and Combinational Logic</strong> - Define the basic logic operations (AND, OR, NOT) - Evaluate Boolean expressions - Derive the logic function implemented by a combinational logic circuit - Use Laws and Theorems of Boolean Algebra to simplify logic expressions - Find the complement of a Boolean expression using DeMorgan's Law - Find the dual of a Boolean expression - State and use the Negative Logic Theorem - Use Consensus theorem to simplify logic expressions - Implement Boolean expressions using 2-level networks (SOP, POS)</td>
<td>Ch. 2</td>
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<td>- Convert functional specifications (written in English) to logic expressions - Convert specifications written in English to a truth table - Write a logic expression as a minimum POS, minimum SOP, canonical POS and a canonical POS - Design logic circuits to add/subtract two's complement numbers - Obtain minterm and maxterm expansions (using m/M notations or in algebraic form) from a truth table or an algebraic expression</td>
<td>Ch. 3</td>
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<td>W5 (Feb. 15 – Feb. 19)</td>
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<td>Ch. 4</td>
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<td>Week</td>
<td>Topics</td>
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| W6 (Feb. 22 – Feb. 26) | - Convert a minterm expansion it a maxterm expansion and vice versa  
- Use m/M notation to obtain product/sum of logic expressions  
- Find the minterm and maxterm expansions of $F'$, $F.G$, $F+G$ where $F$, $G$ are Boolean functions  
- Hardware for Arithmetic  
- Design logic circuits to add/subtract two's complement numbers  
- Design an array multiplier for binary integers |
| W7 (Mar. 1 – Mar. 5)  
W8 (Mar. 8 – Mar. 12) | - Use don't care terms to simplify logic expressions  
- Represent 3,4,5 and 6 variable functions using K-maps  
- Represent expressions given in SOP, POS, maxterm or minterm form on K-maps  
- Obtain minimum POS and SOP expansions using K-map  
- Design multiple output circuits using K-maps  
- Represent 5 and 6 variable functions using K-maps and obtain minimum SOP, POS |
| W9 (Mar. 15 – Mar. 19)  
W10 (Mar. 22 – Mar. 26) | **Sequential Circuits**  
- Describe the operation of S-R, T, D, and J-K latches and flip-flops  
- Draw timing diagrams of circuits containing latches and flip-flops  
- Draw the circuit diagram, and describe the operation of registers, shift registers, cyclic shift registers, etc. |
| W11 (Mar. 29 – Apr. 2)  
W12 (Apr. 5 – Apr. 9) | **Midterm 2 (April 8, 2021)**  
- Analyze Moore and Mealy type sequential networks, i.e., given a sequential circuit, |

Midterm 1 (February 25, 2021)  

Ch. 5  

Ch. 7  

Ch. 8  

Ch. 9  

Ch. 11  

Ch. 12  

Ch. 13  

Ch. 14
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<tr>
<th>Week</th>
<th>Dates</th>
<th>Activities</th>
<th>Ch. 15</th>
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| W13  | Apr. 12 – Apr. 16 | Derive the state graphs/ state tables of a given sequential circuit  
|      |              | Draw timing diagrams corresponding to given input waveforms  
|      |              | Derive Moore and Mealy type state diagrams to meet given specifications  
|      |              | Synthesize Moore & Mealy circuits to meet given specifications using D, T, J-K and/or S-R flip-flops |        |
|      |              | **Break – No Class/Labs**                                                                  |        |
| W14  | Apr. 19 – Apr. 23 | Identify equivalent states and reduce state diagrams to minimum number of states  
|      |              | Determine whether two state diagrams are equivalent  
|      |              | Use Alphanumeric Notation in state graphs  
|      |              | Verilog                                                                                      |        |
| W15  | Apr. 26 – Apr. 30 | Review                                                                                       |        |
| W16  | May 3 – May 7  | **Final Exam**  
|      |              | Wednesday – May 12, 2021  
|      |              | 9:40 AM to 11:40 AM                                                                     |        |