ECE571/ECE757 VLSI System Design and Experiments

Instructor: Steve Undy
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Objectives

ECE 571 is a senior level as well as an entry level graduate three credit lecture course on VLSI design. ECE 575 is the corresponding one credit lab course required to be taken concurrently. The purpose of these courses is to provide students with opportunities to learn and practice the entire process of VLSI chip design. There is a substantial amount of design work associated with the lectures and labs. Students will go through various design stages from logic and circuit design and simulation to layout and design verification. All the design activities will be carried out using Cadence design tools. Up to 4 design labs are scheduled concurrent with the lectures. Students are required to submit a design report and to participate in design reviews.

Prerequisites

Students are required to have taken EE451 and have sufficient knowledge about logic design. Some knowledge about high-level language programming is desirable.

Course Outline

Week	Topic
1	**Introduction, MOS transistors**
2	**MOS transistors**
3	**CMOS Layout. CMOS Fabrication.**
4	**CMOS Fabrication. Delay and Optimization**
5	**Delay and Optimization**
6	**Delay and Optimization. Power**
7	**Power. Interconnect**

8	**Interconnect. Midterm**
9	**Combinational Logic**
10	**Combinational Logic. Sequential Logic, Timing Analysis and Metastability**
11	**Sequential Logic, Timing Analysis and Metastability**
12	**Sequential Logic, Timing Analysis and Metastability. Clocking and Clock Systems**
13	**Robustness. Test, Debug and Verification**
14	**Test, Debug and Verification**
15	**Review**

Textbook and Additional Readings

All the lectures are based on the lecture notes from the instructor. The following are books that students can use for additional references.

- “Principles of CMOS VLSI Design” by N. Weste.

Grading Policy

The breakdown of grades for ECE 571 and ECE 575 is as follows:

- Final Exam 35% (ECE 571)
- Midterm 20% (ECE 571)
- Homework 15% (ECE 571)
- Class participation and quizzes 5% (ECE 571)
- Labs & Design Project 25% (ECE 575)

ECE 571 and ECE 575 will have grades reported separately.

Instructor’s Office Hours

Office Hours: Typically immediately following class.

TA’s Office Hours

The TA for this course is Lekha Rane, lekha.rane@colostate.edu. She will be in charge of the ECE 575 labs. For her office hours please contact her via email first and set up an appointment.