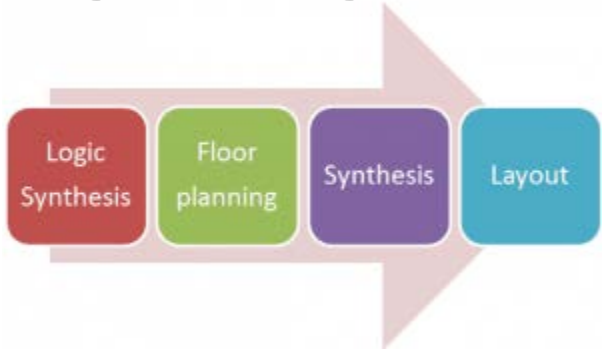
Digital Logic Synthesis – ECE480A4



Instructor: Prof. Mahdi Nikdast (E-mail: Mahdi.Nikdast@colostate.edu).

Office Hours: Tuesday: 2:30 pm – 3:30 pm; Thursday: 4:00 pm – 5:00 pm; and walk-in subject to availability. Office: C103A Engineering Building.

Course Assistant: Yash Chopra (E-mail: Yash.Chopra@colostate.edu). Office hours: Friday 11:00 am – 12:00 pm at Room 10, Engineering Building.

Lectures: Tuesday and Thursday, 8:00 am – 9:15 am, Room B2, Engineering.

Course Summary

What is Logic Synthesis?

Logic synthesis is the process of converting a high-level description of design (usually defined using a hardware description language) into an optimized gate-level representation. Logic synthesis uses a standard cell library which have simple cells, such as basic logic gates like and, or, and nor, or macro cells, such as adder, muxes, memory, and flip-flops.

Course Description

This course educates students on how to extract gate-level circuits from high-level hardware description languages (HDL) and apply top-down design methodology to optimize the designs to achieve better power, performance, timing, and area. Advanced concepts in logic optimization, simulation and testing, and synchronous and asynchronous circuits, as well as a comprehensive review of HDL will be covered.

Course Learning Objectives

Here is a summary of ECE480A4 learning objectives:
1) Study hardware description language (HDL) and extract gate-level circuits from high-level hardware description languages;
3) Explore electronic design automation (EDA) solutions for the design and optimization of digital systems;
2) Study and Apply design optimization methods (e.g., top-down design methodologies to optimize the designs) to digital systems;
3) Study two-level and multi-level logic synthesis;
4) Examine and study timing analysis, physical design, physical synthesis, test, and verification.

Course Textbook and Materials

- Instructor will provide notes and slides during each lecture;
- **Textbook:** G. D. Hachtel and F. Somenzi, Logic Synthesis and Verification Algorithms. ISBN: ISBN-13: 978-0387310046.
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Course Logistics and Grading Policy

Homework Assignments	40%
In-Class Quiz and Activities	10%
Midterm Exam I	15%
Midterm Exam II	15%
Final Exam	20%

The +/- grading scheme will be used, with the following scale

>95%	90 – 94%	85 – 89%	80 – 84%	75 – 79%	70 – 74%	65 – 69%	55 – 64%	40 – 54%	<40%
A+	A	A-	B+	B	B-	C+	C	D	F

Homework Assignments Procedure, Submission Policy

Homework Assignments: To receive full credit for your homework, show all reasonable steps in solving problems. All the homework assignments should be uploaded electronically on Canvas.
Late Submission Policy: Late homework **will not be accepted** unless the lateness is due to circumstances beyond your control **(official proof [e.g., medical note] is required)**.

Instructions to submit your files: All the submitted files should be in PDF format on Canvas.

Academic Integrity

This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (http://www.conflictresolution.colostate.edu/academic-integrity) and the Student Conduct Code (http://www.conflictresolution.colostate.edu/conduct-code). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services. All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one's own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken. My policy is that of **zero tolerance**. Minor first infraction in HWs and presentations will lead to a zero score as well as one letter level (e.g. A to B) reduction in the course grade. Project or Major or repeated infractions in HWs and presentations will result in "F" grade for the course as well as reporting to the Dean's Office.

Diversity Statement

As the instructor in ECE480A4, I am deeply committed to helping build an inclusive culture in this classroom, in the Department of Electrical and Computer Engineering, in the Walter Scott, Jr. College of Engineering, and at CSU. Each individual brings diversity to our class in the identities they hold, the ways they think, their interests and skills, their background and past experiences. To me, inclusion means not only accepting these differences, but embracing them and understanding that we can leverage these differences to be better engineers.

My goal for this class is to create an environment where we do not discriminate against individuals because of their identities (e.g., race, ethnicity, sex, gender identity, sexual orientation, religion, nationality, age, levels of ability). It is also important to understand that even when we hold egalitarian beliefs, we can hold implicit or unconscious biases that can also influence the way we treat others or approach engineering design. It is my expectation that students in this class will:

1. Adhere to the CSU Principles of Community https://diversity.colostate.edu/principles-of-community/;
2. Work in teams in ways that recognize the contributions of all team members and provide all team members the opportunity to learn;
3. Examine their own behaviors and refrain from acting in biased ways;
4. Reflect on the ways bias can influence engineering work;
5. Speak with the professor when biased behaviors may occur from other students, their TAs, and the professor;
6. Be sensitive to context and acknowledge that hurtful comments can sometimes be inadvertent but they still have an impact.

Topics (Dates/Topics may change with reasonable notice. Important dates are in **red**)

Week	Lecture Topics	HW
W1 (Jan. 21)	Introduction to Logic Synthesis	
W2 (Jan. 28)	Summary of Boolean Algebra	
W3 (Feb. 4)	HDL (Verilog) Free Online Course (50 minutes) from Intel (Click here). MIT Course on HDL (Click Here).	
W4 (Feb. 11)	Quine-McCluskey Method	
W5 (Feb. 18)	Binary Decision Diagram	
W6 (Feb. 25)	Satisfiability Part I	
W7 (March 3)	Satisfiability Part II; **Midterm I**	
W8 (March 10)	MiniSat	
W10 (March 24)	Two-Level Logic Synthesis	
W11 (March 31)	Multi-Level Logic Synthesis Part I	
W12 (April 7)	Introduction to Espresso; **Midterm II**	
W13 (April 14)	Multi-Level Logic Synthesis Part II	
W14 (April 21)	DC Extraction	
W15 (April 28)	Technology Mapping	
W16 (May 5)	Physical Synthesis	
May 13, 2020 (2 pm to 4 pm)	**Final Exam**	