ECE450/451 Course Syllabus

Objectives: ECE451 is a senior level course on digital design techniques. The purpose of this course is to provide students with opportunities to learn different digital systems and their practical applications, and various design techniques for different types of digital systems. Because this is a course related to designing hardware, a great deal of emphasis will be paid to practical issues in designing digital systems which combines both the software and hardware skills in a top-down design flow. Practical design issues can be understood only by going through a set of extensive design experiments in ECE450 both in the form of software programming at a higher level of design hierarchy and in the form of hardware building and debugging at a lower level of design hierarchy. The behavioral level design of a digital system is often performed using hardware description languages (HDLs) such as Verilog. Students taking this course will learn how to use Verilog to describe behavior and functionalities of any complex digital systems. The gate level implementation of a digital system is mapped to a field programmable gate array device for verification. Therefore, students will go through the entire design process of describing hardware using software languages, mapping it into gates and simulating the gate level design, and finally load the schematic design on to a silicon chip to verify the functionality of the system in hardware.

Prerequisites and Corequisites: Students are required to have taken ECE102 and ECE202 and have a grade better than C in both classes. Having sufficient knowledge about high-level language programming in C, Java, or C++ will be a plus. Students MUST register ECE450 together with ECE451. ECE450 is the lab component of the ECE451.

URL: The official home page for ECE450/451 is **Canvas**. **Students are expected to visit the official home page frequently for class handouts, homework assignments, lab assignments, and important announcements!** Student must follow Modules (left-hand-side tab on Canvas) every week. Each module includes lectures and a lab session and some assignments. We expect to complete one module per week.

Textbook: The textbook for ECE451 is "Contemporary Logic Design" by Randy H. Katz. The reference books for additional reading are:

- Digital Design, Principles and Practices" by John Wakerly.
- Digital Design Fundamentals" by Kenneth J. Breeding, Prentice-Hall, 1992.
- Computation Structures" by S.A. Ward and R.H. Halstead Jr., McGraw-Hill, 1990.
- Logic Synthesis" by Srinivas Devadas et. al., McGraw-Hill, 1994.

Grading Policy: The grade will be based on

Homework (**Almost every week**)	25%
Labs (**8 in total**)	30%
Online Quizzes (Zoom and Canvas)	10%
Midterm (**Oct. 29, 2020**)	15%
Final Exam (**Dec. 17, 2020**)	20%

The +/- grading scheme will be used, with the scale

>95%	90-94%	85-89%	80-84%	75-79%	70-74%	65-69%	55-64%	40-54%	<40%
A+	A	A-	B+	B	B-	C+	C	D	F

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Topics: Following is a tentative course outline. It is subject to change depending on progress in class instruction and the design project.

Week	Course Objectives	Readings	LAB
W1 (Aug. 24 – Aug. 28) W2 (Aug. 31 – Sep. 4)	Review of basic logic design, number systems, and basic logic families	Chapters 1, 2, 3	LB1-W2
W3 (Sep. 7 – Sep. 11)	Introduction to Verilog/VHDL and design tools	-	-
W4 (Sep. 14 – Sep. 18) W5 (Sep. 21 – Sep. 25)	Design of combinational logic	Chapters 4 and 5	LB2-W4 LB3-W5
W6 (Sep. 28 – Oct. 2) W7 (Oct. 5 – Oct. 9)	Design and optimization of sequential logic state machines	Chapters 7 and 8	LB4-W7
W8 (Oct. 12 – Oct. 16) W9 (Oct. 19 – Oct. 23)	Examples of some sequential logic circuits and their implementation	Chapters 9, 10, 11	LB5-W9
W10 (Oct. 26 – Oct. 30)	Midterm Exam	-	LB6-W10
W11 (Nov. 2 – Nov. 6)	Introduction to programmable logic devices (PLDs)	-	-
W12 (Nov. 9 – Nov. 13)	Implementing combination logic with PLDs	Chapter 6	LB7-W12
W13 (Nov. 16 – Nov. 20)	Arithmetic logic	-	-
W14 (Nov. 23 – Nov. 27)	Break		
W15 (Nov. 30 – Dec. 4)	Design of data path logic	-	LB8-W15
W16 (Dec. 7 – Dec. 11)	Design of control logic	-	-

LAB Topics:

LB1. Three-Bit ALU (Cadence)
LB2. Three-Bit ALU (Verilog)
LB3. Subway Signal Control Logic (Cadence)
LB4. Blinkenlights (Cadence and Verilog)
LB5. Grey Code Counter (Cadence)
LB6. Pulse Clock and Pyramid Counter (Verilog)
LB7. Subway Signal Control Logic II (Cadence)
LB8. Finite State Machines - Traffic Light Controller (Cadence & Verilog)

Online Quizzes: During the online lectures (and mostly at the beginning of each lecture), there will be several **online questions using polling function in Zoom**. **These quizzes cover the material taught on the same day of the lecture OR to review materials delivered in the previous lecture. Therefore, it is very important to attend the online lectures to take part in online quizzes, which account for 10% of the final course grade.**

Homework Procedures: Homework assignments are due online (**must be submitted on Canvas**). Turn in **ALL** of the assigned problems. All assigned problems are equally important for the development of your understanding of the subjects of digital system design. To receive full credit for your homework, show **ALL** reasonable steps in solving the problem. Written solutions might be available in the lab/online after the due date of the homework. **Make sure the file you submit to Canvas is readable, otherwise the course grader may NOT grade your assignment.**

Late Policy: Quizzes and Exams must be taken as scheduled in order to receive credit. Late homework will **NOT** be accepted unless its lateness is due to circumstances beyond your control (**official** proof is required). To receive full credit, lab reports **must be submitted online through Canvas** on/before the date due. Late lab reports will be accepted, but points will be deducted from the score (see penalties below).

Lab Assignments and Attendance: Laboratory assignments are a very important component of this course. You will learn to design and develop digital circuits and systems, and by the end of the semester, will be able to design sophisticated digital circuits. We use a set of digital tools used by professional engineers, which may appear a bit intimidating at first. After the first two to three labs, you will become comfortable with the tools and will be on your way to designing some interesting circuits.

- **You must pass EVERY lab assignment with score > 50% to pass the course.**
- **Lab attendance: Mandatory**. In rare situations when you cannot attend your scheduled lab session due to circumstances beyond your control, you must obtain clearance in advance from your lab instructor. In such a case, you must attend another lab section during that same week. Failing that, you will be marked absent for the project and will receive a penalty (-10%). Remember that all projects must be completed with a passing grade in order to pass the course **(i.e., >50%)**.
- **Conduct in the lab:** Students are expected to maintain a professional working atmosphere in the lab, which includes not disturbing other students or groups, not talking loudly, and following additional instructions provided by the Teaching Assistants. **Use of cellphones (for voice or texting) is not allowed. No food or drinks allowed in C105/C107. TAs are responsible to report any misconduct or unprofessional behavior to the instructor for further actions. You MUST follow CSU policies on safety regulations during COVID-19.**
- **Demonstration of hardware circuits & Submitting Project reports:** You may show the hardware demo any time before the start date of the next project for your lab section (during GTA's office hours or during other lab sections). At the time of the demo, you must present your circuit diagram built using Cadence software. Your lab instructor will confirm this

diagram once she/he has seen your hardware circuit working correctly. The circuit diagram should then be incorporated into your project report. Demonstrating your hardware circuit during the next lab meeting is permitted, but make sure that it works flawlessly. You will not be given extra time to debug your circuit at that time. **No excuses will be entertained in this regard.**

- **Policy on collaboration with other students:** Design alone, build alone, write alone, and submit individually prepared reports and circuits. It is fine to talk, give advice, receive advice, but do your own work.
- **Grading policy:** The grading differs from one project to the other. An example would be—hardware circuit: 30%, required technical items in the report: 40%, memo text: 20%, instructor discretion: 10%. A neatness bonus of 5% may be assigned.
- **Penalties:** Penalties will be assessed for each lab report (except where specifically allowed): -10% for not attending the lab session, and -2.5%-per-day for late submission.

Conduct and Nature of Exams: You will be allowed to use one double-sided page of notes, prepared by you, during the three exams. Exams will be straightforward but will demand the kind of preparation only possible through continual, daily study.

Academic Integrity: This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (http://www.conflictresolution.colostate.edu/academic-integrity) and the Student Conduct Code (http://www.conflictresolution.colostate.edu/conduct-code). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services**. My policy is that of zero tolerance.** Minor first infraction in HWs and Lab reports will lead to a zero score (-50% for Lab assignments) as well as one letter level (e.g., A to B) reduction in the course grade. Project or Major or repeated infractions in HWs and Lab reports will result in "F" grade for the course as well as reporting to the Dean's Office. Any misconduct in an exam (e.g., cheating) will lead to a zero score for that exam, and very likely, course failure.

All submitted work should be your own. Copying of language, structure, images, ideas, or thoughts of another, and representing them as one's own without proper acknowledgement (from web sites, books, papers, other students, solutions from previous offerings of this course, etc.) and failure to cite sources properly is not acceptable. Sources must always be appropriately referenced, whether the source is printed, electronic, or spoken.

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Diversity Statement: As the instructor in ECE450/451, I am deeply committed to helping build an inclusive culture in this classroom, in the Department of Electrical and Computer Engineering, in the Walter Scott, Jr. College of Engineering, and at CSU. Each individual brings diversity to our class in the identities they hold, the ways they think, their interests and skills, their background and past experiences. To me, inclusion means not only accepting these differences, but embracing them and understanding that we can leverage these differences to be better engineers.

My goal for this class is to create an environment where we do not discriminate against individuals because of their identities (e.g., race, ethnicity, sex, gender identity, sexual orientation, religion, nationality, age, levels of ability). It is also important to understand that even when we hold egalitarian beliefs, we can hold implicit or unconscious biases that can also influence the way we treat others or approach engineering design. It is my expectation that students in this class will:

1. Adhere to the CSU Principles of Community https://diversity.colostate.edu/principles-of-community/;
2. Work in teams in ways that recognize the contributions of all team members and provide all team members the opportunity to learn;
3. Examine their own behaviors and refrain from acting in biased ways;
4. Reflect on the ways bias can influence engineering work;
5. Speak with the professor when biased behaviors may occur from other students, their TAs, and the professor;
6. Be sensitive to context and acknowledge that hurtful comments can sometimes be inadvertent, but they still have an impact.