1. ECE 580B4: FPGA Signal Processing/Software-Defined Radio

2. 3 credits: 2-75 minute lecture sessions/week

3. Jesse Wilson

4. Digital Signal Processing with Field Programmable Gate Arrays (Signals and Communication Technology. Meyer-Baese, W. 2014.

5. Course Information
    a. Theory, design principles, and implementation of digital signal processing algorithms on FPGA devices, and their applications ranging from telecommunications to scientific equipment
    b. Prerequisites: ECE 312; ECE451
    c. Selected Elective: Electrical Engineering; Computer Engineering

6. Goals for the Course
    a. Course Learning Objectives
        i. Distinguish FPGA vs microprocessor-based DSP implementation, explain tradeoffs between them, and select an architecture by weighing power consumption, bandwidth, and development effort considerations
        ii. Identify and explain consequences of analog/digital conversion of radio-frequency signals, such as aliasing and effective bit gain from oversampling
        iii. Distinguish and select between and fixed-point and floating-point arithmetic, depending on design objectives, and utilize IEEE math libraries to implement basic operations in either format
        iv. Construct and test in Verilog or VHDL the basic signal processing components: Numerically-controlled oscillator (NCO), mixers, finite- and infinite-impulse response filters (FIR, IIR), adaptive filters, and cascaded integrator-comb downsampling and upsampling (CIC) filters
        v. Explain the Fast-Fourier Transform, identify how its implementations on an FPGA differs from on a DSP microprocessor, and construct it in Verilog or VHDL
        vi. Configure and make use of commercially-available intellectual property (IP) blocks to speed up DSP implementation
        vii. Configure and integrate on-chip soft CPU to reduce development time of functionality better suited to microprocessors (e.g. configuration, control, serial communications)
        viii. Design and build all the digital elements of a basic communications system, including amplitude modulation of an NCO-generated carrier, transmission through a simulated channel, and demodulation with a digital downconverter (DDC)
        ix. Engage in continued learning beyond this course, to be able to design and implement FPGA-based DSP systems with more sophisticated components (e.g. wavelets, spread-spectrum coding, real-time video processing)

b. Student Outcomes
    1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
    3. An ability to communicate effectively with a range of audiences
    5. An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
    6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
    7. An ability acquire and apply new knowledge as needed, using appropriate learning strategies

7. Topics Covered

FPGA technology, VHDL/Verilog review, FPGA vs DSP processors, analog/digital conversion basics, aliasing, oversampling bit gain, number representation, computer arithmetic, multiply-accumulator, CORDIC and numerically-controlled oscillators

FIR theory review, filter design techniques, VHDL/Verilog implementation, IP core usage, adaptive filter theory, LMS algorithm and adaptive update of FIR coefficients

IIR theory review, filter design techniques, VHDL/Verilog implementation, IP core usage, finite wordlength effects (roundoff and saturation), timing closure and maximum sample rate, techniques for speeding up IIR filters

CIC filter theory, decimation, interpolation, CIC passband structure aliasing and distortion, compensation filters

Discrete Fourier transform review, Cooley-Tukey algorithm, Good-Thomas algorithm, Winograd algorithm, Verilog/VHDL implementation, IP core usage

Digital-to-analog and analog-to-digital converters, modulation, demodulation, digital downconverter architecture, coherent vs incoherent demodulation

Microprocessor IP cores (e.g. Altera NIOS, Xilinx MicroBlaze), I/O and data transfer, UART and serial communications