An Outlier Detection Based Approach for PCB Testing with Principal Component Analysis

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This work is sponsored by
Agilent Technologies

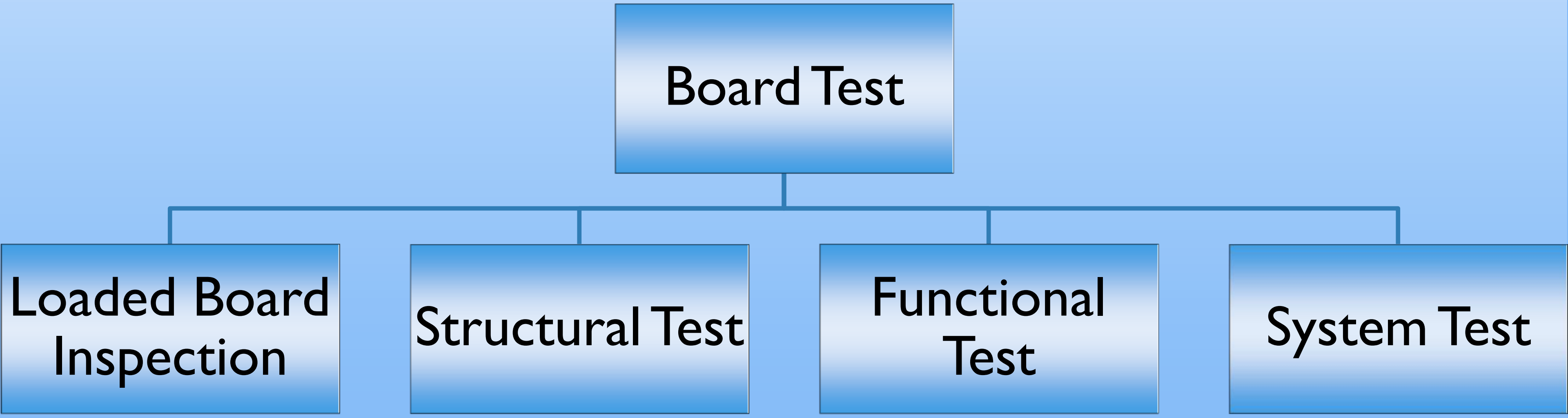
Contribution

- Identifying outlier board/connector measurements
  - Novel approach for board measurements analysis
  - Test window for finer analysis
  - Performance evaluation
- Detect and compensate for systematic variation of measurement data
  - Compensation with regression lines and difference values
  - Compensation and detection with PCs

Outline

- Board Test
  - Capacitive Lead Frame Testing
- PCA Based Outlier Detection
- Global Analysis
- Localized Analysis
- Comparison with Traditional Outlier Detection method
- Mechanical Variation Compensation
- Summary and Future Work

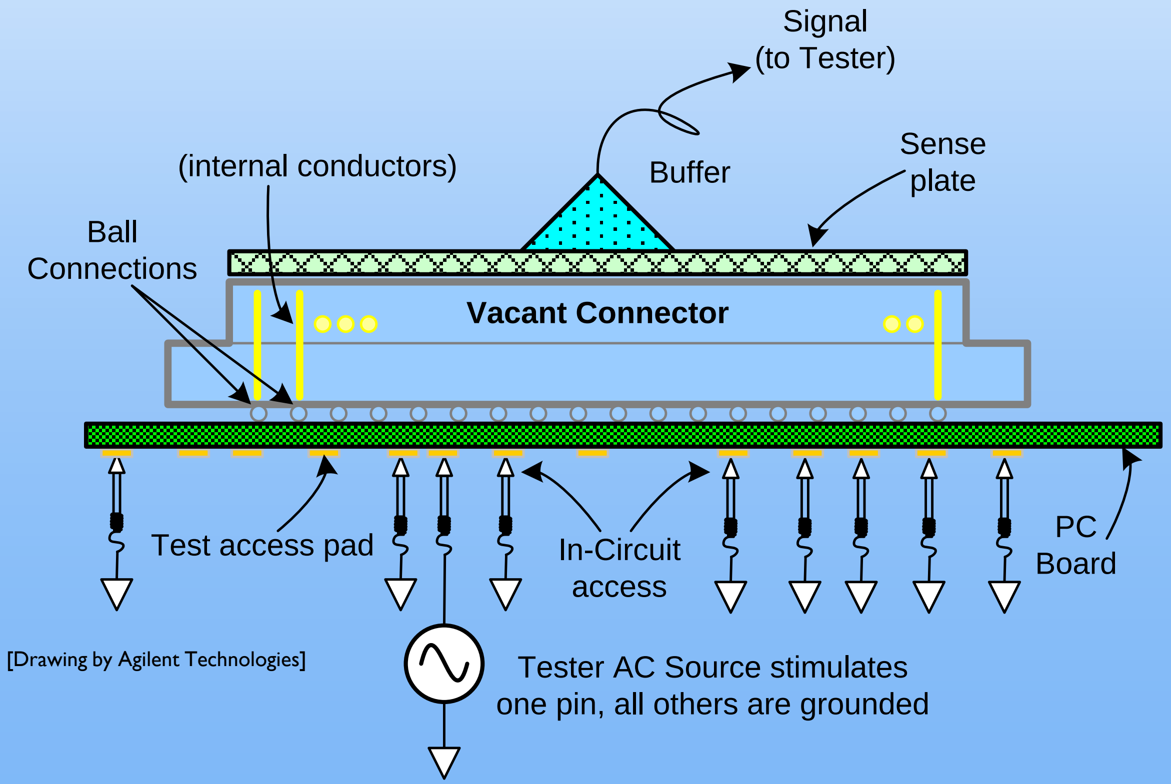
Board Test Categories



Structural Test:

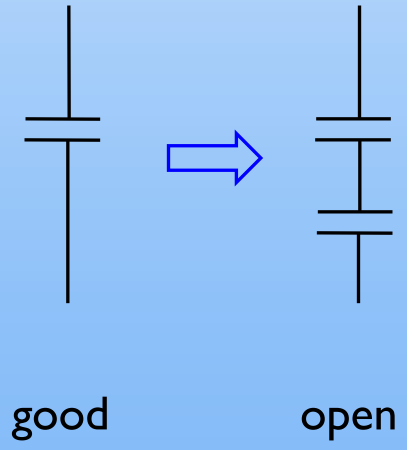
- In-Circuit-Test (ICT)
  - Powered Test: Digital , Mix-signal..
  - Unpowered Test: Short test, TestJet …

Capacitive Lead Frame Testing



[Drawing by Agilent Technologies]

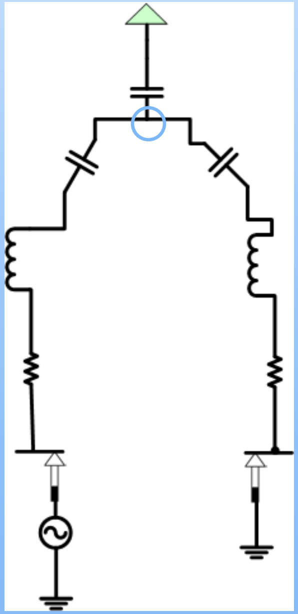
Tester AC Source stimulates
one pin, all others are grounded



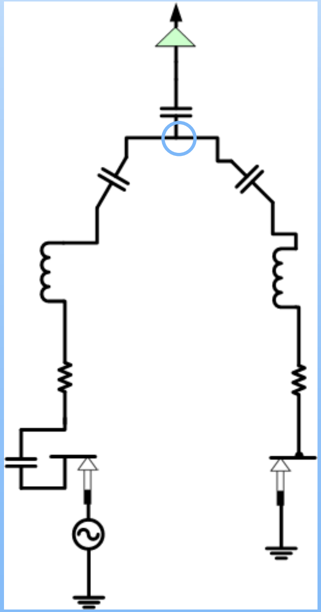
- Capacitance formed between tested pin and sense plate
- Open defect on tested pin affects the normal signal level

Ref: Parker, Hird ITC 2007

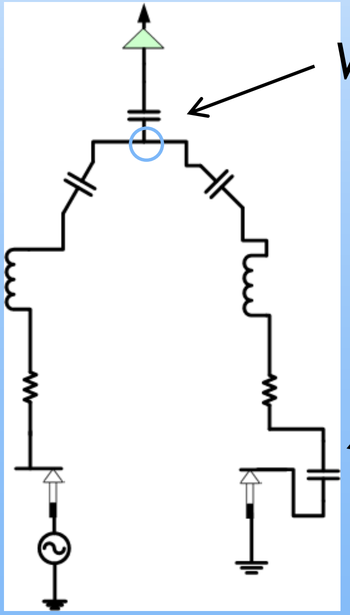
Capacitive Lead Frame Testing



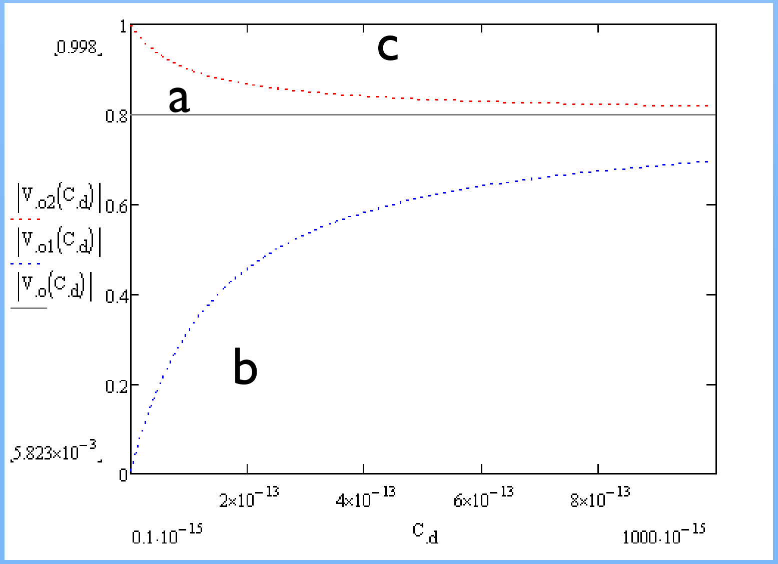
(a)
Non-defective pin



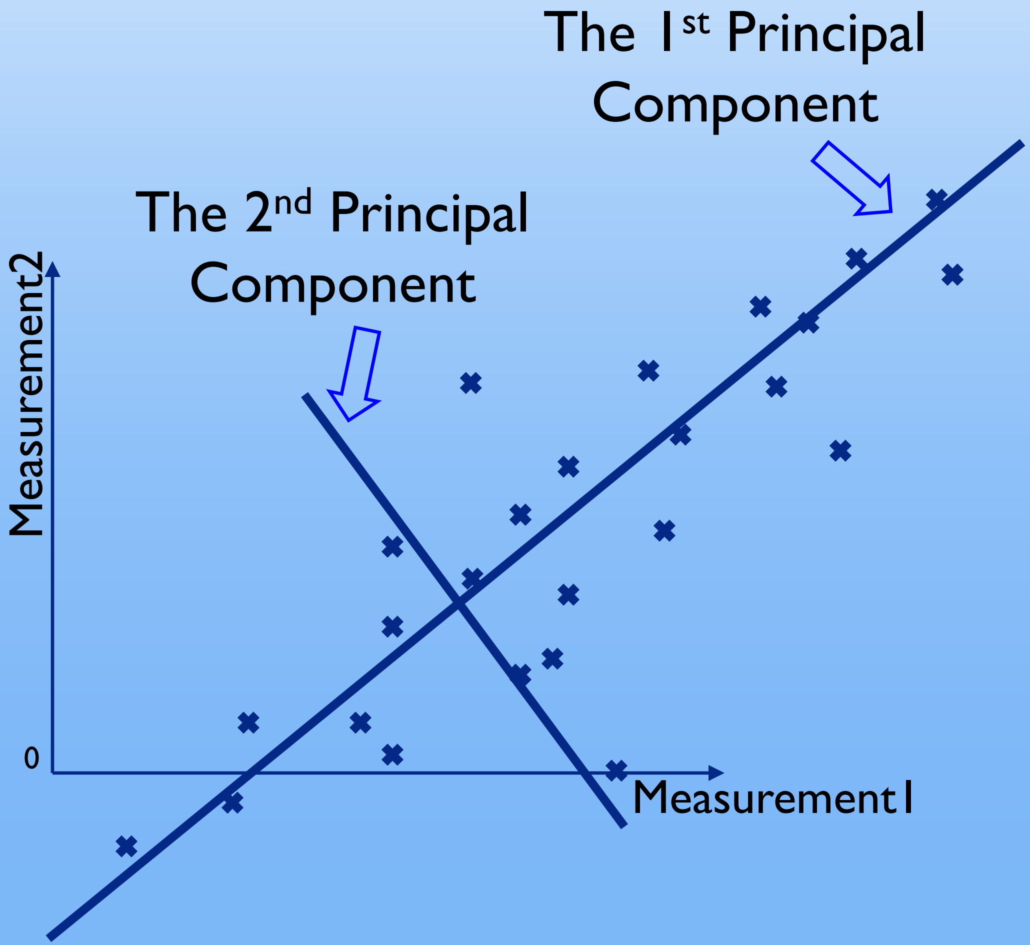
(b)
Opened Tested pin



(c)
opened neighbor pin

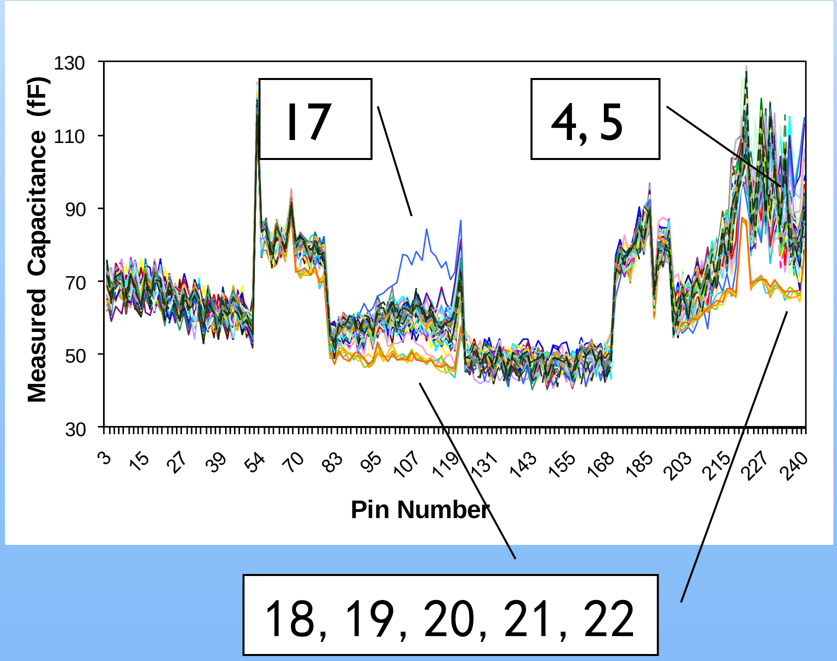


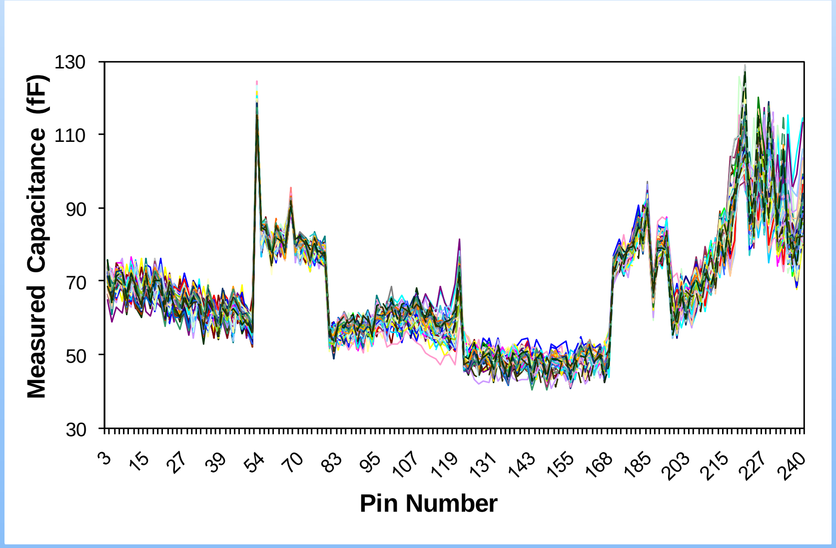
Principal Component Analysis (PCA)



- ❑ 1st Principal Component contains largest variance from the data projection
- ❑ 2nd Principal Component is orthogonal to the 1st one, contains second largest projected variance
- ❑ Is good at analyzing multi-dimensional interrelated data

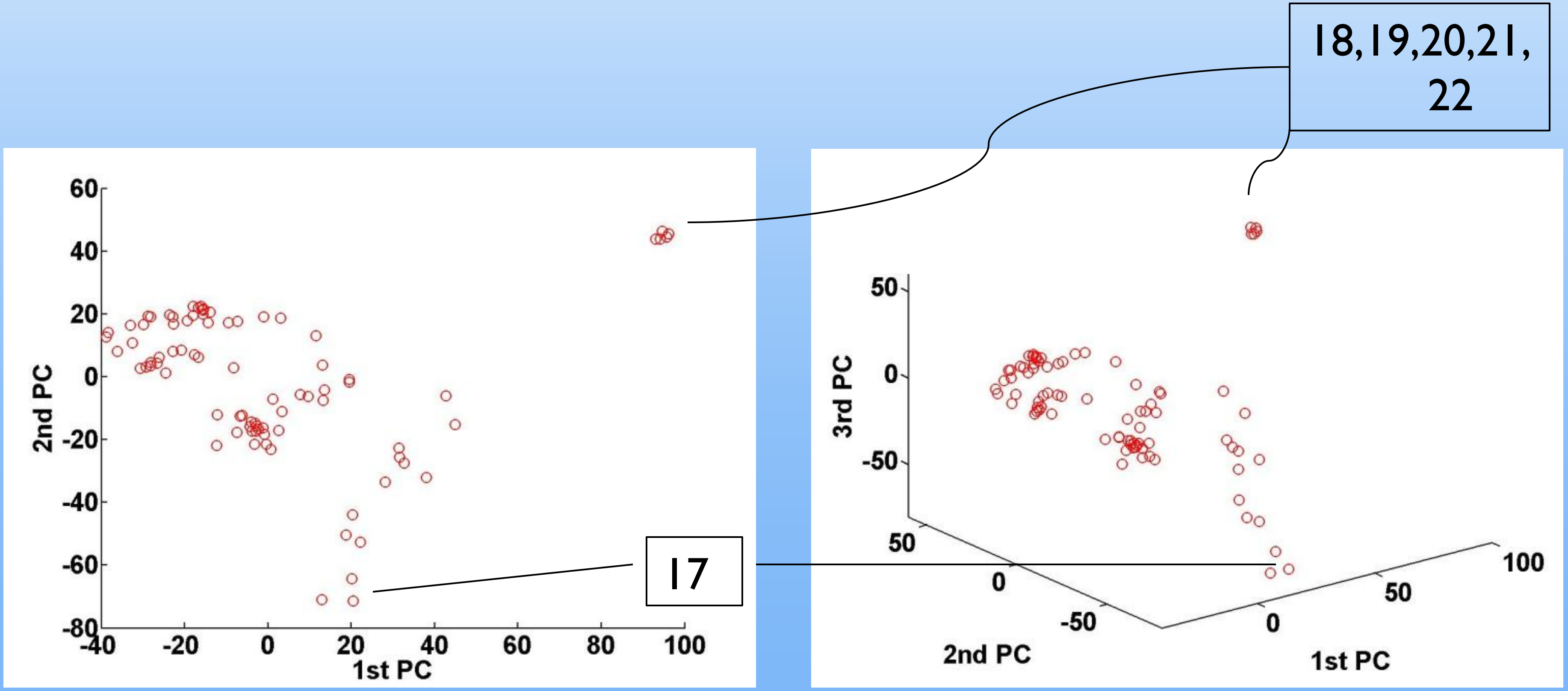
Measurement Analysis (Data_j24)





- ❑ Total 83 board measurements (Boardruns)
- ❑ Clear outliers: 17, 18, 19, 20, 21, 22
- ❑ Potential outlier: 4, 5, 14 ,15……

Single Connector Analysis



18,19,20,21,
22

17

PCA for PCB Outlier Detection

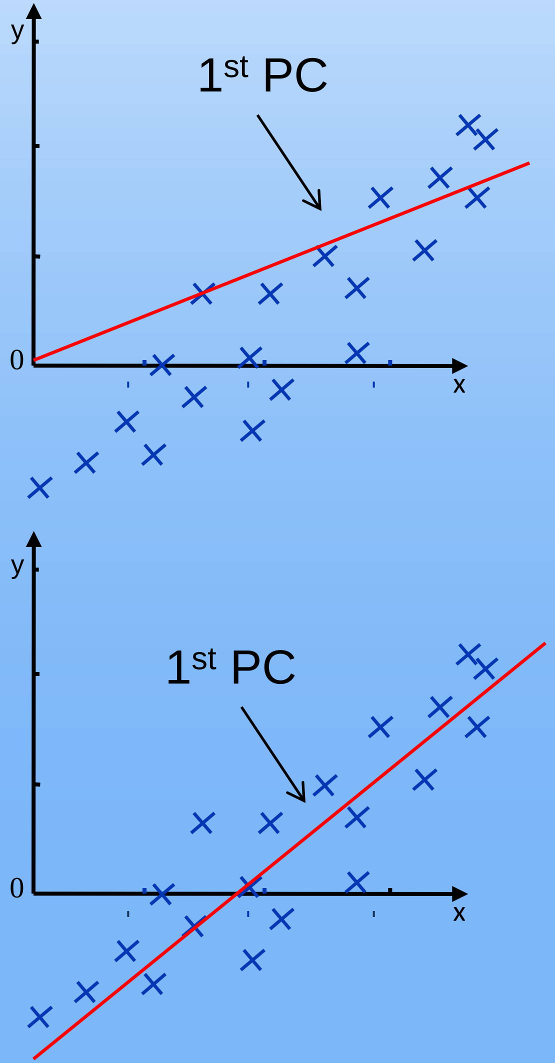
Let M be (mxn) matrix of Capacitive Lead Frame Testing measurements

- m is the number of boards
- n is number of tested pins per board

$$M \Rightarrow M_c$$

$$\begin{pmatrix} x_{11} & \dots & x_{1n} \\ \dots & & \dots \\ \dots & \dots & \\ x_{m1} & \dots & x_{mn} \end{pmatrix} \Rightarrow \begin{pmatrix} x_{11} - \dfrac{\sum_{k=1}^{n} x_{k1}}{n} & \dots \\ \dots & \dots \\ \dots & \\ x_{n1} - \dfrac{\sum_{k=1}^{n} x_{k1}}{n} & \dots \end{pmatrix}$$

Centering



PCA for PCB Outlier Detection

Using the Singular Value Decomposition $\boldsymbol{M_c = USV^T}$

where

U_{mxn} Scaled version of PC scores

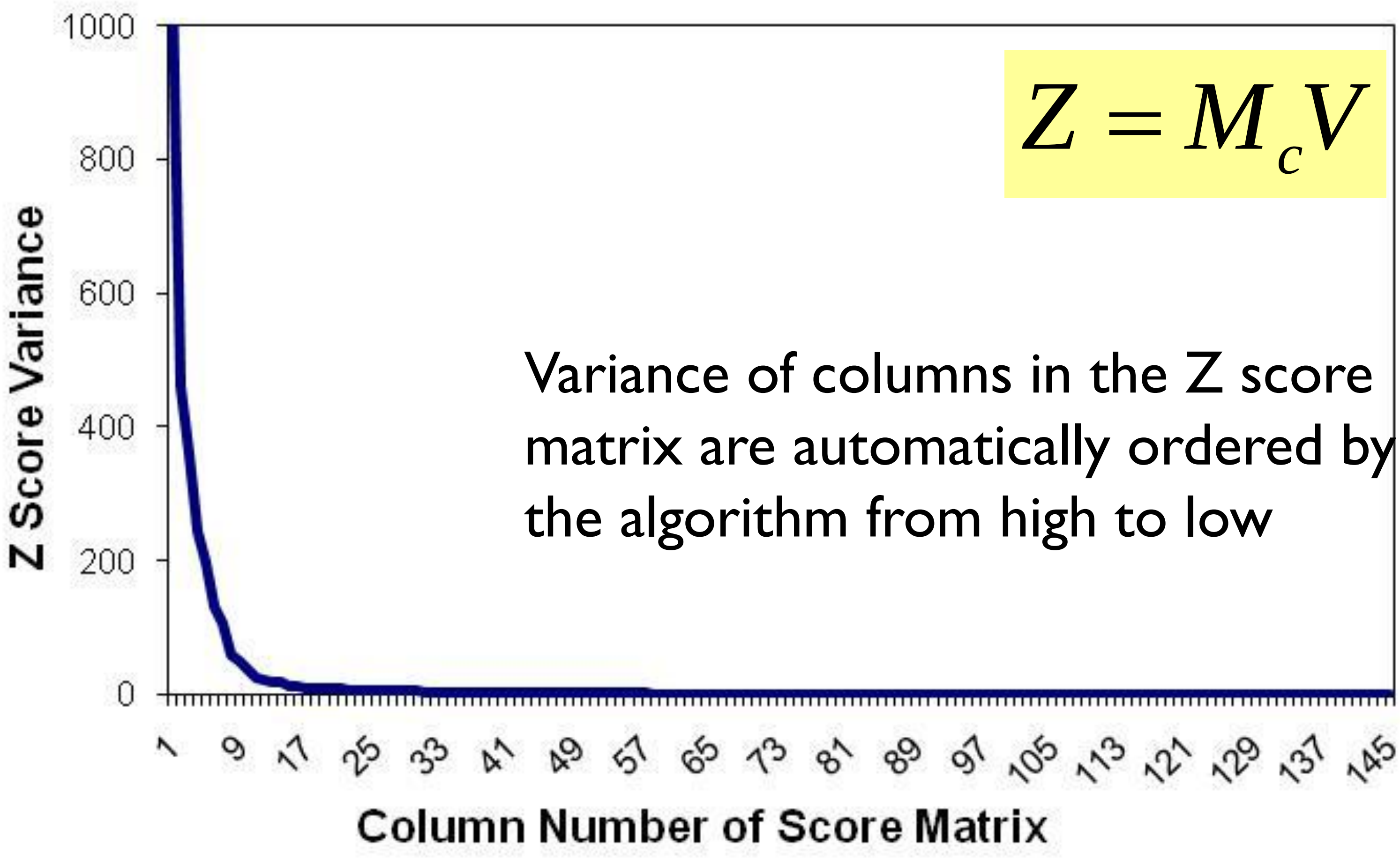
S_{nxn} Diagonal matrix with square roots of Eigen values in descending order

$\mathrm{V^T}_{\mathrm{nxn}}$ Eigen vectors (PCs). V is the transformation matrix

Matrix $\boldsymbol{Z = M_c V}$ gives the z-score value of boards

Z-score value of a board is a linear combination of all the corresponding measurement values for that board

PCA for PCB Outlier Detection



$$Z = M_c V$$

Variance of columns in the Z score matrix are automatically ordered by the algorithm from high to low

Test Statistics

$$d_{1i}^2 = \sum_{k=p-q+1}^{q} z_{ik}^2$$

p : the sequence number of the last PC used

q : the amount of PCs selected

$$d_{2i}^2 = \sum_{k=p-q+1}^{p} \frac{z_{ik}^2}{l_k} \quad \Rightarrow \quad d_0^2 = \sqrt{\sum_{k=1}^{p} \frac{z_{ik}^2}{l_k}}$$

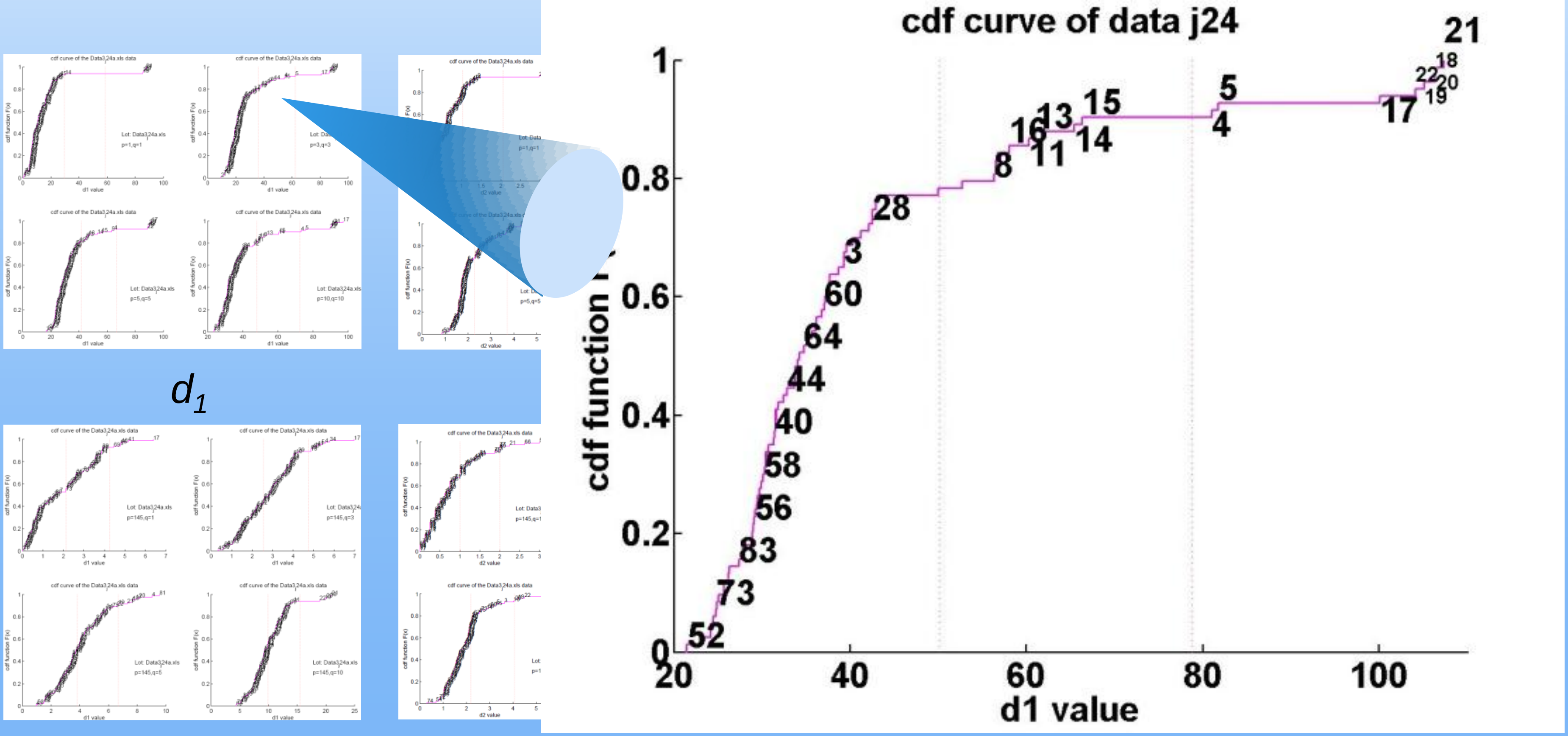
$$d_{3i}^2 = \sum_{k=1}^{p} l_k z_{ik}^2$$

$$d_{4i} = \max_{p-q+1 \le k \le p} \left| \frac{z_{ik}}{\sqrt{l_k}} \right| \quad \Rightarrow \quad X_i = \log 10\left(\max_{p-q+1 \le k \le p} \left| \frac{z_{ik}}{\sqrt{l_k}} \right| \right)$$

Measurement Outlier Analysis with Test statistic

- Test statistics calculation with Principal Components from data set.
- Board measurements are sorted according to the respective d value.
- The outlier boards should stand out at the high-end of the Cumulative Distribution Function curve in d scale.

Statistics & p, q Value Selection



Board run numbers on CDF plot from left to right:
52,51,50,53,49,32,***73***,24,48,25,74,72,***83***,71,57,47,1,42,***56***,70,6,68,38,37,***58***,43,59,41,39,55,***40***,2,23,78,33,35,***44***,69,79,54,75,36,***64***,*80*,76,31,77,65,***60***,29,81,63,61,62,***3***,67,66,82,27,45,***28***,46,26,30,34,12,***8***,7,10,9,***16***,***11***,***13***,***14***,***15***,***4***,***5***,***17***,***22***,***19***,***18***,***20***,***21***

Test Statistic for Outlier Detection

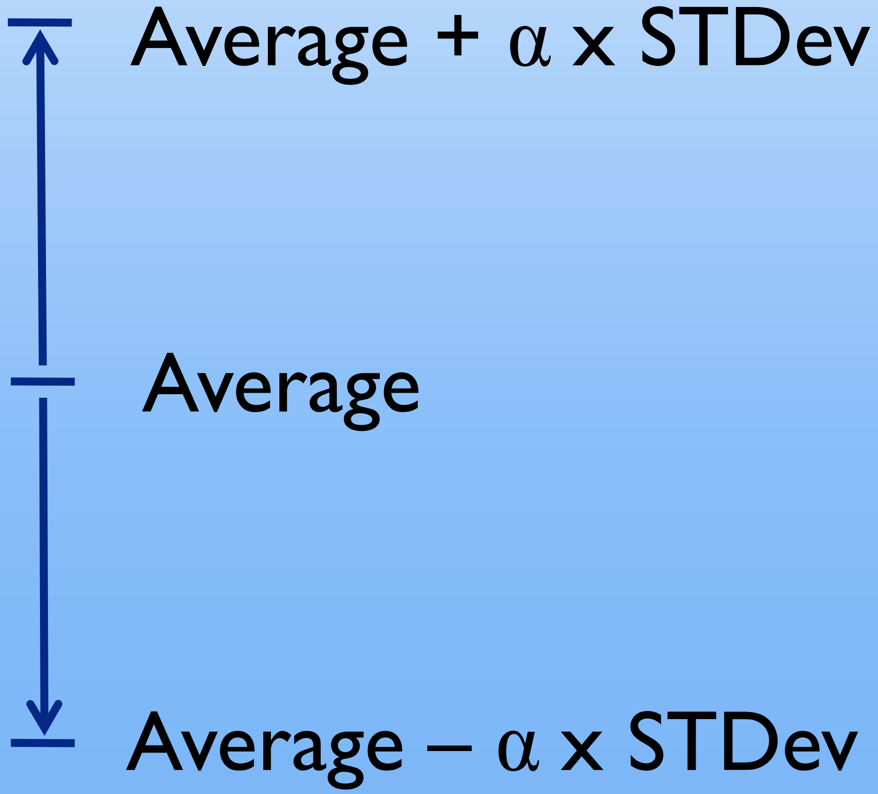
$$d_{1i} = \sqrt{\sum_{k \in E} z_{ik}^{2}}$$

Z_{ik} :Value of the *k*-th PC for *i*-th board

E : a subset of PCs - most significant PCs are used here

- Sort the boards with respect to d_1
- Plot cumulative distribution function (CDF) of d_l
- Outliers are clearly identifiable on right side of plot, and typically are separated from other devices by a clear margin

PCA vs. Standard Deviation (STDev)



Average + α x STDev

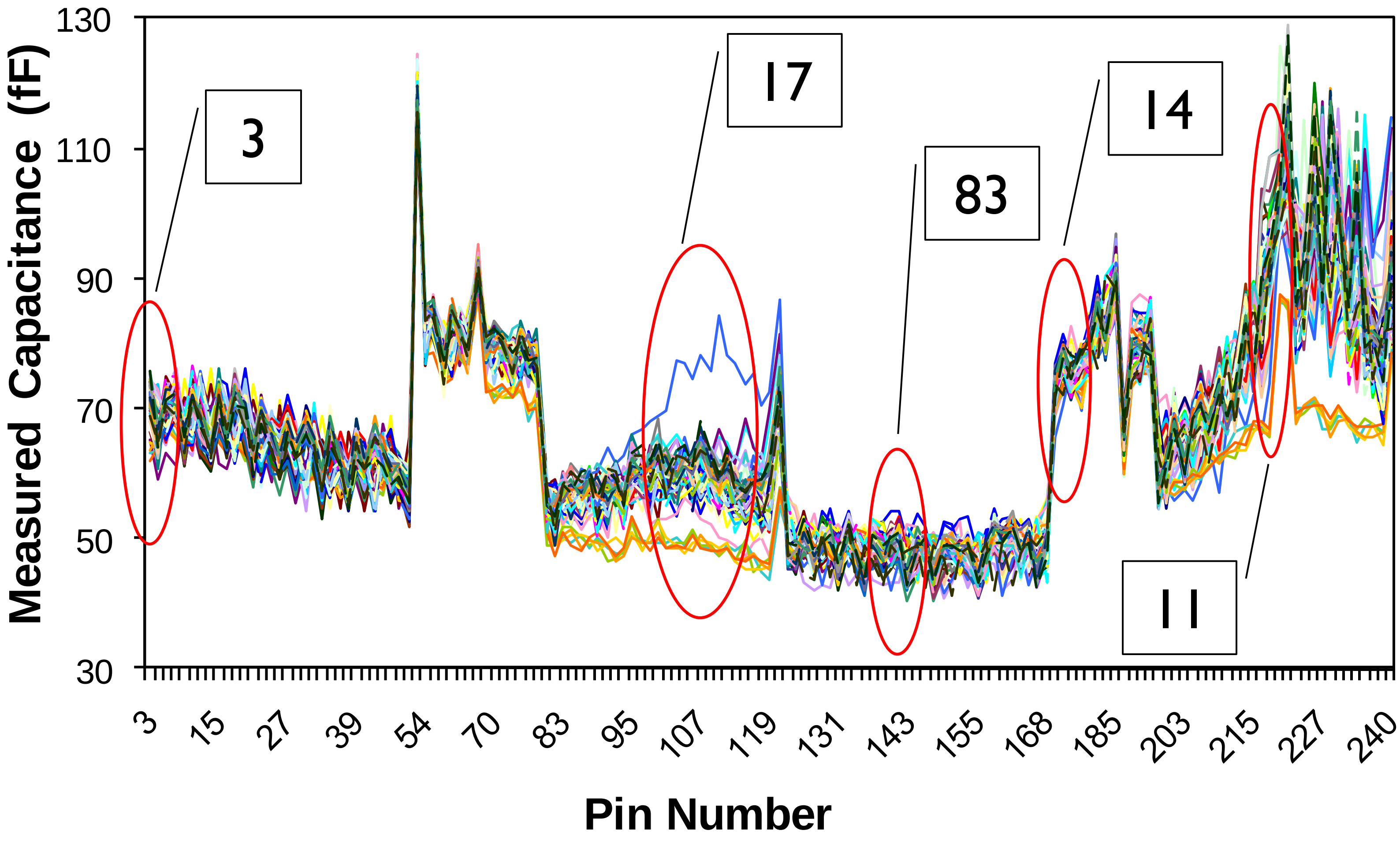
Average

Average – α x STDev

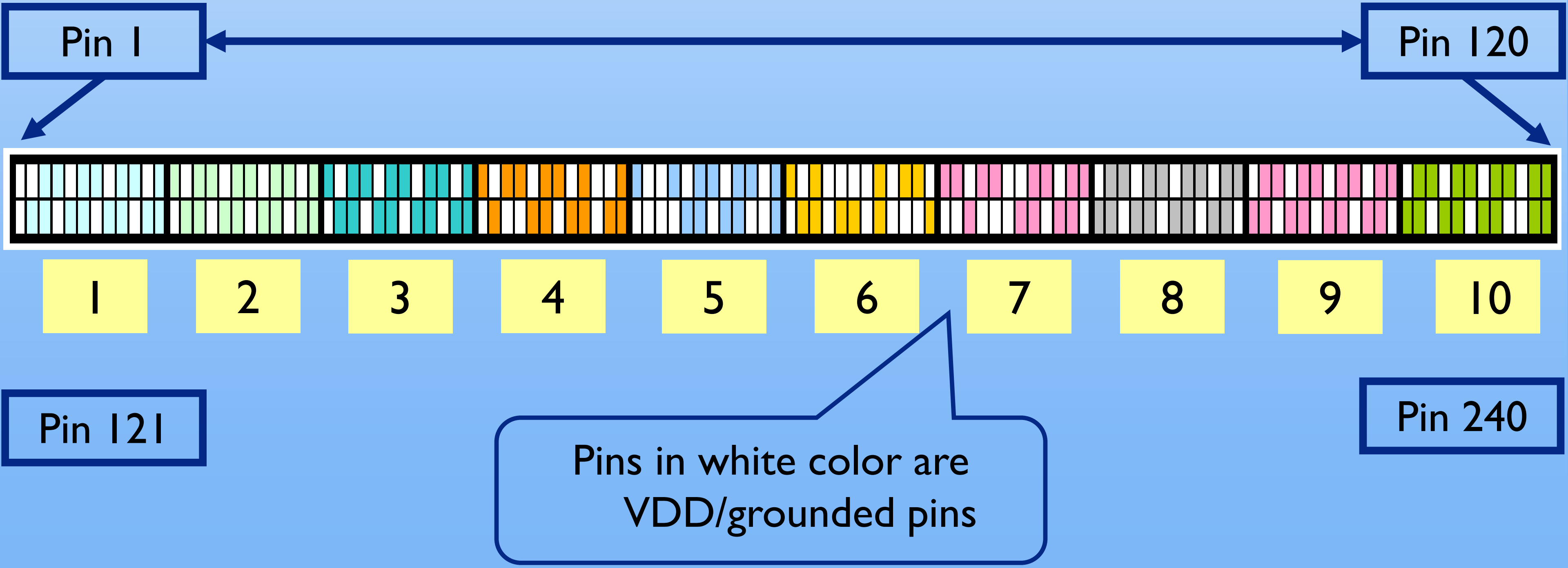
PCA vs. Standard Deviation (STDev)

α	Abnormal Boardruns Detected	Boardruns No.
6	0	
5.5	1	17
5	1	17
4.5	2	14, 17
4	5	3,11,14,17,83
3.5	11	3,4,5,6,8,11,14,15,17,59,83
3	18	3,4,5,6,8,9,11,14,15,16,17,18,19,20,21,51,59,83
2.5	35	3,4,5,6,7,8,9,11,12,13,14,15,16,17,18,19,20,21,22,34,36,47,48,51,53,57,58,59,60,63,68,73,80,81,83

PCA vs. Standard Deviation (STDev)



Localized Analysis



Pin 1

Pin 120

1

2

3

4

5

6

7

8

9

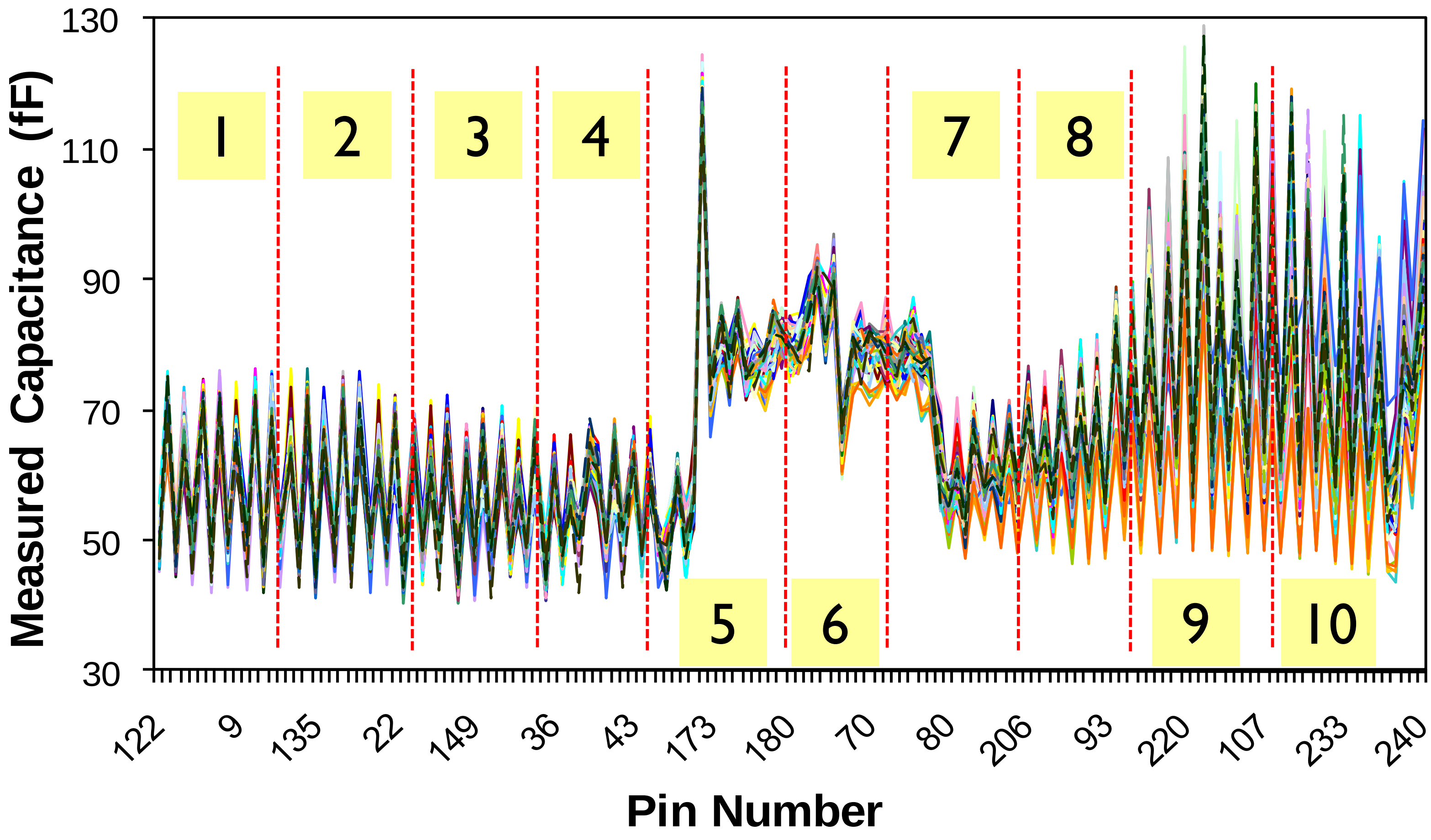
10

Pin 121

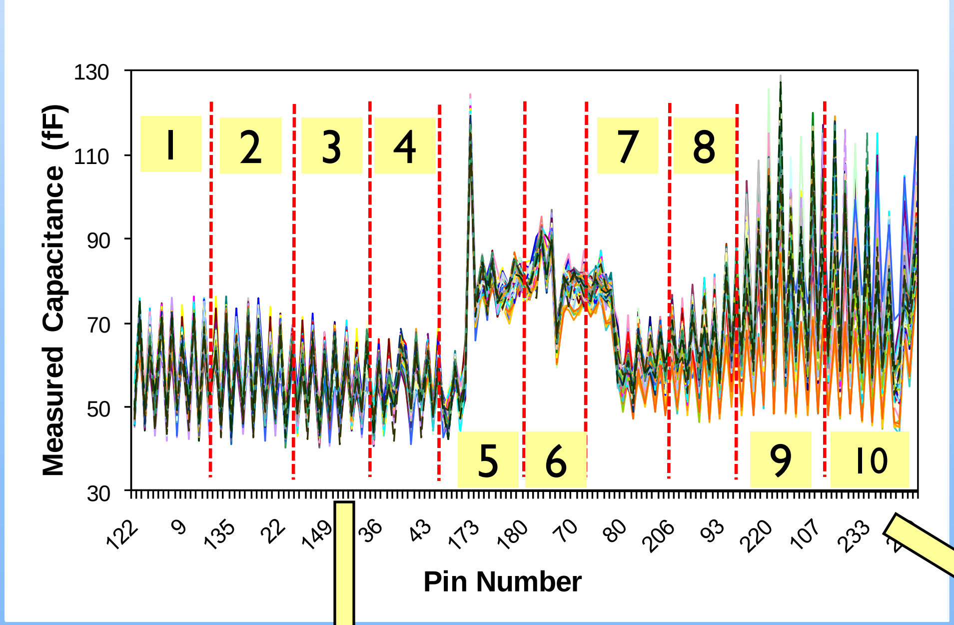
Pin 240

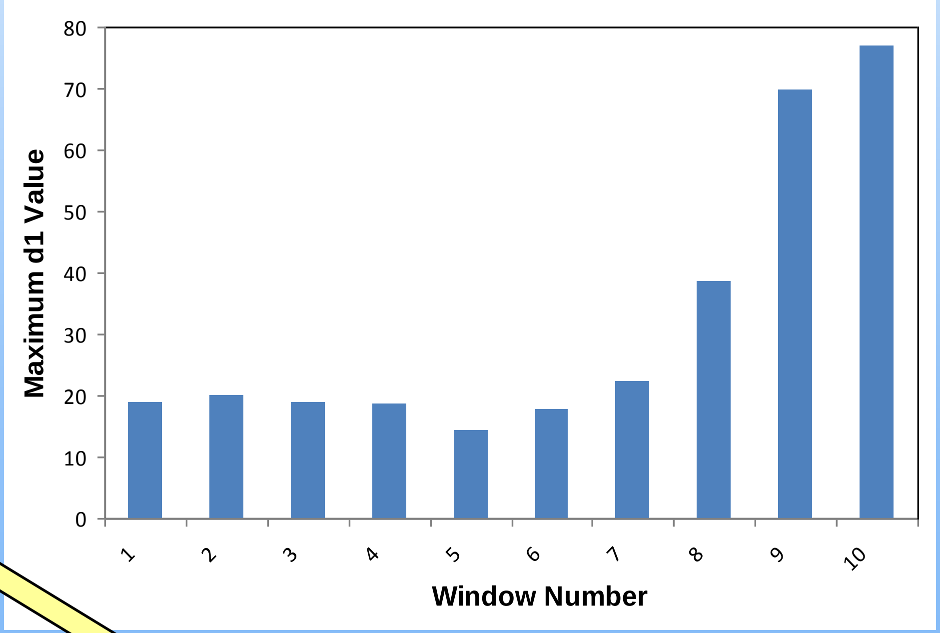
Pins in white color are VDD/grounded pins

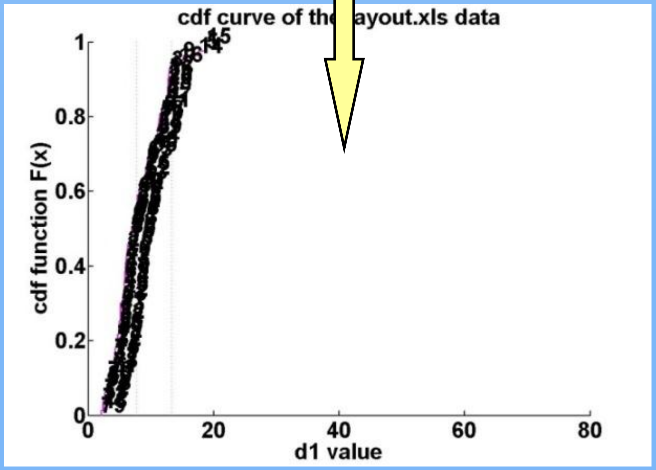
Test Windows (Data_ j24)



Localized Analysis







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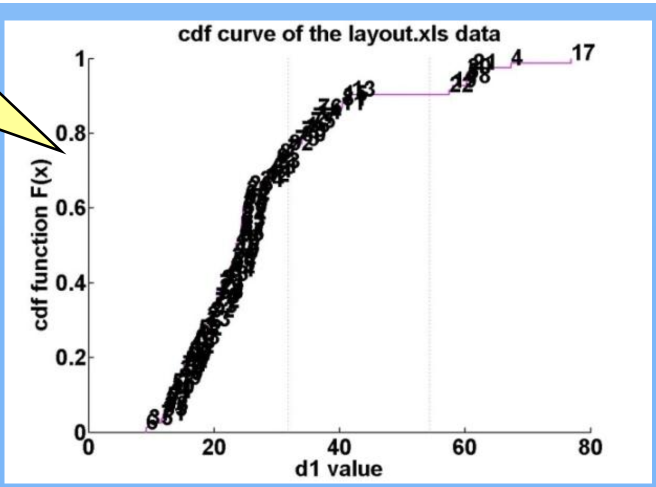
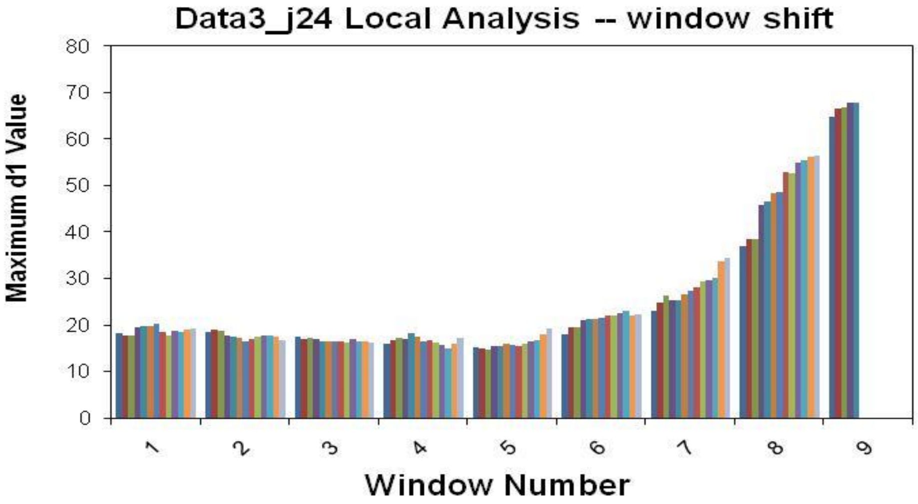
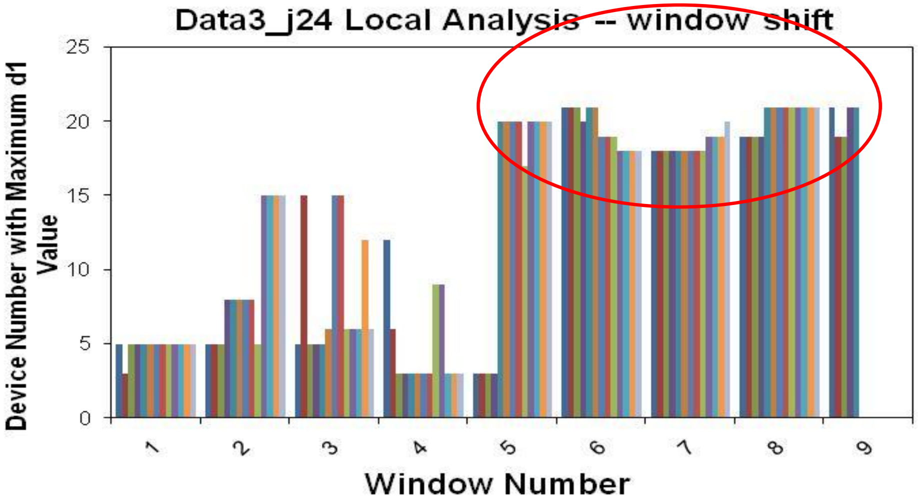
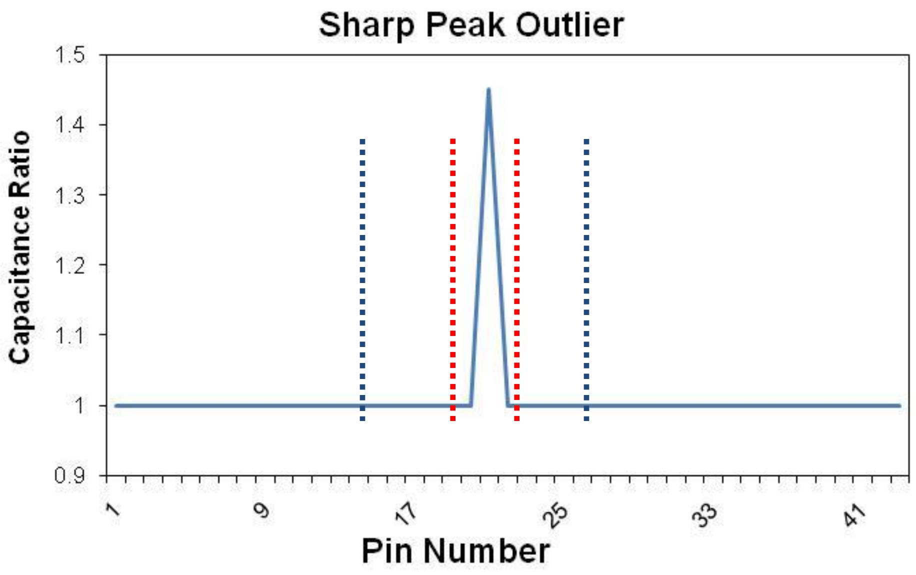


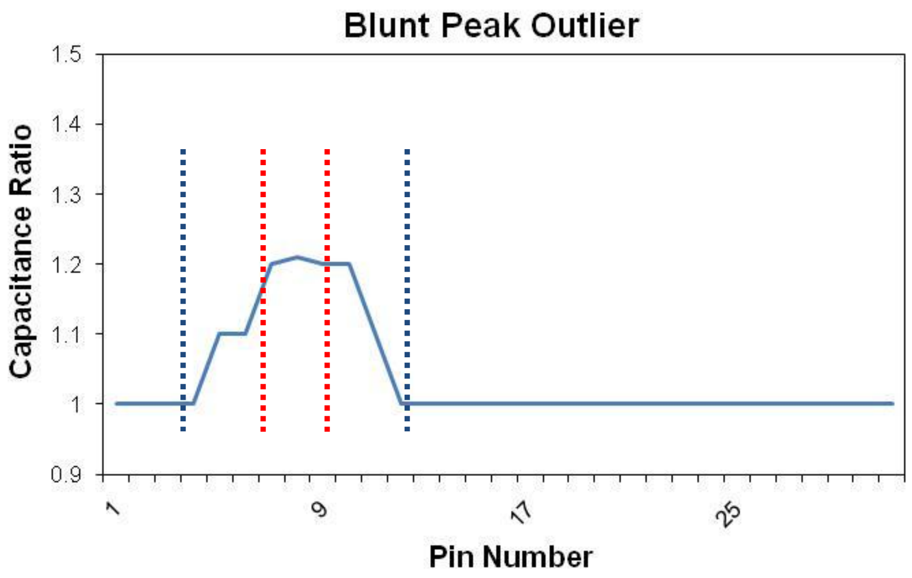
Test Window Shift


Data3_j24 Local Analysis -- window shift

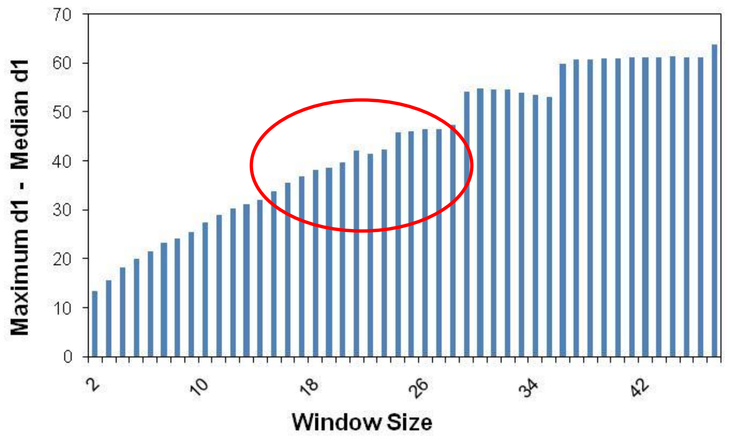

Data3_j24 Local Analysis -- window shift

Size of Test Window

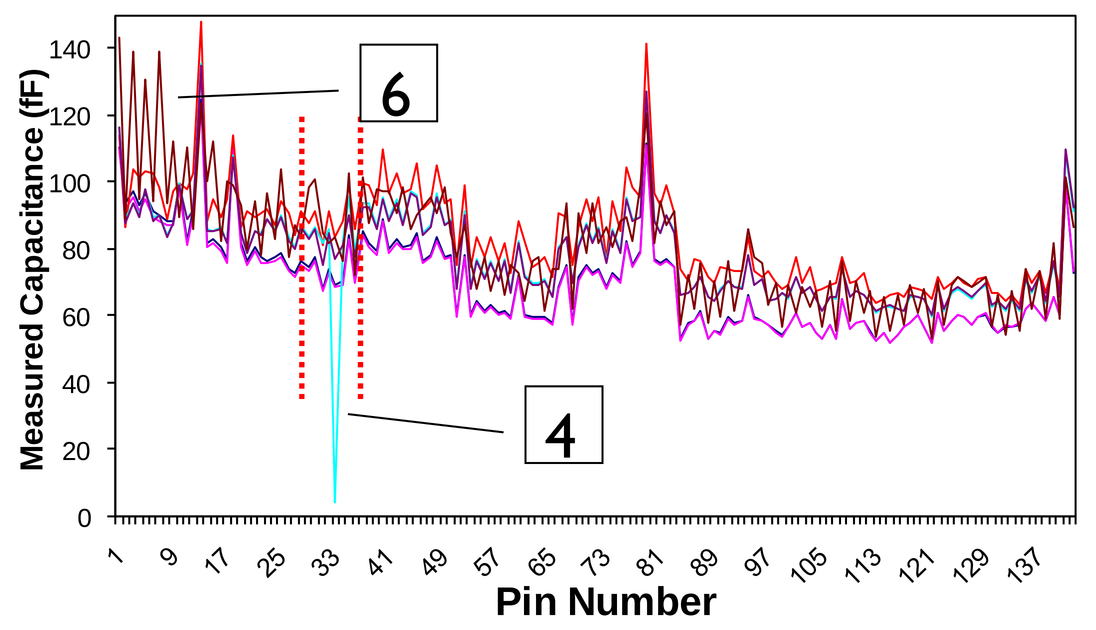


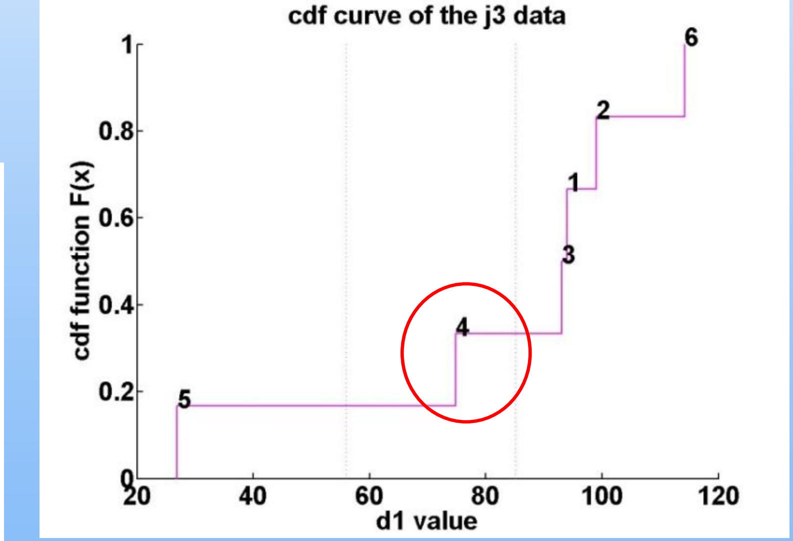


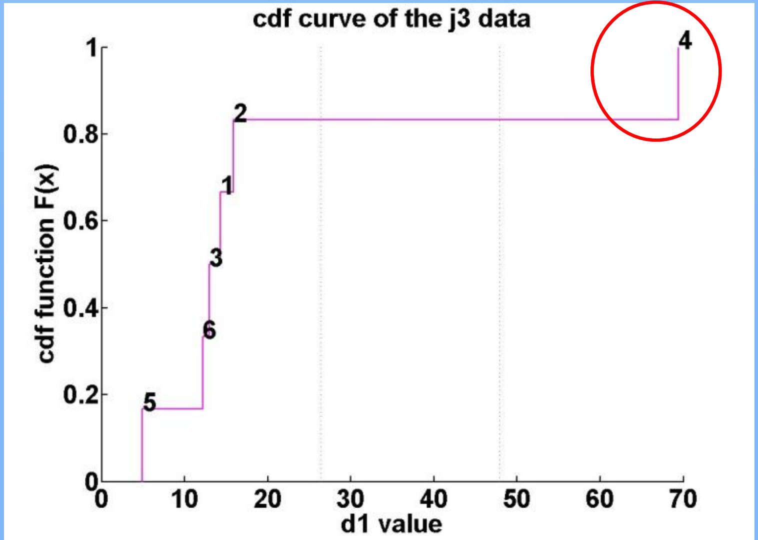
Window size simulation for Data_j24



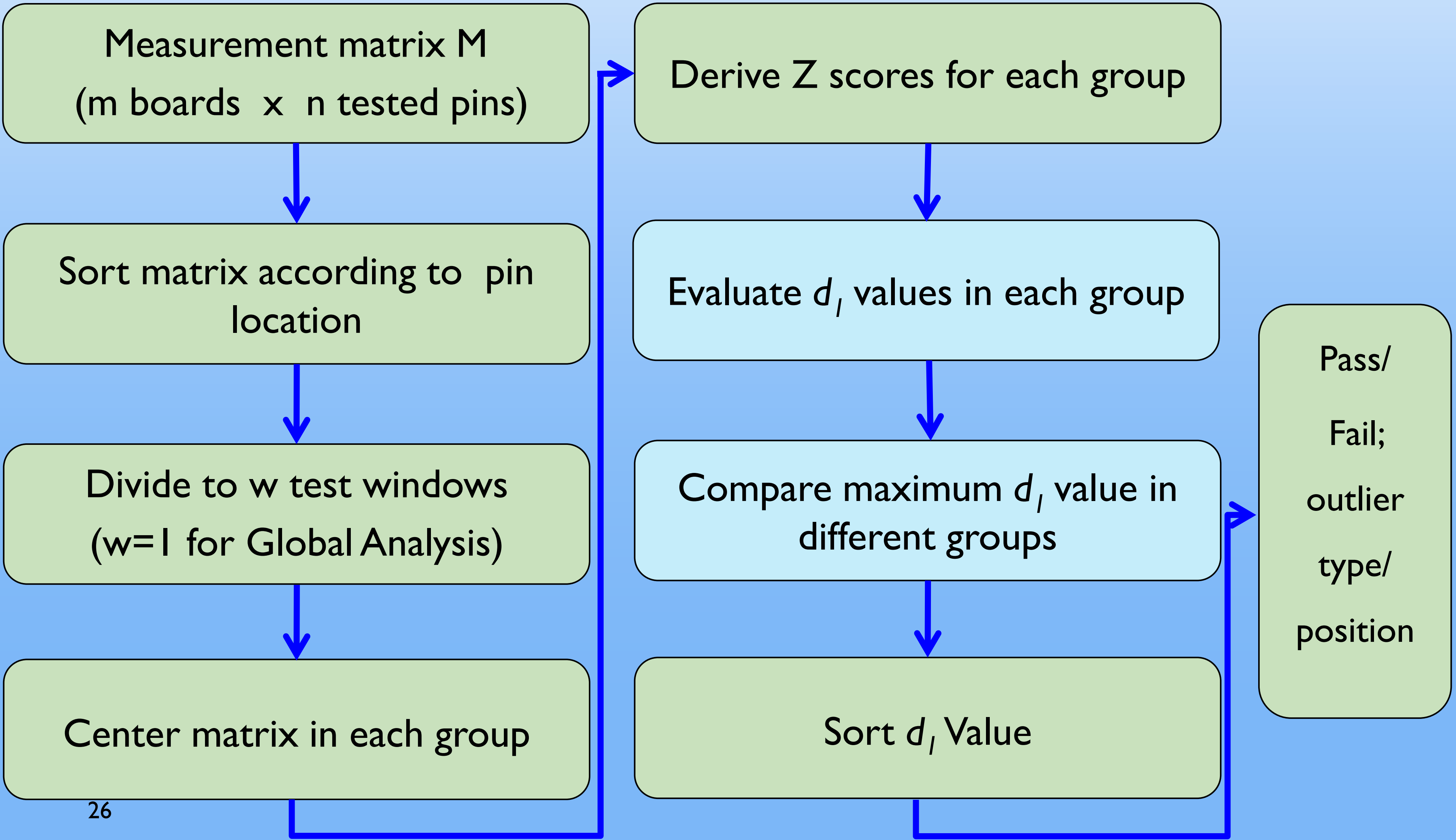
Comparison of Global and Localized Methods (Data_ j3)







PCA Flow Chart



Measurement matrix M
(m boards x n tested pins)

Sort matrix according to pin location

Divide to w test windows
(w=1 for Global Analysis)

Center matrix in each group

Derive Z scores for each group

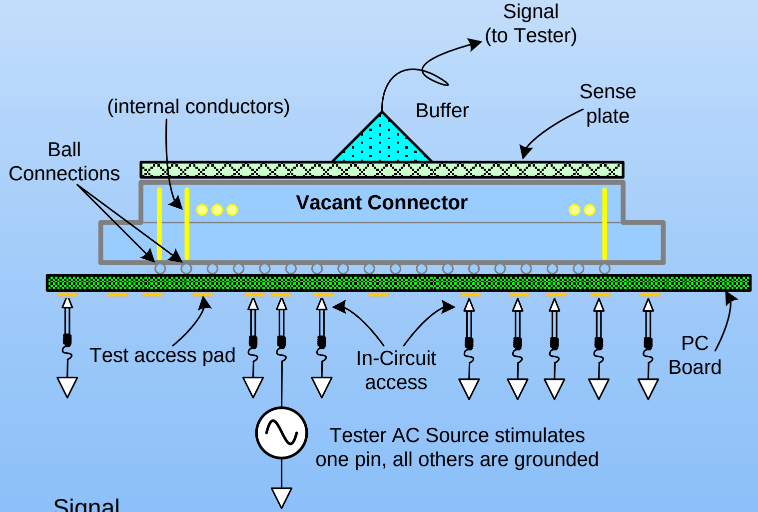
Evaluate d_l values in each group

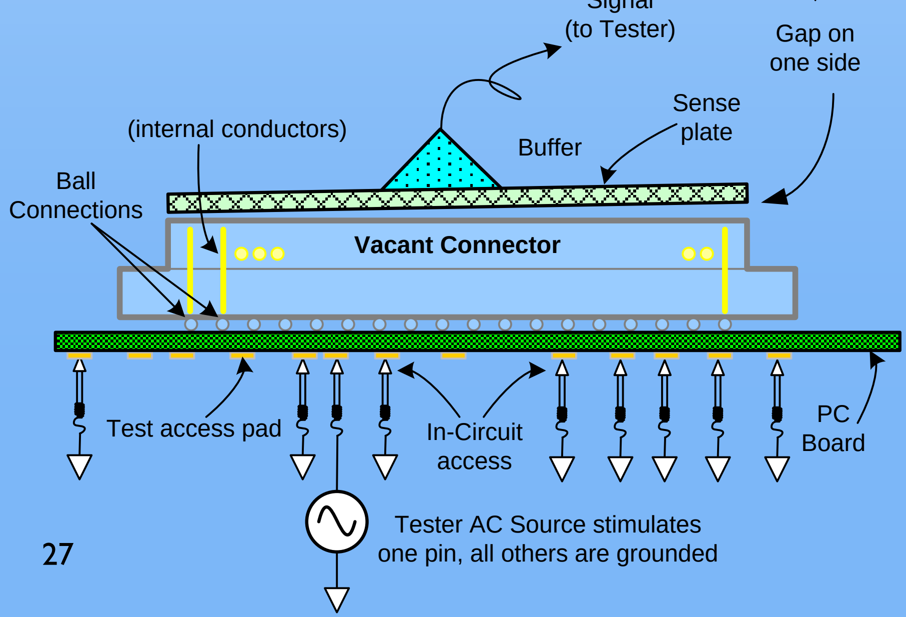
Compare maximum d_l value in different groups

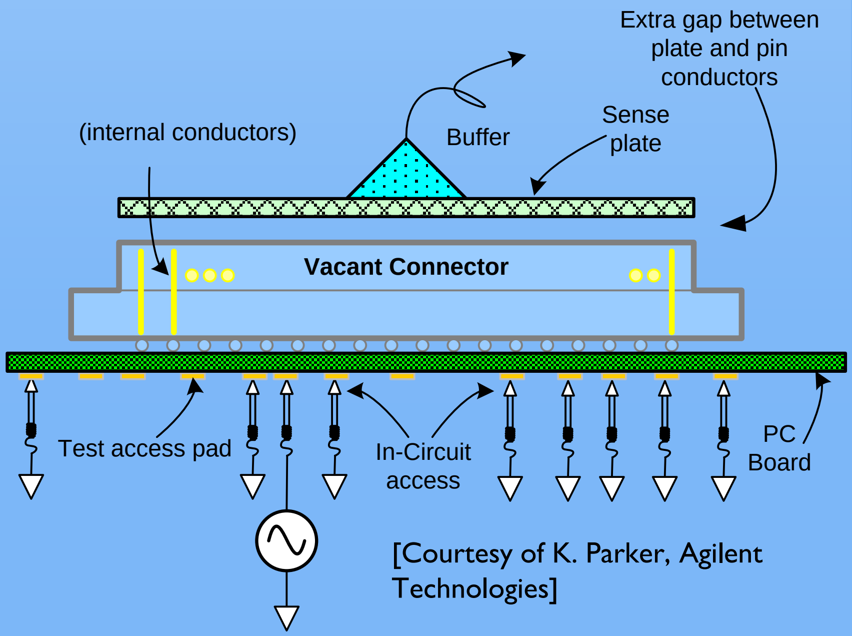
Sort d_l Value

Pass/
Fail;
outlier
type/
position

Capacitive Lead Frame Testing Challenges

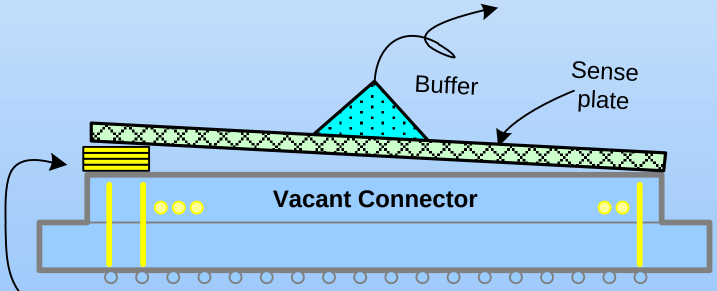




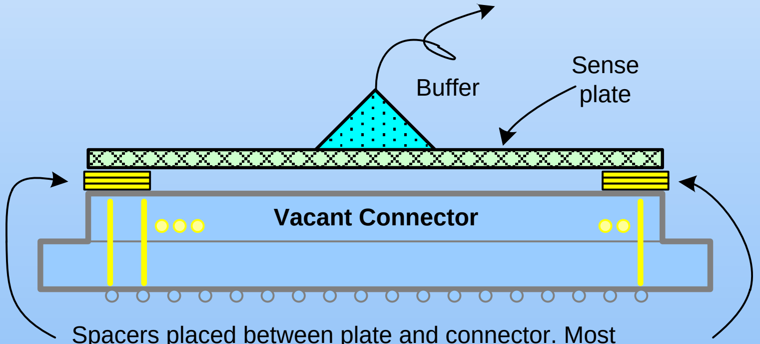


[Courtesy of K. Parker, Agilent Technologies]

Compensation for Mechanical Variation

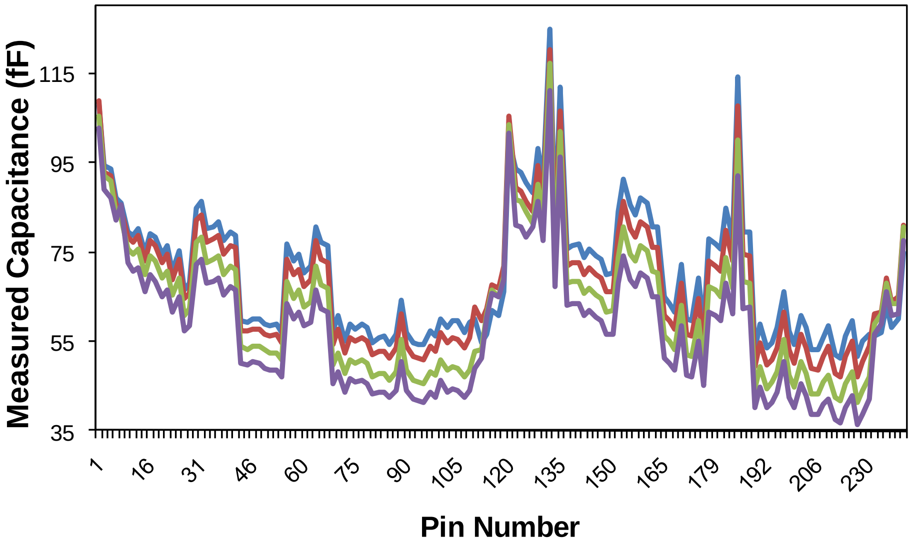


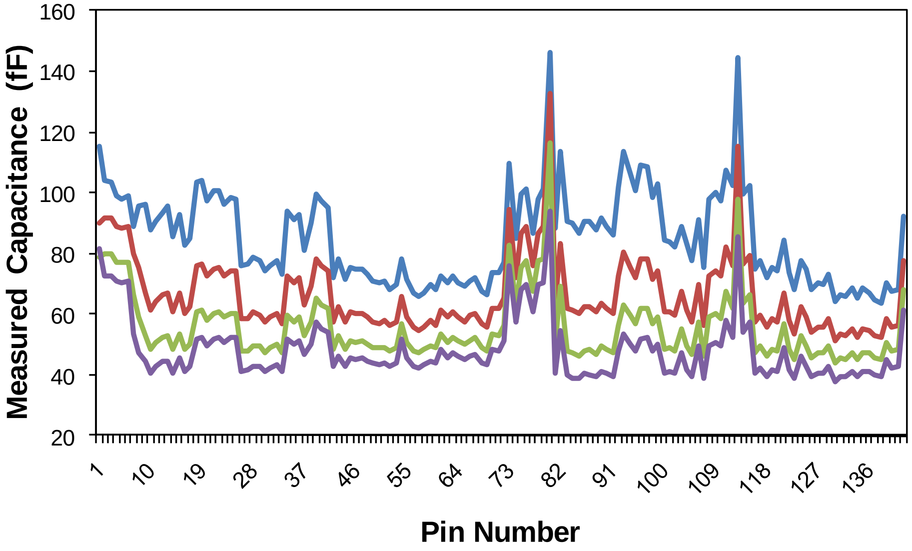
Spacers placed between plate and connector at one end. Again, the spacers have a different dielectric constant from air.



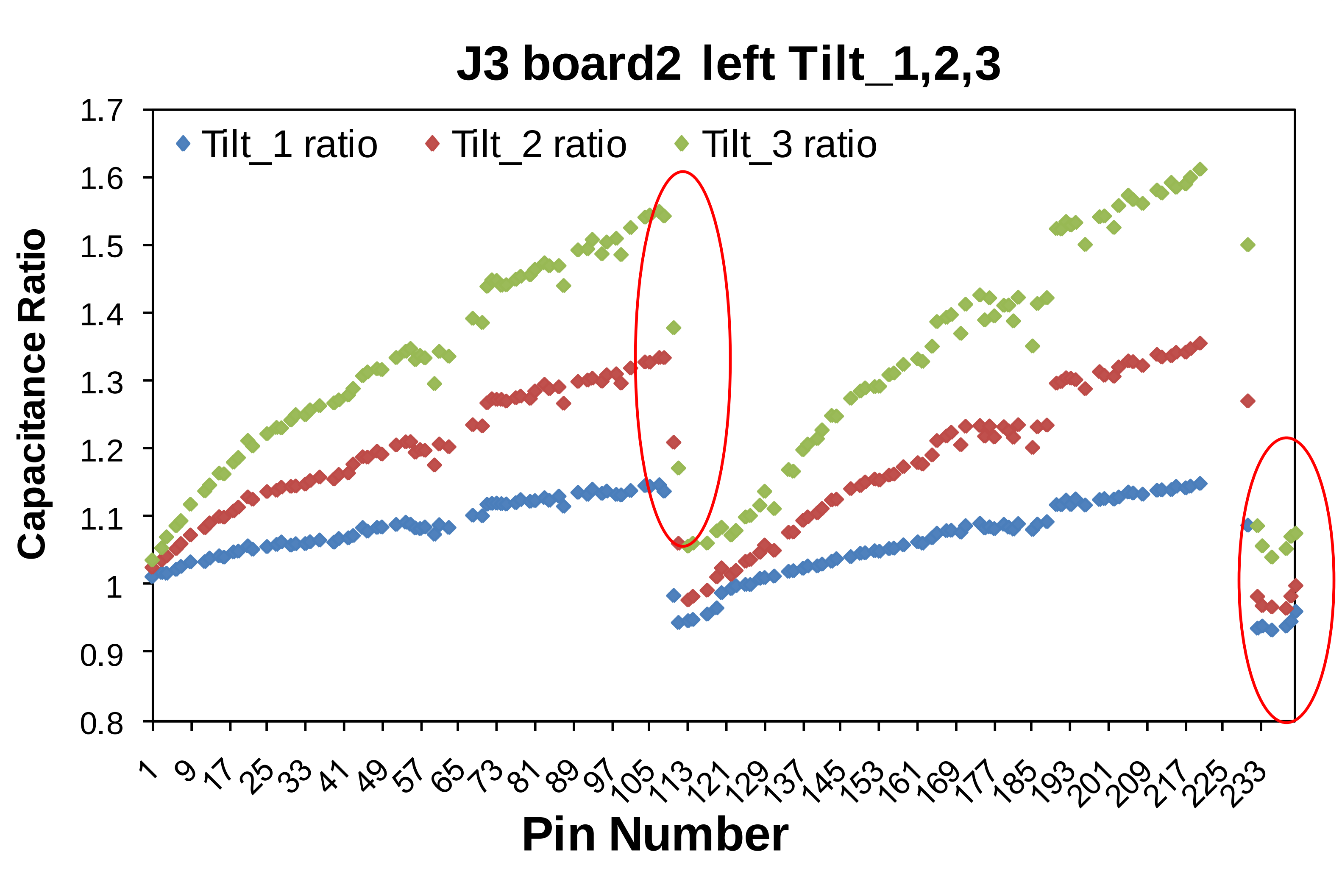
Spacers placed between plate and connector. Most connector pin tips see an air gap to the sense plate, but at the ends, the gap has a different dielectric constant.

[Courtesy of K. Parker, Agilent Technologies]

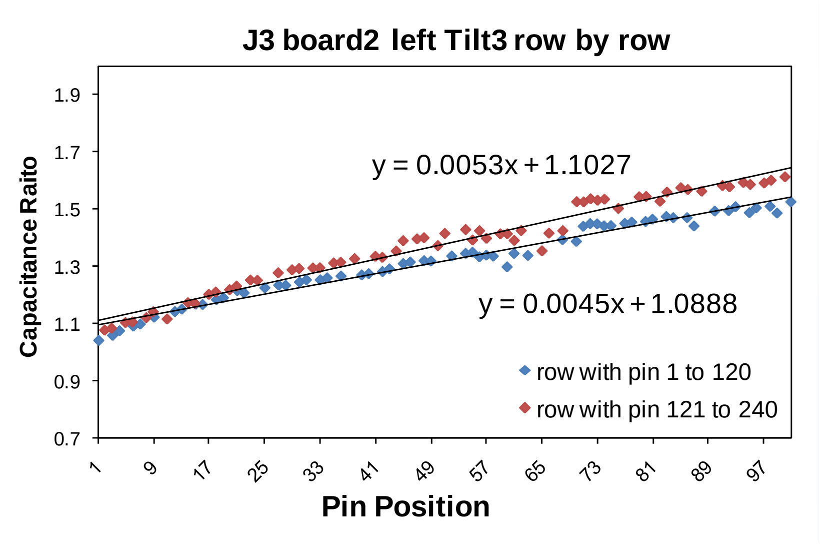


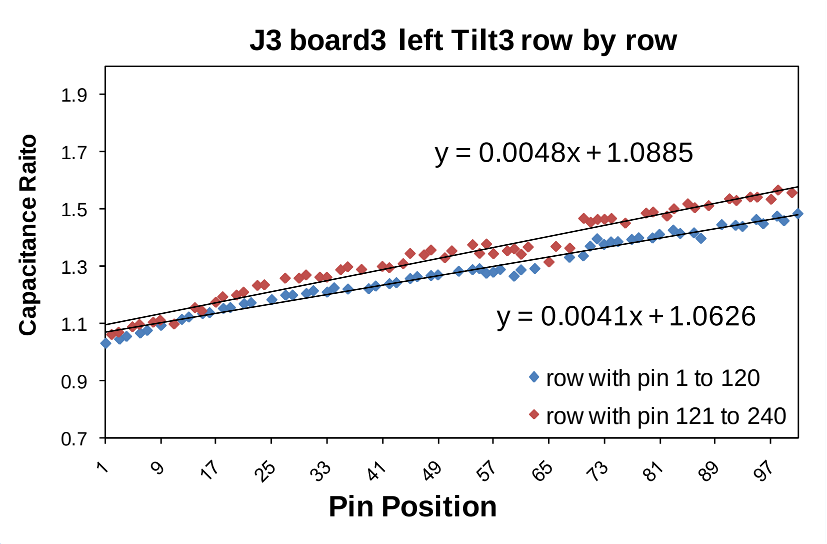


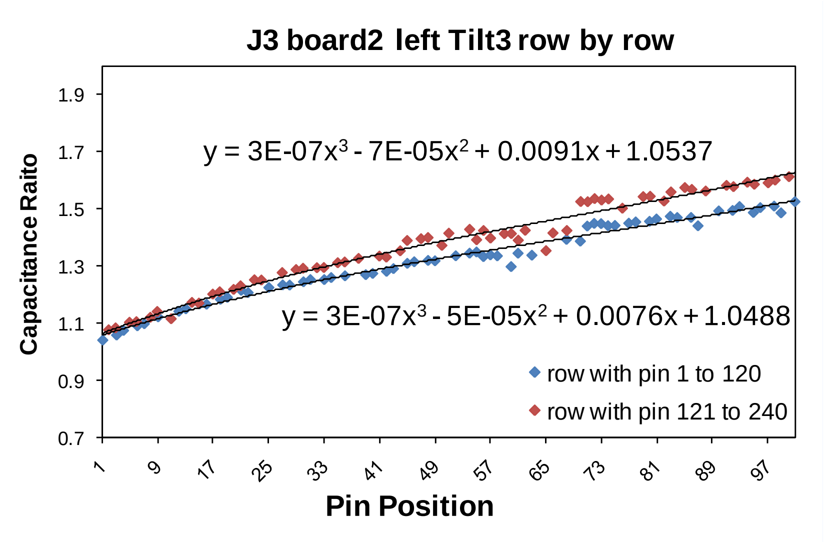
Compensation for Mechanical Variation

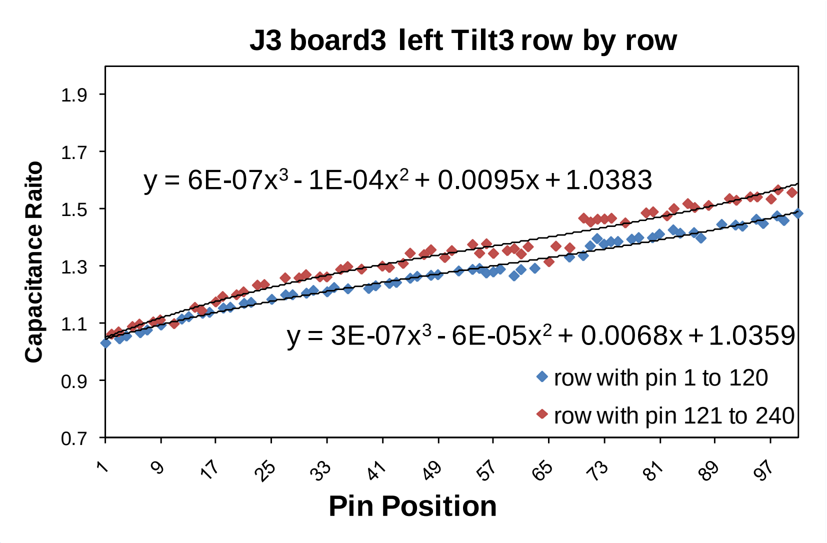


Compensation for Mechanical Variation

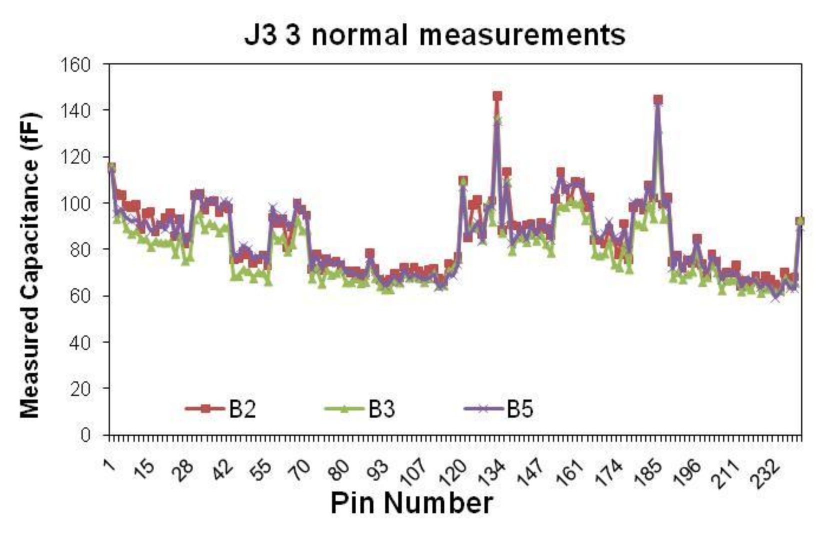

J3 board2 left Tilt3 row by row

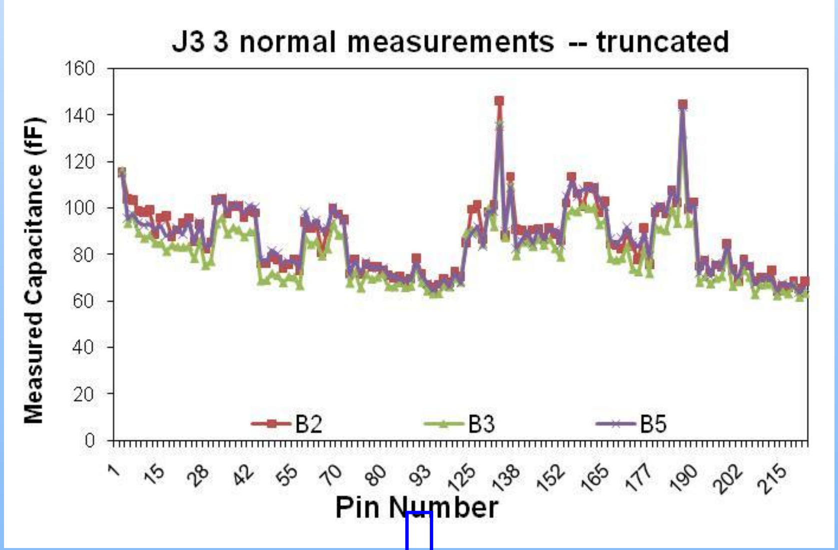

J3 board3 left Tilt3 row by row

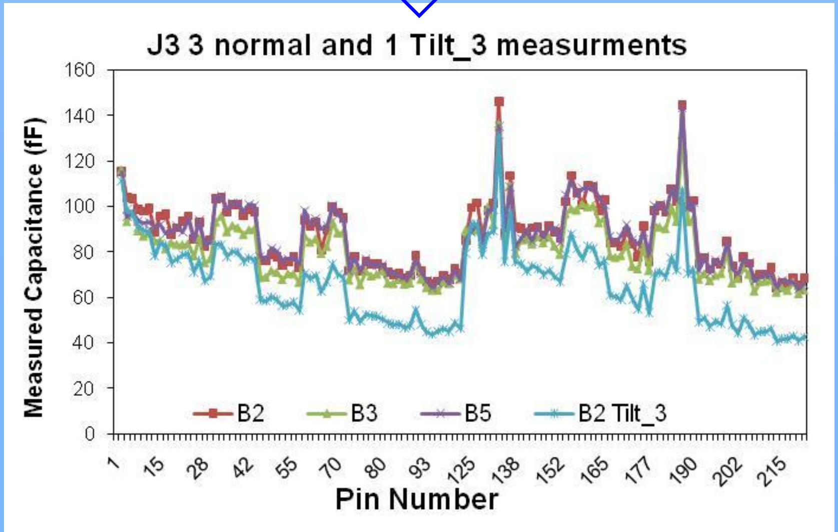

J3 board2 left Tilt3 row by row

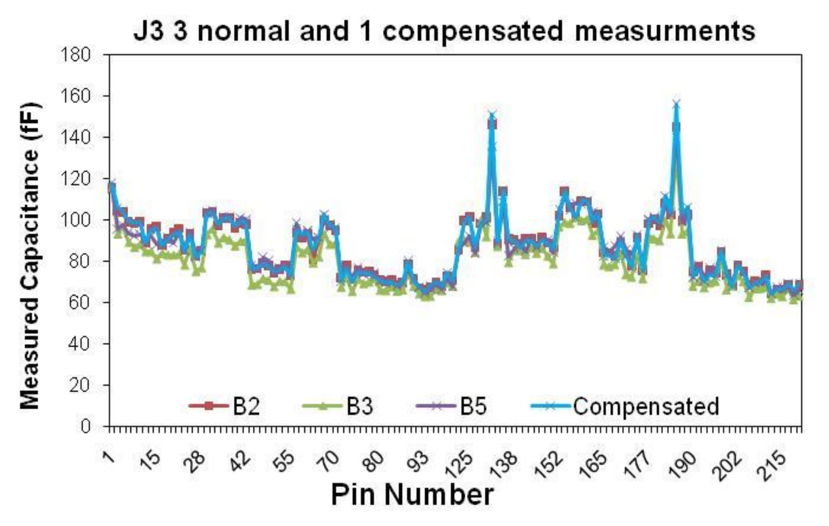

J3 board3 left Tilt3 row by row

Compensation for Mechanical Variation

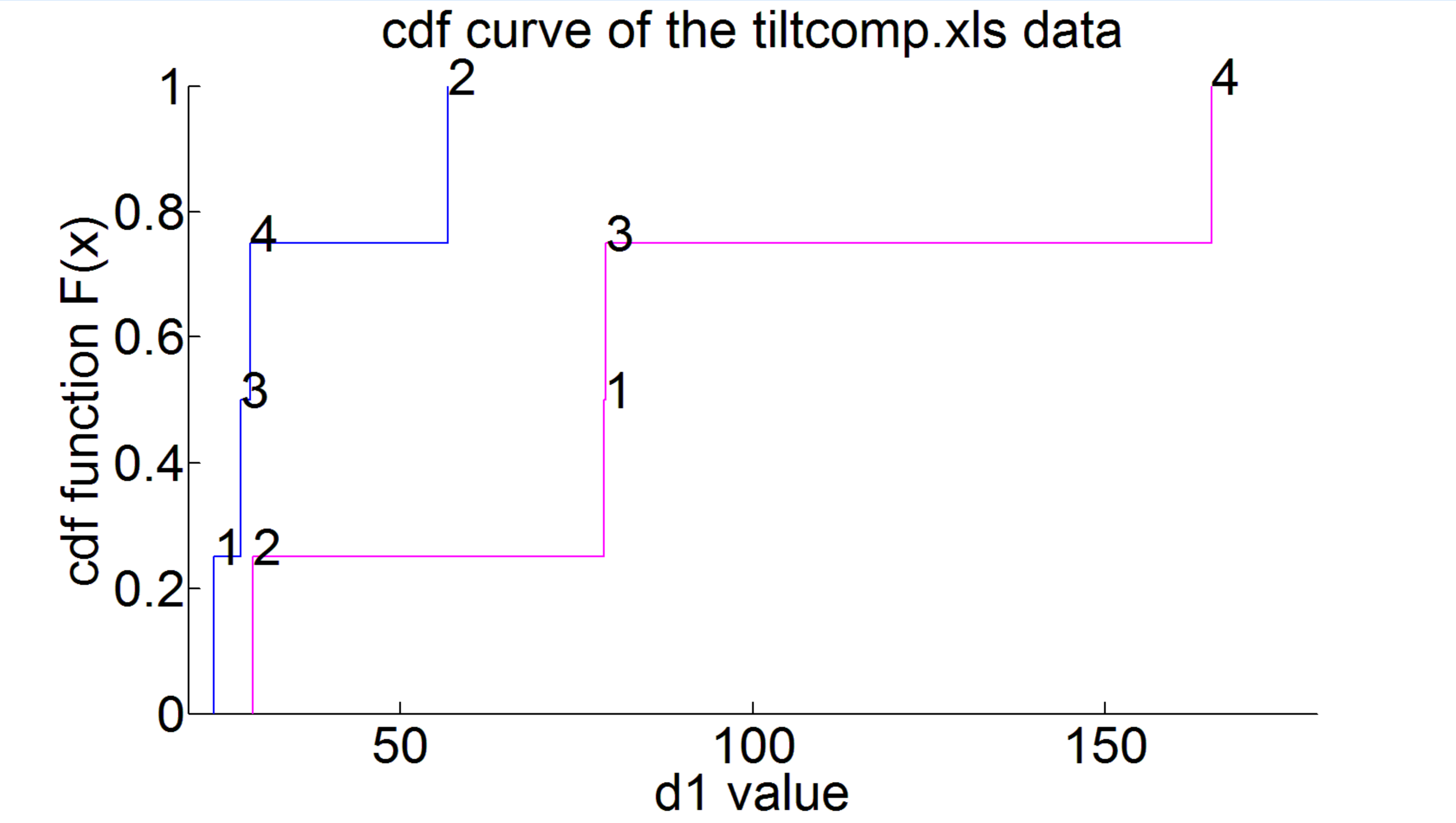

J3 3 normal measurements


J3 3 normal measurements -- truncated


J3 3 normal and 1 Tilt_3 measurments

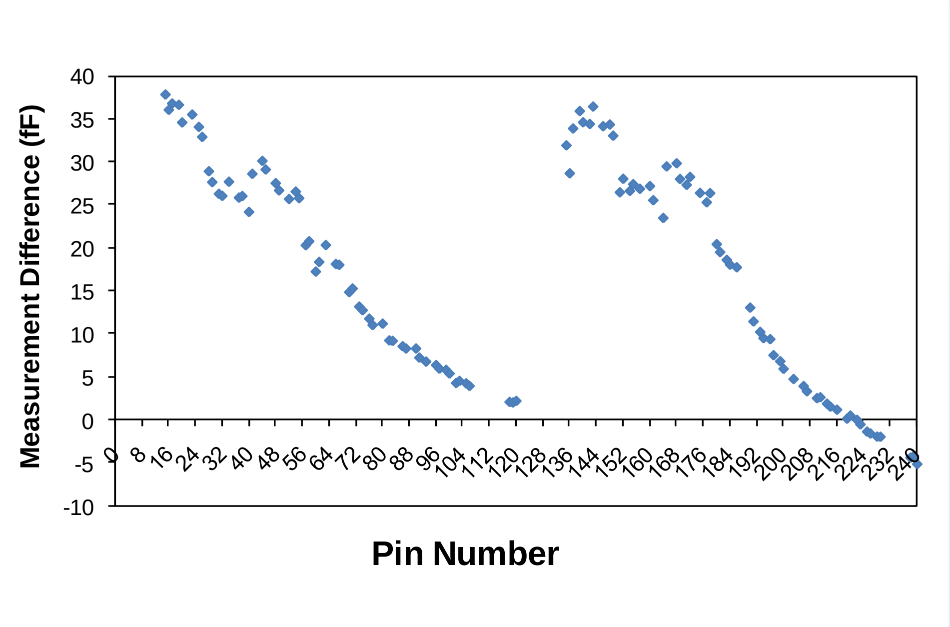

J3 3 normal and 1 compensated measurments

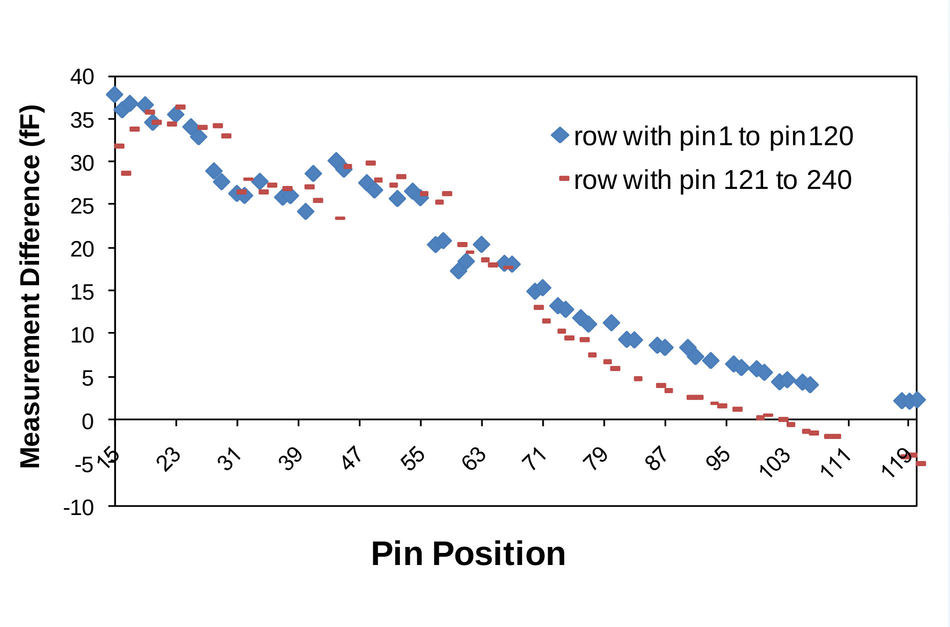
Compensation for Mechanical Variation



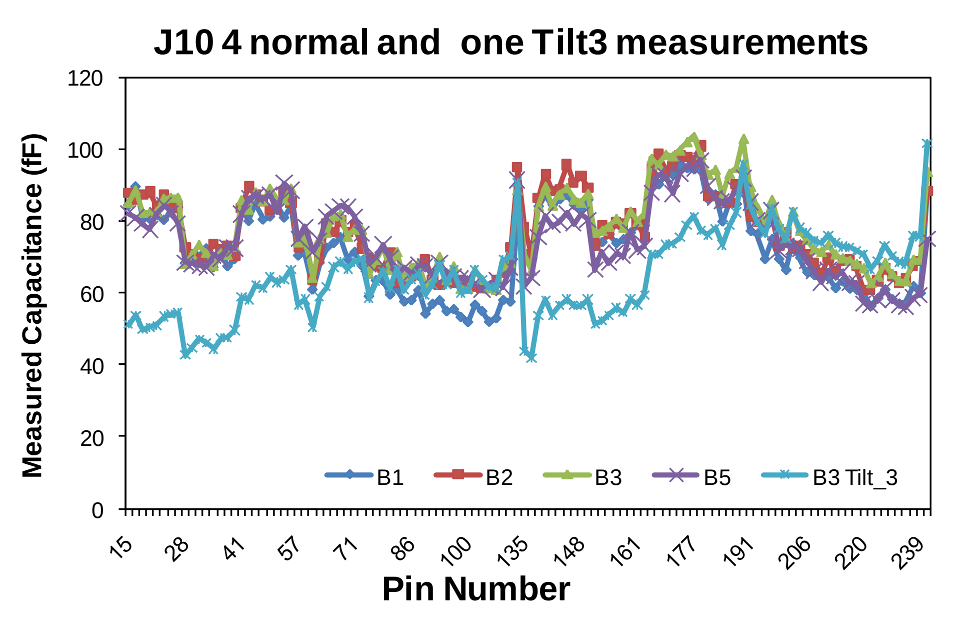
Compensation for Mechanical Variation

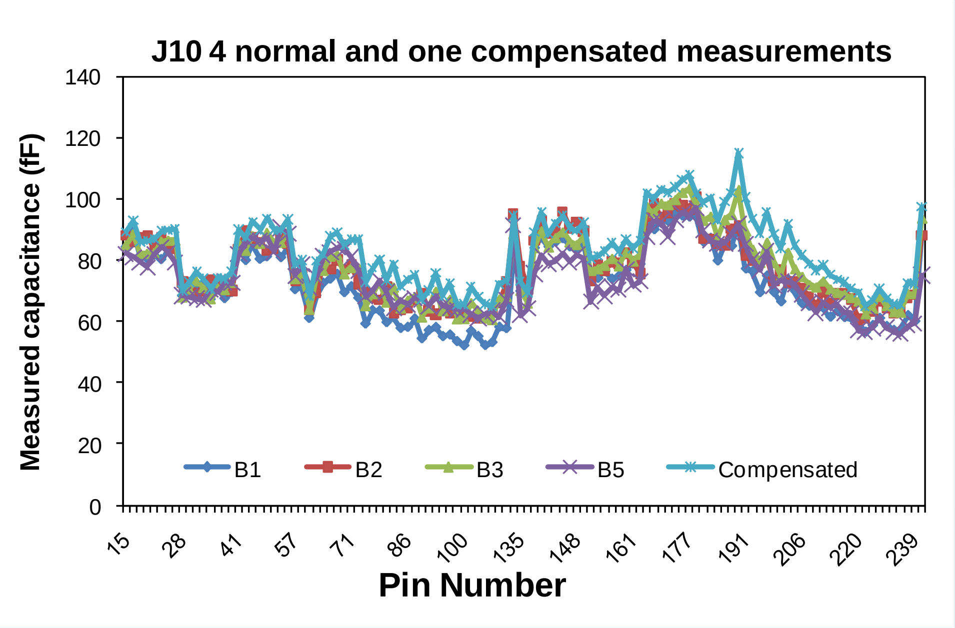
Difference value plot between tilted-plate measurements and normal measurements



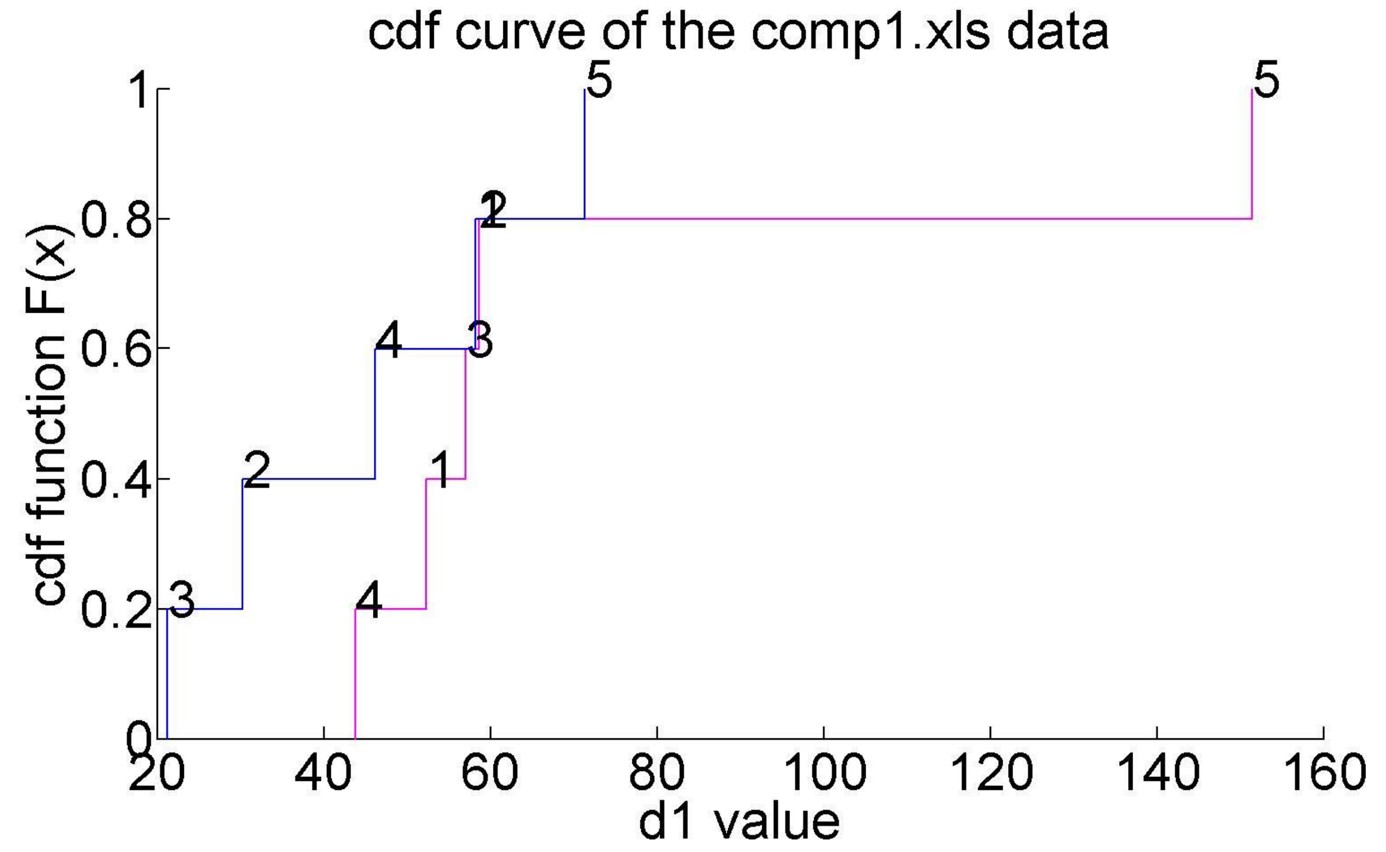


Compensation for Mechanical Variation

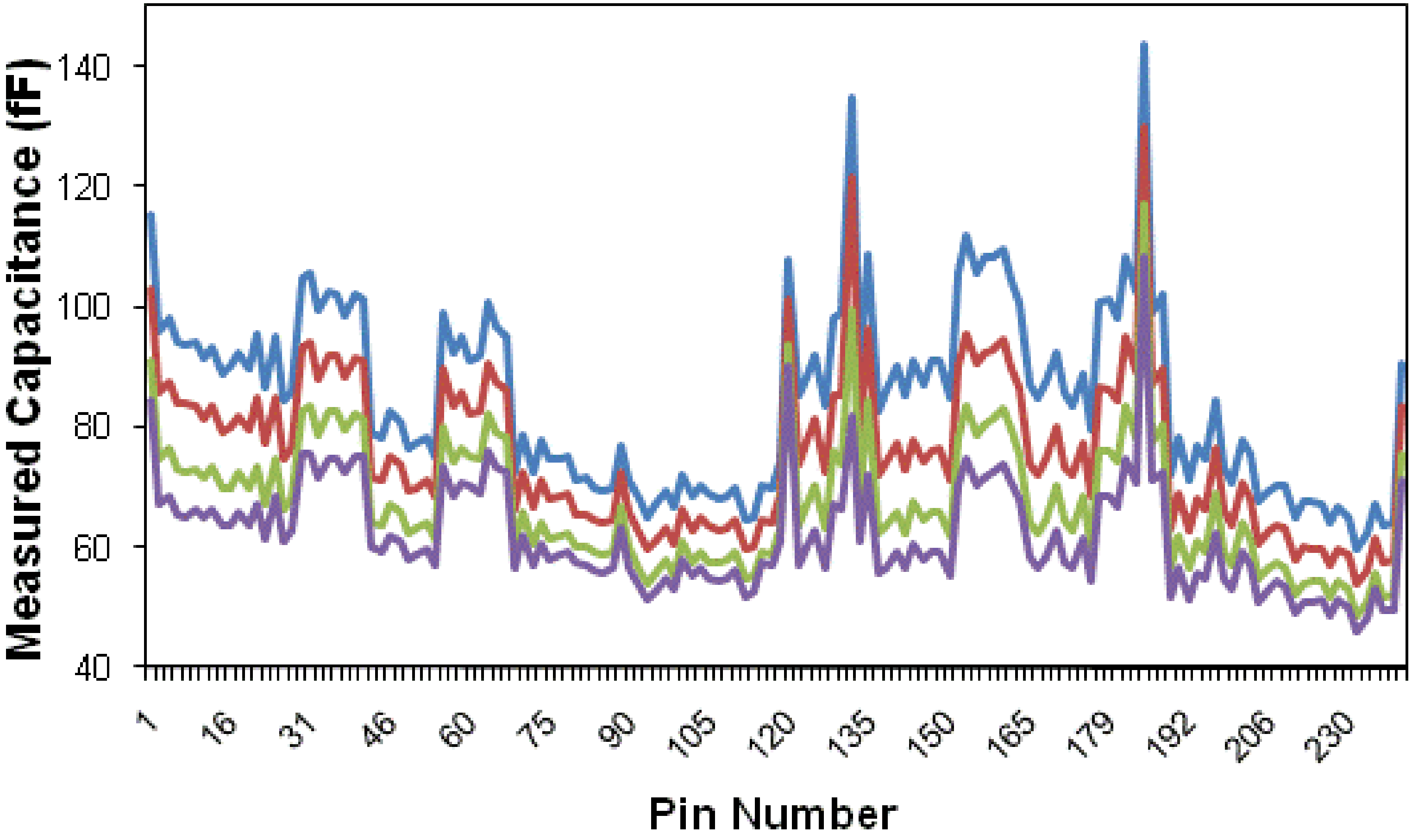




Compensation for Mechanical Variation

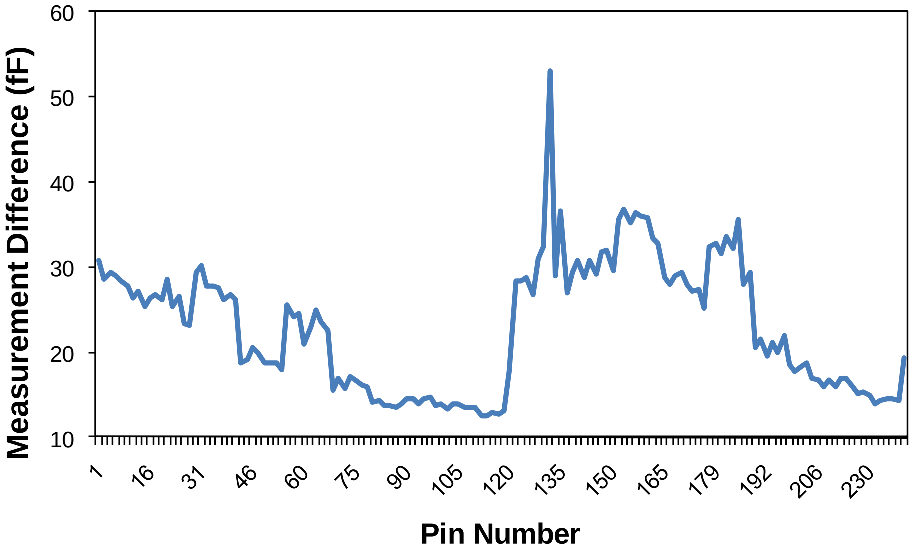


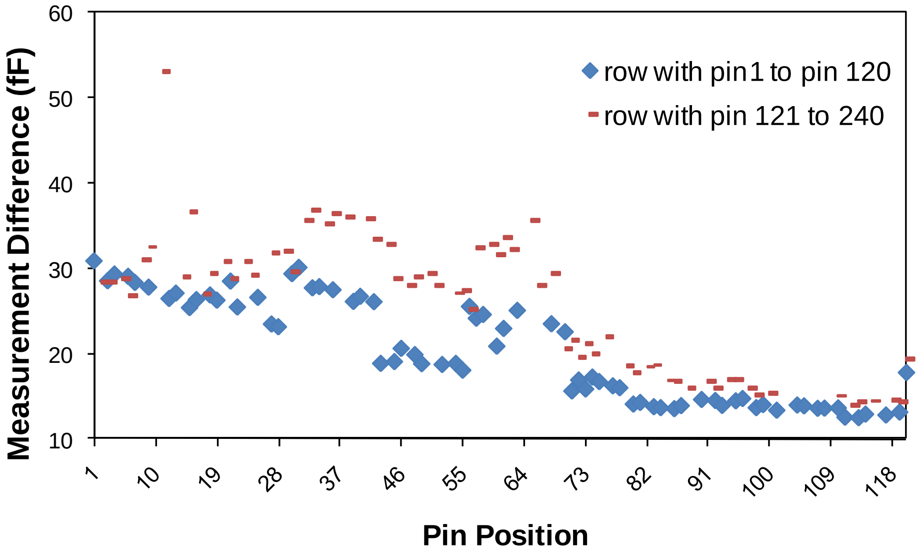
Compensation for Mechanical Variation



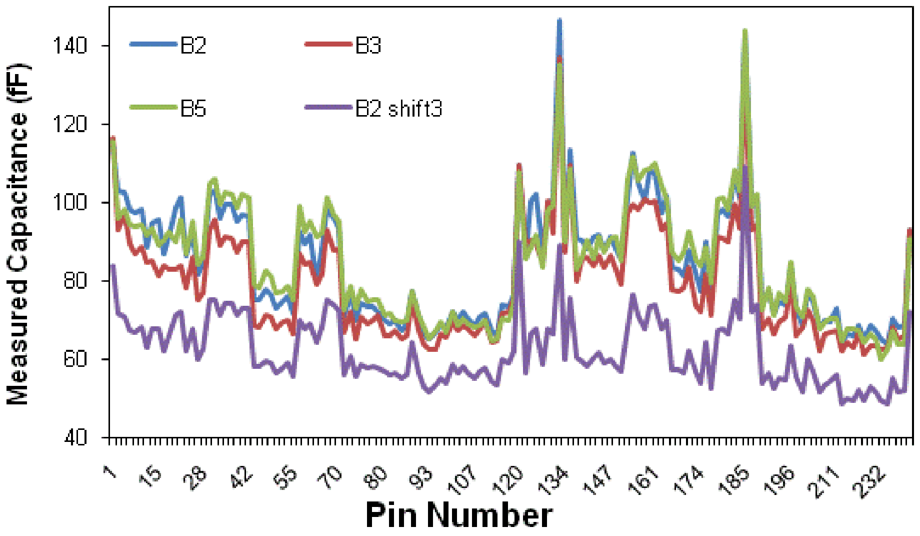
Compensation for Mechanical Variation

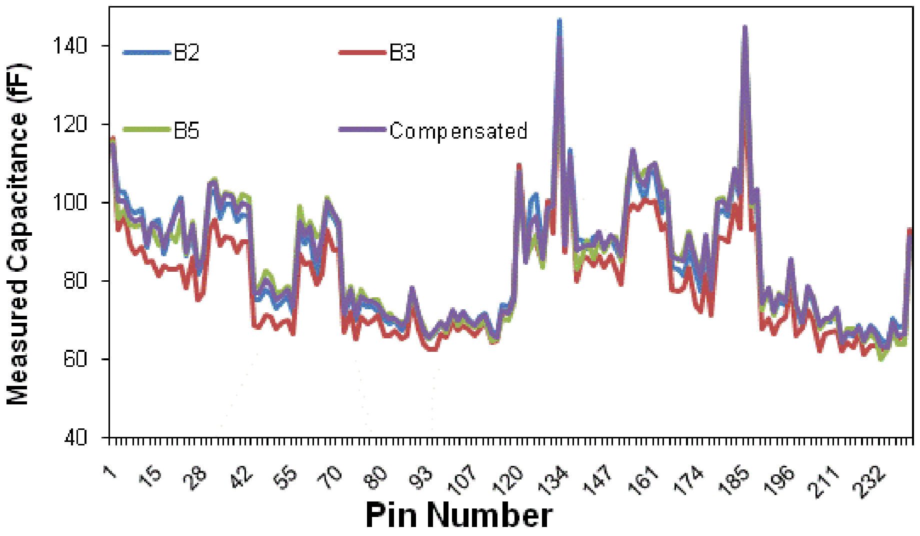
Difference value plot between tilt-measurement and normal measurement.



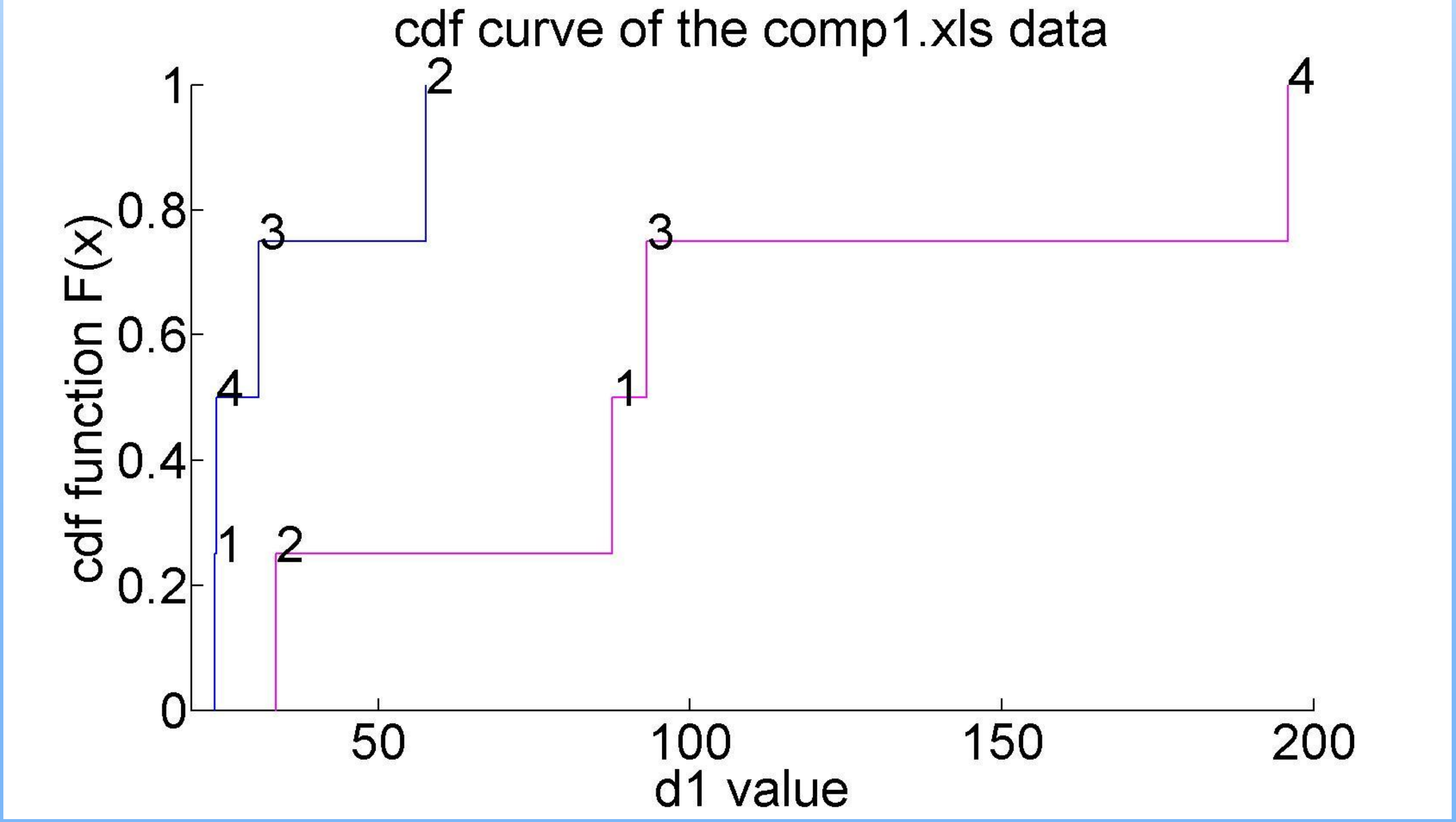


Compensation for Mechanical Variation

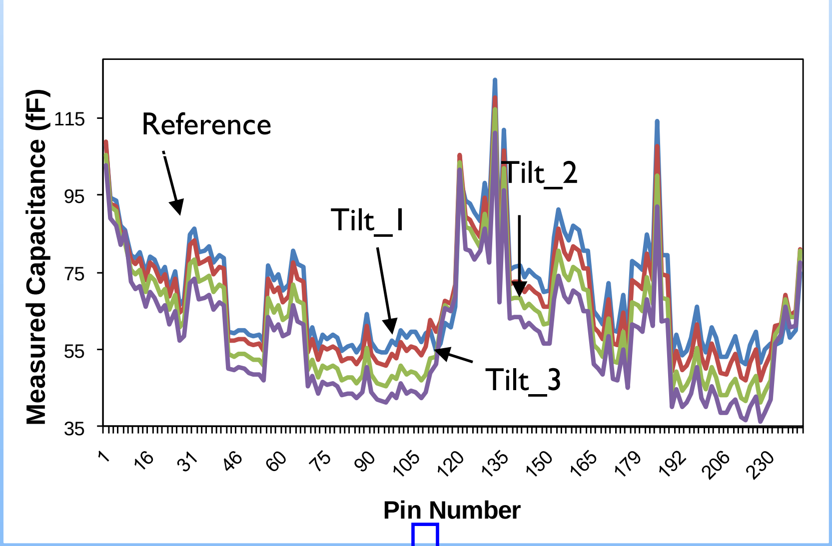


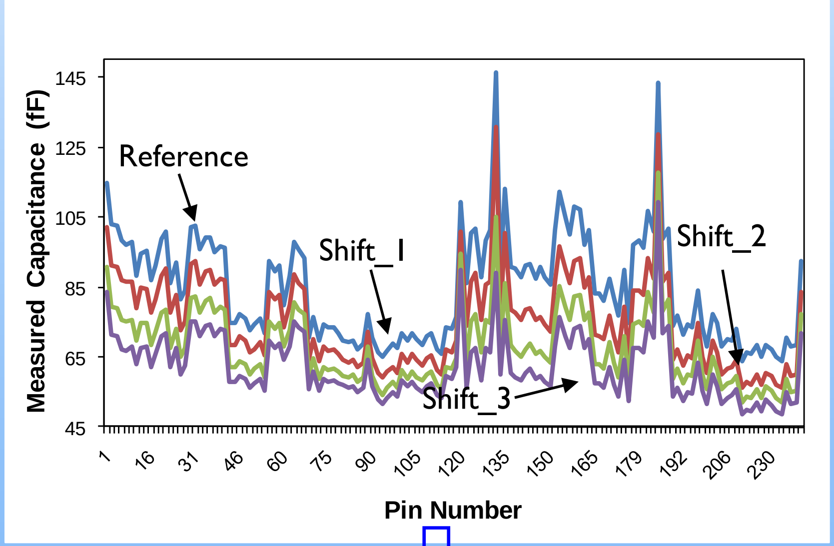


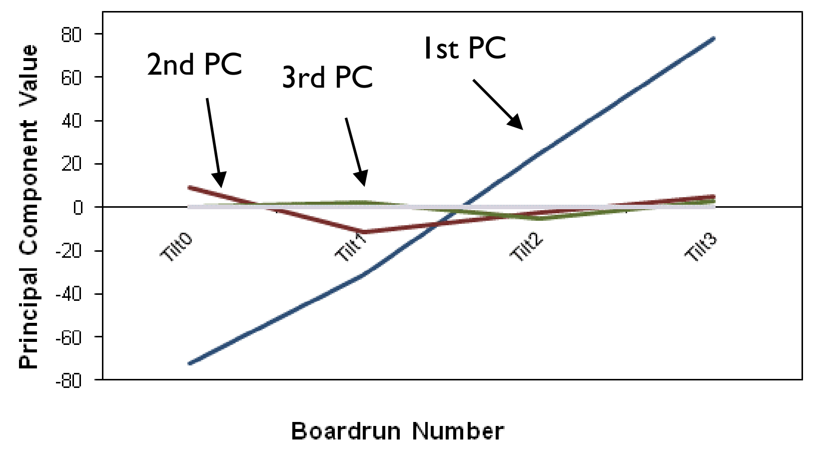
Compensation for Mechanical Variation

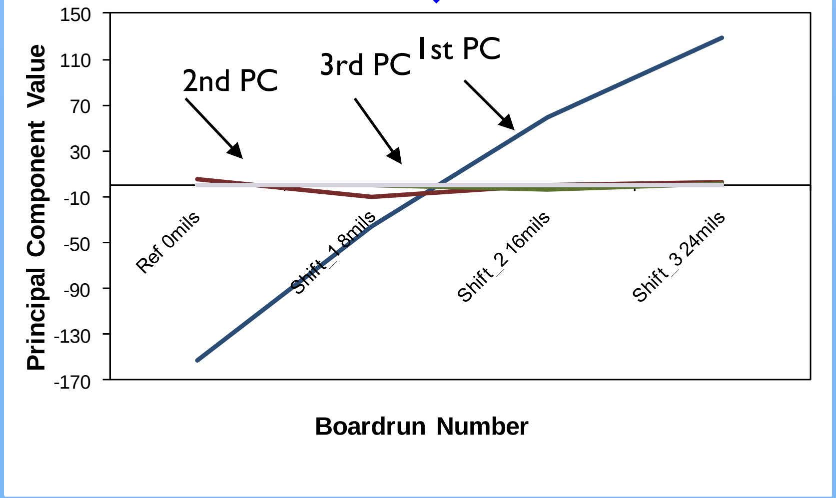


Compensation for Mechanical Variation

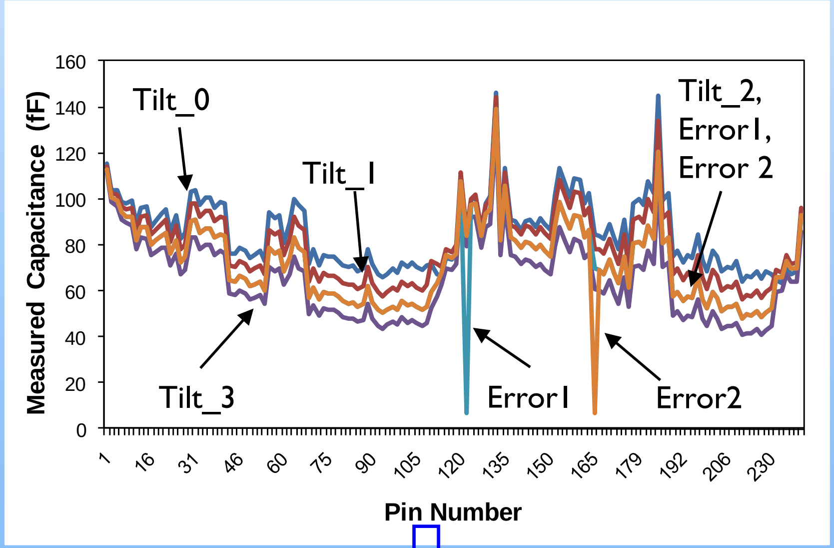


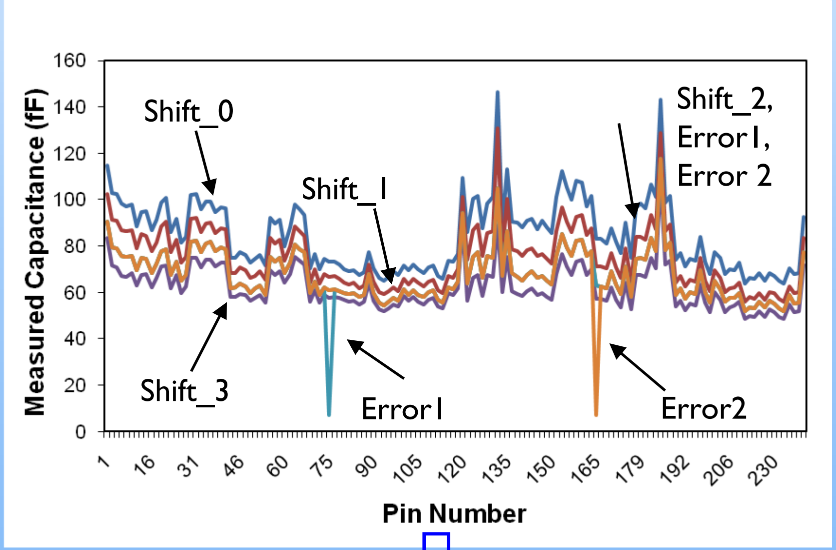


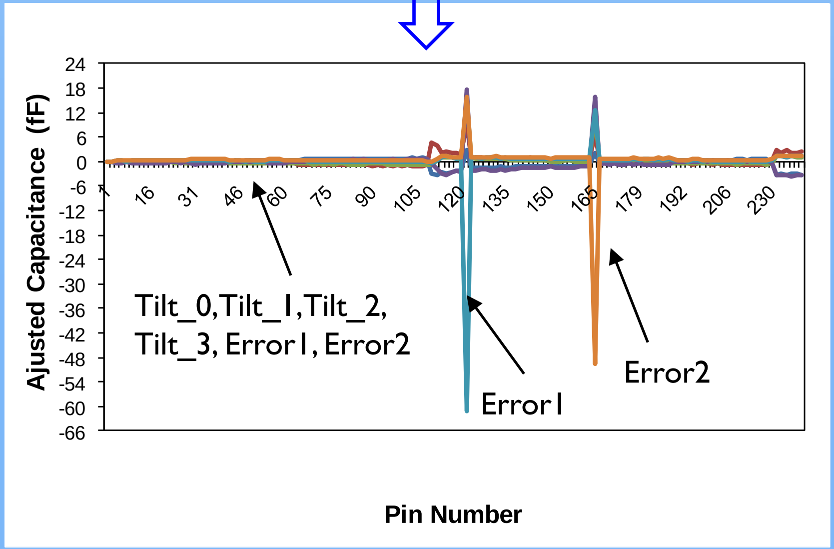


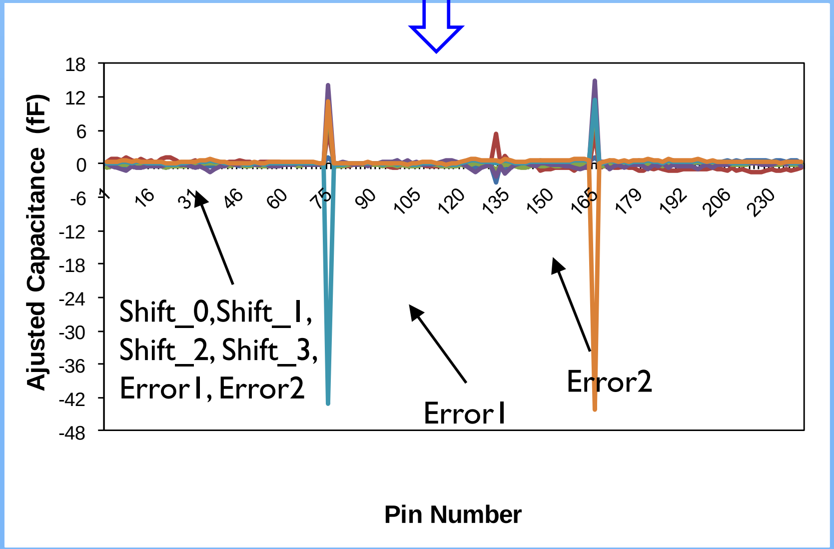


PCA Based Tilt or Shift Evaluation









Summary

- Can effectively identify outlier boards
- Localized analysis can increase test resolution and assist in the location of outliers
- The global and localized analysis can be combined to filter the outliers
- Can be applied to other kinds of PCB test data beside Capacitive Lead frame test data
- Compensation is effective for fixture variation

Future Work

- On-line testing techniques to enhance the detection efficiency
- Investigate data variation caused by measurement errors, mechanical and electrical tolerances
- Technique to compensate for the effects of mechanical variations parameter variations by setting the PC values

Related Publication

- Conference and Workshop Papers
  - X. He, Y. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "Outlier Detection in Capacitive Open Test Data Using Principal Component Analysis,“ Presented at the IEEE 8th International Board Test Workshop (BTW'09), Fort Collins, CO, Sept. 2009
  - X. He, Y. K. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "An Outlier Detection Based Approach for PCB Testing," Proc. 40th International Test Conference (ITC09), Austin, Texas, November 2009.
  - A. P. Jayasumana, Y. K. Malaiya, X. He, K. P. Parker and S. Hird, "Compensation for Measurement Errors Due to Mechanical Misalignments in PCB Testing,“ Presented at the IEEE 9th International Board Test Workshop (BTW'10), Fort Collins, CO, Sept. 2010
  - X. He, Y. K. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "Principal Component Analysis-Based Compensation for Measurement Errors Due to Mechanical Misalignments in PCB Testing" To appear at the 41st International Test Conference (ITC'10), Austin, Texas, November 2010
- Poster
  - Xin He, Yashwant Malaiya, Anura Jayasumana, and Kenneth Parker, "An Outlier Detection Based Approach for PCB Testing," Agilent University Research Fair, Loveland, CO, Feb. 2009.

Thank you!

Questions