Efficient Delay and Crosstalk Modeling of RLC Interconnects Using Delay Algebraic Equations

Sourajeet Roy and Anestis Dounavis

***Abstract*—This paper presents a delay and crosstalk noise model for coupled resistance-inductance-capacitance (RLC) on-chip interconnects. The proposed algorithm, based on a modified Lie formula, is used to convert the solution of the transmission line network into delay algebraic equations to obtain the time domain response. The proposed algorithm is not limited to fixed number of coupled RLC lines or to specific topologies and can be used to model both identical and nonidentical multiconductor lines and loads. For the example presented in this paper, the 50% delay and crosstalk using the proposed method agrees with SPICE results to within 0.75% average error.**

***Index Terms*—Aggressor line, crosstalk, delay, inductance, interconnects, system analysis and design, transmission line theory, victim line.**

I. Introduction

As size of modern generation integrated circuit (IC) decreases, clock speeds are expected to increase beyond the 10-GHz range [1]. However to eliminate large interconnect latencies, scaling of interconnect geometries has not been so rapid, leading to longer wire delays [2]. At such high speeds of operation, the high-frequency effects in the inductively prominent on-chip interconnect ceases to be negligible [3], [4]. Moreover with the diminishing size of modern VLSI circuits, the inductive coupling of the on-chip interconnect affect a substantially larger physical area of the IC [5]. Thus signal integrity impairment owing to effects like attenuation, crosstalk, ringing and spurious glitches are a primary source of concern for modern IC designers. Although accurate SPICE simulation techniques for coupled RLC interconnects do exist [4], such methods use numerical integration or convolution which is computationally expensive for layout optimizations in early stages of the design cycles. For iterative layout design of densely populated ICs, accurate analytic models are needed to efficiently predict delay and crosstalk noise of interconnects.

In the past, on-chip interconnects were modeled as RC lines and single pole Elmore-based models [6]–[9] were widely used to estimate signal delay. However, in current integrated circuit designs, wire inductance can no longer be ignored due to higher operating speeds and RLC models are required. As a result, the issue of developing closed form expressions for coupled RLC interconnects has been a topic of intense research [10]–[21]. However, these algorithms may have limitations in accuracy, due to the type of approximations made to derive the models. For example, the Bessel function model of [13]–[16] is not suitable for coupled line structures beyond three coupled lines due to the model complexity involved; [19] uses nonphysical empirical corrections to model inductive coupling effects and [20] assumes open load terminations and provides no coupling aware switching.

In [22], the DEPACT algorithm is developed for SPICE analysis of high speed interconnects. The formulation of [22] uses modified nodal analysis (MNA) to describe the network equations and provides the complete solution for both the far end and near end responses of interconnects for any linear and nonlinear load terminations. In this paper, the concepts developed in [22] are further extended to create an efficient solution algorithm for the far end responses of coupled RLC interconnects when the lines are terminated by resistances and capacitances as discussed in the literature [7]–[21]. The method approximates the transfer function matrix for the far end of coupled lines as a set of m delay algebraic equations, where m corresponds to the number of coupled lines and does not use the MNA formulation. As a result, the proposed algorithm will be significantly faster for solving the far end responses compared to [22] for the case when the near and far end of the lines are terminated with resistances and capacitances, respectively. This will be illustrated with numerical examples in Section IV.

Manuscript received January 12, 2009; revised April 13, 2009 and June 16, 2009. This work was supported by the Natural Sciences and Engineering Research Council of Canada, The Canada Foundation for Innovation, Ontario Ministry of Research and Innovation—Early Research Award, and The Canadian Microelectronics Corporation.

The authors are with the Department of Electrical and Computer Engineering, University of Western Ontario, London, ON, Canada N6A 5B9 (e-mail: sroy33@uwo.ca; adounavis@eng.uwo.ca).

Digital Object Identifier 10.1109/TVLSI.2009.2032288

II. Analysis of Coupled RLC Interconnect

This section briefly reviews the transmission line theory and describes the DEPACT algorithm [22] which will be used to develop the proposed delay and crosstalk model.

A. Analysis of Coupled RLC Interconnect

The solution of Telegraphers equations for on-chip RLC interconnects are can be written as an exponential matrix function as

$$\begin{bmatrix} \boldsymbol{V}(l,s) \\ -\boldsymbol{I}(l,s) \end{bmatrix} = e^{\boldsymbol{\Phi}} \begin{bmatrix} \boldsymbol{V}(0,s) \\ \boldsymbol{I}(0,s) \end{bmatrix} \tag{1}$$

where

$$\boldsymbol{\Phi} = \boldsymbol{A} + s\boldsymbol{B}; \quad \boldsymbol{A} = \begin{bmatrix} 0 & -\boldsymbol{R}l \\ 0 & 0 \end{bmatrix}; \quad \boldsymbol{B} = \begin{bmatrix} 0 & -\boldsymbol{L}l \\ -\boldsymbol{C}l & 0 \end{bmatrix} \tag{2}$$

"s" is the Laplace transform variable; $\boldsymbol{V}$ and $\boldsymbol{I}$ represent the terminal voltage and current vectors of the transmission line, respectively; $\boldsymbol{R}$, $\boldsymbol{L}$, and $\boldsymbol{C}$ are the per-unit-length resistance, inductance, and capacitance matrices, respectively, and l is the length of the transmission line. The exponential matrix of (1) can be subdivided into four block matrices described in terms of $\cosh$ and $\sinh$ functions as

$$e^{\begin{bmatrix} 0 & -(\boldsymbol{R}+s\boldsymbol{L})l \\ -s\boldsymbol{C}l & 0 \end{bmatrix}} = \begin{bmatrix} \cosh(l\sqrt{\boldsymbol{Z}\boldsymbol{Y}}) & -\boldsymbol{Y}_0^{-1}\sinh(l\sqrt{\boldsymbol{Y}\boldsymbol{Z}}) \\ -\boldsymbol{Y}_0\sinh(l\sqrt{\boldsymbol{Y}\boldsymbol{Z}}) & \cosh(l\sqrt{\boldsymbol{Y}\boldsymbol{Z}}) \end{bmatrix} \tag{3}$$

where $\mathbf{Y}_0 = \mathbf{Y}(\sqrt{\mathbf{Y}\mathbf{Z}})^{-1}$, $\bar{\boldsymbol{Z}} = (\bar{\boldsymbol{R}} + s\bar{\boldsymbol{L}})$ and $\mathbf{Y} = s\boldsymbol{C}$. Equation (1) does not have a direct representation in the time-domain which makes it difficult to analytically predict the delay and crosstalk signals of transmission lines.

B. Review of DEPACT Model

The basic idea of the DEPACT algorithm is to separate the delay terms from $e^{(\mathbf{A}+s\mathbf{B})}$, however, this is not a simple task since the matrices $\boldsymbol{A}$ and $s\boldsymbol{B}$ do not commute, (i.e. $e^{(\mathbf{A}+s\mathbf{B})} \neq e^{\mathbf{A}}e^{s\mathbf{B}}$). To approximate $e^{(\mathbf{A}+s\mathbf{B})}$ in terms of a product of exponentials, a modified Lie product is used as

$$e^{\mathbf{A}+s\mathbf{B}} \approx \prod_{i=1}^{n} \boldsymbol{\Psi}_i + \varepsilon_n \quad \text{and} \quad \boldsymbol{\Psi}_i = e^{\frac{\mathbf{A}}{2n}} e^{s\frac{\mathbf{B}}{n}} e^{\frac{\mathbf{A}}{2n}} \tag{4}$$

where "n" is the number of sections. The associated error of the approximation is $\|\varepsilon_n\| \cong O(1/n^2)$. Provided sufficient lumped sections,

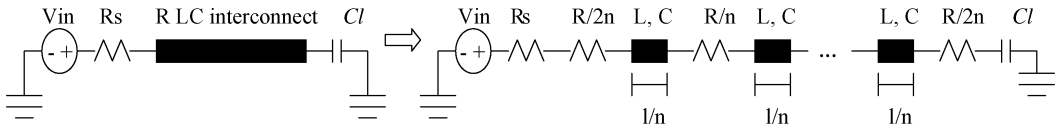

Fig. 1. Circuit model of distributed RLC interconnect.

"n," are used, the convergence of the modified Lie product is guaranteed [22]. Equation (4) shows that the exponential function of (2) can be divided into subsections of $e^{\mathbf{A}/2n}$ and $e^{s\mathbf{B}/n}$. The matrix $e^{s\mathbf{B}/n}$ represents a lossless transmission line, which can be expressed in the time domain as delay algebraic equations [22], [23] and $e^{\mathbf{A}/2n}$ represents the attenuation matrix which can be modeled as resistances (Fig. 1). This fact will be used to derive an efficient delay and crosstalk model for coupled RLC interconnects.

III. Development of Delay and Crosstalk Model

The development of the proposed model begins with the description of the single RLC line case and then extends to coupled lines.

A. Single RLC Line Analysis

The frequency domain solution at the far end is expressed as

$$V_f = \frac{V_{in}}{(1+sR_sC_l)\cosh(\Gamma l) + \left(R_sY_0 + sC_lY_0^{-1}\right)\sinh(\Gamma l)} \tag{5}$$

where $\Gamma = \sqrt{YZ}$, R_s is the driver resistance at the near end, C_l is the load capacitance at the far end, and V_{in} is the input voltage (as shown in Fig. 1).

For ease of presentation and without loss of generality, the proposed model is derived for the case when the order of (4) is set to $n = 1$. The exponential function of (1) is approximated as

$$\begin{aligned} e^{\mathbf{A}+s\mathbf{B}} &\approx e^{\mathbf{A}/2}e^{s\mathbf{B}}e^{\mathbf{A}/2} \\ &= \begin{bmatrix} 1 & -Rl/2 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh(s\tau_n) & -\frac{1}{Y_n}\sinh(s\tau_n) \\ -Y_n\sinh(s\tau_n) & \cosh(s\tau_n) \end{bmatrix} \\ &\quad \cdot \begin{bmatrix} 1 & -Rl/2 \\ 0 & 1 \end{bmatrix} \end{aligned} \tag{6}$$

where $\tau_n = l\sqrt{LC}/n$ and $Y_n = \sqrt{C/L}$. Multiplying the matrices of (6) and equating the terms with (3) yields the following approximations:

$$\begin{aligned} \cosh(l\sqrt{ZY}) &\approx \cosh(s\tau_n) + \frac{RlY_n}{2}\sinh(s\tau_n) \\ Y_0^{-1}\sinh(l\sqrt{YZ}) &\approx Rl\cosh(s\tau_n) \\ &\quad + \left(\frac{1}{Y_n} + \frac{(Rl)^2Y_n}{4}\right)\sinh(s\tau_n) \\ Y_0\sinh(l\sqrt{YZ}) &\approx Y_n\sinh(s\tau_n) \\ \cosh(l\sqrt{YZ}) &\approx \cosh(s\tau_n) + \frac{RlY_n}{2}\sinh(s\tau_n) \end{aligned} \tag{7}$$

Using (7), the $cosh$ and $sinh$ functions of (5) can be expressed in the time domain as delay algebraic equations. Substituting (7) in (5) and taking the Laplace inverse results in a delay differential equation, as

$$\begin{aligned} \alpha_0V_f(t) + \beta_0\frac{dV_f(t)}{dt} + \alpha_1V_f(t-2\tau_n) + beta_1\frac{dV_f(t-2\tau_n)}{dt} \\ = 2V_{in}(t-\tau_n) \end{aligned} \tag{8}$$

where

$$\alpha_0 = 1 + \frac{RlY_n}{2} + R_sY_n \tag{9}$$

$$\beta_0 = R_sC_l\left(1+\frac{RlY_n}{2}\right) + C_l\left(Rl + \frac{1}{Y_n} + \frac{(Rl)^2Y_n}{4}\right) \tag{10}$$

$$\alpha_1 = 1 - \frac{RlY_n}{2} - R_sY_n \tag{11}$$

$$\beta_1 = R_sC_l\left(1-\frac{RlY_n}{2}\right) + C_l\left(Rl - \frac{1}{Y_n} - \frac{(Rl)^2Y_n}{4}\right) \tag{12}$$

Solving (8) using numerical integration techniques like Backward Euler's equation, (8) can be expressed as a delay algebraic equation

$$\begin{aligned} V_f(t) = \frac{1}{\left(\alpha_0 + \frac{\beta_0}{h}\right)}\Bigg(2V_{in}(t-\tau_n) + \frac{\beta_0}{h}V_f(t-h) \\ - \left(\alpha_1 + \frac{\beta_1}{h}\right)V_f(t-2\tau_n) + \frac{\beta_1}{h}V_f(t-2\tau_n-h)\Bigg) \end{aligned} \tag{13}$$

where h is the step size. For the general case when the order of (4) is set to $n = N$, the time domain expression of (5) is obtained in similar manner and is expressed as

$$\begin{aligned} V_f(t) = \alpha_0V_{in}(t-\tau_v) - \sum_{k=1}^{N}\alpha_kV_f(t-\tau^k) \\ - \sum_{k=1}^{N+1}\beta_kV_f(t-\tau^{k-1}-h) \end{aligned} \tag{14}$$

where $\tau_v = l\sqrt{LC}$, $\tau^k = 2k\tau_n$ and the values α_k and β_k are constant coefficients derived by substituting (4) in (5) and using Backward Euler's rule to convert to algebraic form.

B. Coupled RLC Line Analysis

A coupled RLC interconnect network with m coupled conductors is shown in Fig. 2. The frequency domain solution at the far end is expressed as

$$\boldsymbol{V}_f = (\boldsymbol{A}_T - s\boldsymbol{B}_T\boldsymbol{C}_L - \boldsymbol{R}_s\boldsymbol{C}_T + s\boldsymbol{R}_s\boldsymbol{D}_T\boldsymbol{C}_L)^{-1}\boldsymbol{V}_{in} \tag{15}$$

where $\boldsymbol{R}_s$ and $\boldsymbol{C}_l$ are diagonal matrices corresponding to the driver resistance matrix and load capacitance matrix, respectively; $\boldsymbol{V}_{in}$ is a vector corresponding to the applied input voltages at the near end of transmission line; the matrices $\boldsymbol{A}_T$, $\boldsymbol{B}_T$, $\boldsymbol{C}_T$, and $\boldsymbol{D}_T$ are defined as

$$\boldsymbol{A}_T = \cosh(l\sqrt{\boldsymbol{ZY}}) \tag{16}$$

$$\boldsymbol{B}_T = -\boldsymbol{Y}_0^{-1}\sinh(l\sqrt{\boldsymbol{YZ}}) \tag{17}$$

$$\boldsymbol{C}_T = -\boldsymbol{Y}_0\sinh(l\sqrt{\boldsymbol{YZ}}) \tag{18}$$

$$\boldsymbol{D}_T = \cosh(l\sqrt{\boldsymbol{YZ}}) \tag{19}$$

As explained in Section II, the modified Lie formula of (4), decomposes the exponential matrix of (1) into a cascade of resistive networks and lossless transmission lines. The resistive network modeled as $e^{\mathbf{A}/2n}$ represents a constant matrix as

$$e^{\frac{\mathbf{A}}{2n}} = \begin{bmatrix} \boldsymbol{I} & -(\boldsymbol{R}l)/(2n) \\ \mathbf{0} & \boldsymbol{I} \end{bmatrix} \tag{20}$$

where $\boldsymbol{I}$ is the identity matrix. The lossless transmission line is modeled as $e^{s\mathbf{B}/n}$ and requires eigenvalue analysis to express in the time domain as delay algebraic equations. For this purpose, the matrices $\boldsymbol{L}$ and $\boldsymbol{C}$ are converted to diagonal matrices as described in [23] as

$$\hat{\boldsymbol{L}} = \boldsymbol{E}_V^{-1}\boldsymbol{L}\boldsymbol{E}_I; \quad \hat{\boldsymbol{C}} = \boldsymbol{E}_I^{-1}\boldsymbol{C}\boldsymbol{E}_V; \quad \boldsymbol{E}_V^t = \boldsymbol{E}_I^{-1} \tag{21}$$

where $\boldsymbol{E}_V$ and $\boldsymbol{E}_I$ are constant matrices used to decouple the lossless transmission line; $\hat{\boldsymbol{L}}$ and $\hat{\boldsymbol{C}}$ are diagonal matrices of the form $\hat{\boldsymbol{L}} = diag\{l_1, l_2, \ldots, l_n\}$, $\hat{\boldsymbol{C}} = diag\{c_1, c_2, \ldots, c_n\}$, and the superscript t denotes the transpose of the matrix. Using (21), the exponential matrix $e^{s\mathbf{B}/n}$ is expressed as

$$e^{s\mathbf{B}/n} = \boldsymbol{M}_T^{-1} \begin{bmatrix} \cosh(s\boldsymbol{\tau}_n) & -\boldsymbol{Y}_n^{-1}\sinh(s\boldsymbol{\tau}_n) \\ -\boldsymbol{Y}_n \sinh(s\boldsymbol{\tau}_n) & \cosh(s\boldsymbol{\tau}_n) \end{bmatrix} \boldsymbol{M}_T \tag{22}$$

where the matrices $\boldsymbol{\tau}_n$, $\boldsymbol{Y}_n$, and $\boldsymbol{M}_T$ are defined as

$$\begin{aligned} \boldsymbol{\tau}_n &= \mathrm{diag}\{\sqrt{\mathrm{l_1 c_1}}, \sqrt{\mathrm{l_2 c_2}} \ldots., \sqrt{\mathrm{l_m c_m}}\} \\ &= \mathrm{diag}\{\tau_{\mathrm{n1}}, \tau_{\mathrm{n2}} \ldots., \tau_{\mathrm{nm}}\} \\ \boldsymbol{Y}_n &= \mathrm{diag}\{\sqrt{\mathrm{c_1/l_1}}, \sqrt{\mathrm{c_2/l_2}} \ldots., \sqrt{\mathrm{c_m/l_m}}\}; \\ \boldsymbol{M}_T &= \begin{bmatrix} \boldsymbol{E}_V & \mathbf{0} \\ \mathbf{0} & \boldsymbol{E}_I \end{bmatrix} \end{aligned} \tag{23}$$

and $\tau_{nk} = \sqrt{l_k c_k}$. Substituting $\cosh(s\tau_{nk}) = (e^{s\tau_{nk}} + e^{-s\tau_{nk}})/2$ and $\sinh(s\tau_{nk}) = (e^{s\tau_{nk}} - e^{-s\tau_{nk}})/2$ into (22) and multiplying the matrices yields (24), as shown at the bottom of the page, where $\boldsymbol{A}_k$, $\boldsymbol{B}_k$, $\boldsymbol{C}_k$, and $\boldsymbol{D}_k$ are constant matrices that result from the multiplication of (22).

Using (4), (20), and (24) in (15) and taking the Laplace inverse of (15) yields a delay differential algebraic equation which is solved using the Backward Euler's formula. The time domain expression of (15) can be approximated as

$$\boldsymbol{V}_f(t) = \sum_{k=1} \boldsymbol{\alpha}_{0,k} V_{in,k}\left(t - \tau_v^k\right) - \sum_{j=1}\sum_{k=1} \boldsymbol{\alpha}_{j,k} V_{f,k}\left(t - \tau_k^j\right) \tag{25}$$

where $\boldsymbol{\alpha}_{j,k} \in \Re^m$ are constant vectors and, $\tau_v^k = \sqrt{l_k c_k}$ and τ_k^j are the delay terms that are derived by substituting (4), (20), and (24) in (15) followed by the Backward Euler's formula to convert (15) into algebraic form. The values $V_{f,k}$ correspond to the output voltage of line k at the far end and $V_{in,k}$ correspond to the applied voltage of line k at the near end (Fig. 2).

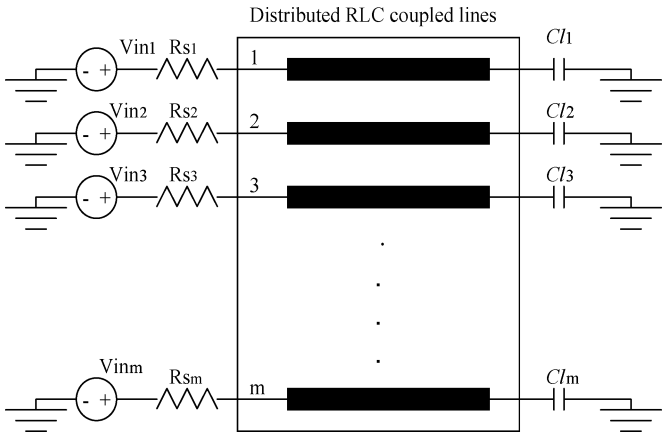

Fig. 2. Circuit model for m-coupled interconnects.

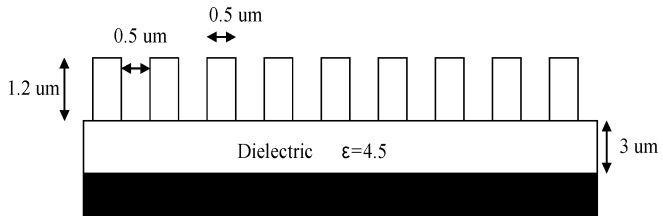

Fig. 3. Interconnect layout for example in Section IV.

Although (14) and (25) are solutions of the delay differential equation obtained by numerical integration techniques similar to that used in SPICE, the number of equation to be solved to obtain the far end transient response is equal to the number of lines only. In contrast, the number of equations to be solved by [22] would depend on the discretization involved in formulation of the MNA matrix. For the single-line example shown in Fig. 1, the number of MNA equations due to n sections will be $n * 6 + 1$ (six equations are required for the lossless line and resistance [23]). Thus, the proposed model provides a more efficient method to obtain the transient response for the case when the near and far ends of transmission lines are terminated with resistances and capacitances, respectively.

IV. Numerical Examples

A coupled RLC interconnect example is presented in this section to demonstrate the validity and efficiency of the proposed method. The results were obtained using MATLAB R2008a operating on DELL T7400 64-bit workstations with clock speed 3.16 GHz and are also compared with SPICE analysis. Within the context of this section SPICE analysis refers to using the conventional lumped model [24].

A nine-coupled on-chip line example of Fig. 3 is considered. The per-unit-length parameters of the example are obtained using the HSPICE field solver [24]. The line length is set to 1 cm. The driver resistances at the near end are each 50 Ω and the load capacitances at the far end are each 0.1 pF. For this example, $n = 6$ sections was used

$$e^{s\mathbf{B}/n} = \begin{bmatrix} \sum_{k=1}^{m}(\boldsymbol{A}_k e^{s\tau_{nk}} + \boldsymbol{A}_k e^{-s\tau_{nk}}) & \sum_{k=1}^{m}(\boldsymbol{B}_k e^{s\tau_{nk}} - \boldsymbol{B}_k e^{-s\tau_{nk}}) \\ \sum_{k=1}^{m}(\boldsymbol{C}_k e^{s\tau_{nk}} - \boldsymbol{C}_k e^{-s\tau_{nk}}) & \sum_{k=1}^{m}(\boldsymbol{D}_k e^{s\tau_{nk}} + \boldsymbol{D}_k e^{-s\tau_{nk}}) \end{bmatrix} \tag{24}$$

TABLE I
COMPARISONS OF 50% DELAY AND PEAK CROSSTALK OF PROPOSED MODEL WITH HSPICE AND DEPACT MACROMODEL FOR SWITCHING SCENARIOS

Switching Scenarios	Line Investigated	Signal Transients	HSPICE Conventional Lumped Model	DEPACT Macromodel (Order 6)	Proposed Model (Order 6)
0 ↑↑↑↑↑↑↑	Line 1	Peak Crosstalk (mV)	377.50	379.22	379.41
↑ 0 ↑↑↑↑↑↑	Line 2	Peak Crosstalk (mV)	553.02	557.00	557.44
↑↑ 0 ↑↑↑↑↑	Line 3	Peak Crosstalk (mV)	590.71	593.33	594.10
↑↑↑ 0 ↑↑↑↑	Line 4	Peak Crosstalk (mV)	604.50	603.85	601.77
↑↑↑↑ 0 ↑↑↑	Line 5	Peak Crosstalk (mV)	608.33	612.24	611.88
↑↓↓↓↓↓↓↓	Line 1	50 % Delay (ps)	279.00	277.00	277.45
↓↑↓↓↓↓↓↓	Line 2	50 % Delay (ps)	353.06	352.29	350.11
↓↓↑↓↓↓↓↓	Line 3	50 % Delay (ps)	354.03	352.67	352.33
↓↓↓↑↓↓↓↓	Line 4	50 % Delay (ps)	352.88	350.20	350.20
↓↓↓↓↑↓↓↓	Line 5	50 % Delay (ps)	352.55	350.11	350.18
Average Error % w.r.t. HSPICE lumped model				0.51	0.62
Maximum Error % w.r.t. HSPICE lumped model				0.72	0.85

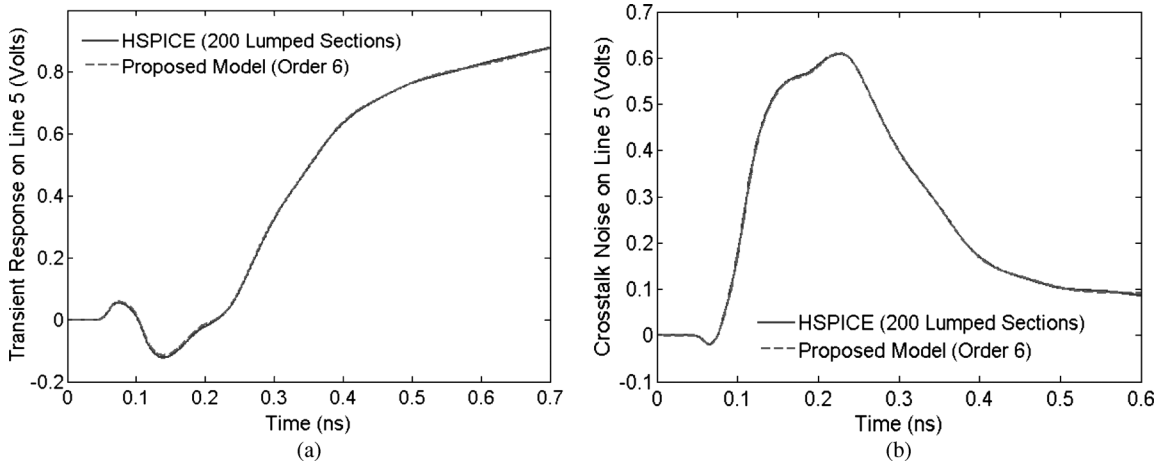

Fig. 4. Far end response for given example. (a) Transient response on line 5. Line 5 is active with rising ramp signals. All other lines are active with falling ramp inputs. (b) Crosstalk on line 5. Line 5 is quiet. All other lines are active with rising ramp inputs.

TABLE II
CPU COMPARISONS OF PROPOSED MODEL WITH DEPACT MACROMODEL AND HSPICE

CPU Expense using Proposed Model		CPU Expense using DEPACT macromodel		CPU Expense using HSPICE conventional lumped model			
Order n	CPU Time (s)	Order n	CPU Time (s)	No. of Lumped Sections	CPU Time (s)	No. of Lumped Sections	CPU Time (s)
6	0.65	6	3.44	26	39.16	200	267.96

to approximate the multiconductor line. The interconnect structure is examined for various switching scenarios as illustrated in Table I, where ↑ corresponds to a rising ramp input of 50 ps and ↓ corresponds to a falling ramp input of 50 ps. Fig. 4 compares the transient response for two different switching scenario using proposed model and SPICE lumped model using 200 sections.

Table II lists the CPU expense to solve (25) and compares the results with the DEPACT macromodel and SPICE analysis using 200 RLC lumped sections and the following rule of thumb $N_{RLC} = 20l\sqrt{LC}/T_r$ [24] where T_r is the rise time of the input signal; $\sqrt{LC}$ is the maximum eigenvalue of the matrix $\sqrt{\boldsymbol{LC}}$ for the coupled line case. The proposed model is roughly five times faster than [22], 50 times faster when 26 lumped sections are used and 400 faster than the SPICE when 200 lumped sections are used.

REFERENCES

[1] J. Rosenfeld and E. G. Friedman, "Design methodology for global resonant H-tree clock distribution networks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 2, pp. 135–148, Feb. 2007.
[2] D. Sylvester and C. Hu, "Analytic modeling and characterization of deep-submicron interconnect," *Proc. IEEE*, vol. 89, no. 5, pp. 634–664, May 2001.
[3] Y. I. Ismail and E. G. Friedman, *On-Chip Inductance in High Speed Integrated Circuits*. Norwell, MA: Kluwer Academic, 2001.
[4] R. Achar and M. Nakhla, "Simulation of high-speed interconnects," *Proc IEEE*, vol. 89, no. 5, pp. 693–728, May 2001.
[5] Y. Eo, S. Shin, W. R. Eisenstadt, and J. Shim, "Generalized traveling-wave-based waveform approximation technique for the efficient signal integrity verification of multicoupled transmission line system," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 12, pp. 1489–1497, Dec. 2002.

[6] W. C. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *J. Appl. Phys.*, vol. 19, no. 1, pp. 55–63, Jan. 1948.
[7] T. Sakurai, "Approximation of wiring delay in MOSFET LSI," *J. Solid-State Circuits*, vol. SC-18, no. 4, pp. 418–426, Aug. 1983.
[8] T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSIs," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 118–124, Jan. 1993.
[9] T. Sakurai, S. Kobayashi, and M. Noda, "Simple expressions for interconnection delay, coupling and crosstalk in VLSI's," in *Proc. Int. Symp. Circuits Syst.*, Jun. 1991, pp. 2375–2378.
[10] A. B. Kahng and S. Muddu, "An analytic delay model for RLC interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 16, no. 12, pp. 1507–1514, Dec. 1997.
[11] K. Bannerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 8, pp. 904–915, Aug. 2002.
[12] Y. Tanji and H. Asai, "Closed-form expressions of distributed RLC interconnects for analysis of on-chip inductance effects," in *Proc. IEEE Des. Autom. Conf.*, 2004, pp. 810–813.
[13] J. A. Davis and J. D. Meindl, "Compact distributed RLC interconnect models-Part I: Single line transient, time delay and overshoot expression," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2068–2077, Nov. 2000.
[14] J. A. Davis and J. D. Meindl, "Compact distributed RLC interconnect models-Part II: Coupled line transient expressions and peak crosstalk in multilevel networks," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2078–2087, Nov. 2000.
[15] R. Venkatesan, J. A. Davis, and J. D. Meindl, "Compact distributed RLC interconnect models-Part III: Transients in single and coupled line with capacitive load terminations," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1081–1093, Apr. 2003.
[16] R. Venkatesan, J. A. Davis, and J. D. Meindl, "Compact distributed RLC interconnect models-Part IV: Unified models for time delay, crosstalk and repeater insertion," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1094–1102, Apr. 2003.
[17] G. Chen and E. G. Freidman, "An RLC interconnect model based on Fourier analysis," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 2, pp. 170–183, Feb. 2005.
[18] S. Shin, Y. Eo, and W. R. Eisenstadt, "Analytic models and algorithms for the efficient signal integrity verification of inductance-effect-prominent multicoupled VLSI circuit interconnects," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 4, pp. 395–407, Apr. 2004.
[19] G. Servel, D. Deschacht, F. Saliou, J. Mattei, and F. Huret, "Inductance effect in crosstalk prediction," *IEEE Trans. Adv. Packag.*, vol. 25, no. 3, pp. 340–346, Aug. 2002.
[20] A. Naeemi, J. A. Davis, and J. D. Meindl, "Compact physical models for multilevel interconnect crosstalk in gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1902–1912, Nov. 2004.
[21] T. Kim and Y. Eo, "Analytic CAD models for the signal transients and crosstalk noise of inductance-effect-prominent multicoupled RLC interconnect lines," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 7, pp. 1214–1227, Jul. 2008.
[22] N. M. Nakhla, A. Dounavis, R. Achar, and M. S. Nakhla, "DEPACT: Delay extraction-based passive compact transmission-line macromodeling algorithm," *IEEE Trans. Adv. Packag.*, vol. 28, no. 1, pp. 13–23, Feb. 2005.
[23] C. R. Paul, *Analysis of Multiconductor Transmission Line*. New York: Wiley, 1994.
[24] *"Star-HSPICE Manual, Release 2001.2,"* Synopsis Inc., Santa Clara, CA, 2001.