Waveform Relaxation with Overlapping based Partitioning for Fast Transient Simulation of Package/Board Power Distribution Networks

Sourajeet Roy
Dept. of Electrical and Computer Engineering
University of Western Ontario
London, Ontario, Canada
sroy33@uwo.ca

Anestis Dounavis
Dept. of Electrical and Computer Engineering
University of Western Ontario
London, Ontario, Canada
adounavis@eng.uwo

***Abstract* — Modeling of power distribution networks in electronic packages requires the two dimensional discretization of the distributed power/ground planes which can be computationally expensive. Recently, the waveform relaxation algorithm has been proposed for fast transient simulation of power/ground planes. However, due to the strong coupling of each node in a two dimensional (2D) physical space, the relaxation iterations exhibit slow convergence and special techniques need to be adopted to ensure efficient convergence. In this work, a novel waveform relaxation algorithm based on physically partitioning the power/ground plane into smaller overlapping subcircuits is presented. The overlap between the subcircuits provides greater exchange of information per iteration leading to accelerated convergence of the waveform relaxation algorithm. A numerical example has been provided to illustrate the validity of the proposed algorithm over full SPICE simulations.**

Keywords- Convergence, delay extraction, power distribution networks, signal integrity, transmission lines, waveform relaxation

I. INTRODUCTION

With the progressive increase in operating frequencies, scaling of supply voltage and high switching speed of logic circuits, effects like ground bounce, electromagnetic interference (EMI) and simultaneous switching noise (SSN) arising in the power distribution networks (PDNs) can lead to undesirable voltage fluctuations in chip, board and packaging levels [1]. Hence PDNs are fast emerging as a critical area for signal integrity (SI) verification for high speed packages.

A popular methodology for modeling PDN structures is based on deriving equivalent circuit models that can be easily solved using commercial circuit simulators with integrated circuit emphasis like SPICE [2]-[7]. These equivalent circuit models are typically based on discretizing the planar structure into a mesh of transmission lines. Various SPICE models have been provided to represent these transmission line segments such as the conventional lumped model [4], W-element [5] and DEPACT [6]. However, irrespective of the model involved, due to the two dimensional (2D) discretization of the PDN structure, such models typically result in large number of circuit nodes and require correspondingly large CPU costs.

Recently, waveform relaxation (WR) algorithms have been reported to tackle the problem of large simulation costs of both on-chip and package/board PDNs [7], [8]. A key feature of these algorithms is that they are naturally parallelizable leading to significant savings when simulated on a multiprocessor platform. Despite the parallelizable nature of these algorithms, due to the strong two dimensional (2D) spatial coupling of nodes, both methods required special techniques to accelerate the convergence of the relaxation iterations. For example, the work of [8] assumes a regular distribution of the decoupling capacitors over the PDN structure and utilizes the localization of the transient noise provided by the decoupling capacitors to improve the convergence. However, the position and the electrical behavior of the decoupling capacitors may not be available in the early design cycles. Moreover, distribution of local decoupling capacitors depends on the position of the IC devices and may not be regular in nature, whereby the localization of the transient noise is no longer effective enough for fast convergence.

In this work, a new overlapping based waveform relaxation algorithm is proposed for the fast transient simulation of package/board PDNs. This overlap between the subcircuits provides greater exchange of information per iteration leading to accelerated convergence without the need of any assumption regarding the localization of the transient noise. A numerical example has been provided to illustrate the validity and efficiency of the proposed algorithm over full simulation of the equivalent SPICE circuit.

II. REVIEW OF THE DEPACT MACROMODELING OF POWER DISTRIBUTION NETWORKS

This section reviews the application of the DEPACT macromodel to PDN structures. For this purpose a single layer, rectangular package PDN is considered in Fig. 1(a). Traditional SPICE modeling of such structures requires the discretization of the 2D surface into rectangular unit cells as

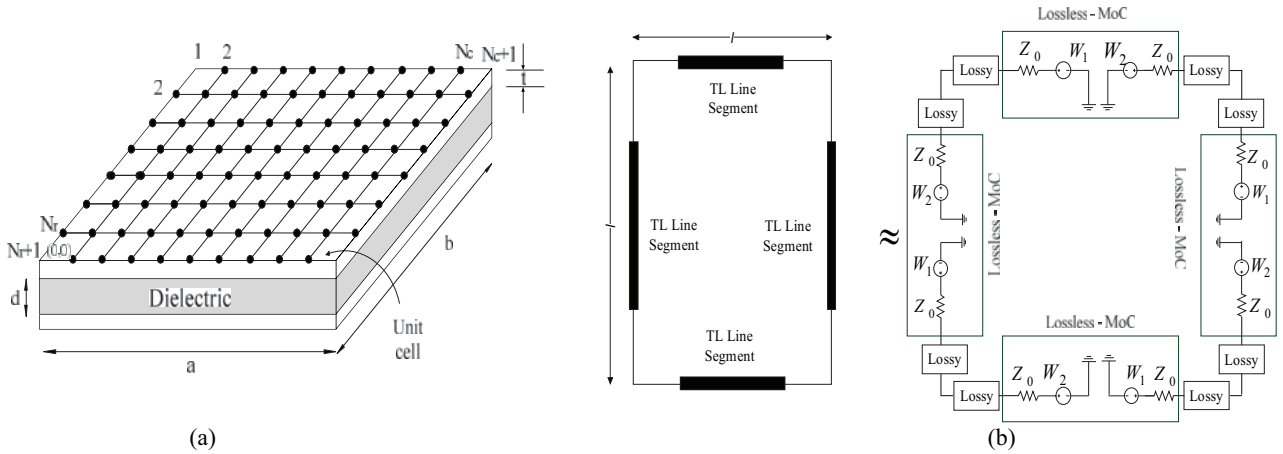

Fig. 1: Modeling of PDN. (a) Discretization of the structure into unit cells. (b) DEPACT modeling of each unit cell as seen from top view.

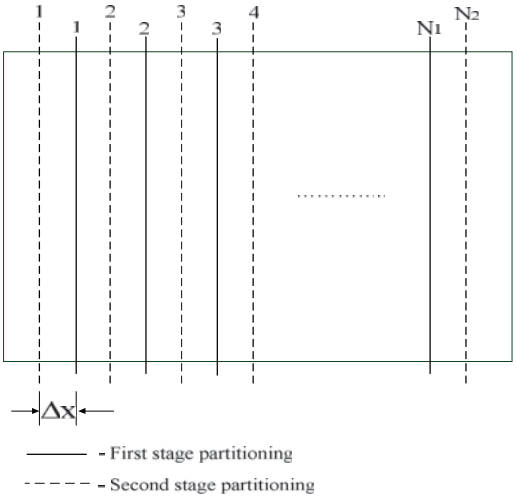

Fig. 2: Top view of the proposed partitioning scheme.

shown in Fig. 1(a) [2]-[6]. The equivalent circuit representing a unit cell can be obtained from the physical and material properties of the plane using a quasi-static model provided the dielectric separation between the power and ground plane pairs is much smaller compared to the dimensions of the plane [4]. Considering a square unit cell of dimensions (l) with a dielectric separation of (d) between planes, thickness of metal (t), metal conductivity (σ), loss tangent (δ) and relative permittivity (ε_r), the equivalent electrical parameters are

$$R = \frac{2}{\sigma t}, C = \varepsilon_o \varepsilon_r \frac{l^2}{d}, L = \mu_o d,$$
$$G = \omega C \tan(\delta), R_s = 2\sqrt{\frac{s\mu_0}{\sigma}} \quad (1)$$

where '$s = j2\pi f$' is the Laplace transform variable, 'f' is the instantaneous frequency, ε_o and μ_o are the permittivity and the permeability of free space, ε_r is the relative permittivity of the dielectric and R, L, C, G and R_s are the resistive, inductive, capacitive, conductive and skin effect losses contribution of the unit cell respectively [4]. Each unit cell can be modeled as a grid of 4 transmission lines segment where each line segment is represented by an equivalent circuit model using one DEPACT section as shown in Fig. 1(b) [6] and Z_0 is the characteristic impedance of each lossless segment while the sources W_1, W_2 arise from the method of characteristics (MoC) equations [9]. Combining the equivalent model of each cell, the DEPACT representation of the whole PDN is achieved. The following section explains the proposed overlapping based WR algorithm using the above DEPACT model of the PDN.

III. Proposed Waveform Relaxation Algorithm

A. Proposed Overlapping Partitioning Scheme

It is observed from Fig 1(a) that the circuit nodes of the discretized PDN are physically coupled in multiple directions in a 2D space to other nodes. As a result, large number of couplings needs to be resolved by the WR iterations, thereby requiring large number of iterations. To address this problem a novel partitioning methodology to discretize the PDN into overlapping subcircuits is presented.

In order to obtain the overlap between subcircuits, the PDN is partitioned in two stages. In the first stage (j = 1), the PDN is partitioned at regular intervals using N_1 partitioning interfaces into $N_1 + 1$ subcircuits as shown by the continuous lines of Fig. 2. At the second stage (j = 2), the same PDN structure is similarly partitioned using N_2 partitioning interfaces (broken lines in Fig. 2) into $N_2 + 1$ subcircuits, with the partitioning interfaces displaced by a distance Δx relative to the first stage.

The physical partitioning of Fig. 2 are all performed along the natural interfaces provided by the method of characteristics (MoC) as proposed in [8]. Considering any general i^{th} partitioning interface between i^{th} and $i+1^{th}$ subcircuits of the j^{th} partitioning stage (i.e. $j = 1$ for the solid lines of Fig. 2 and j = 2 for the broken lines of Fig. 2), there exists a total of $N_r + 1$ couplings between the above subcircuits where $N_r + 1$ is the

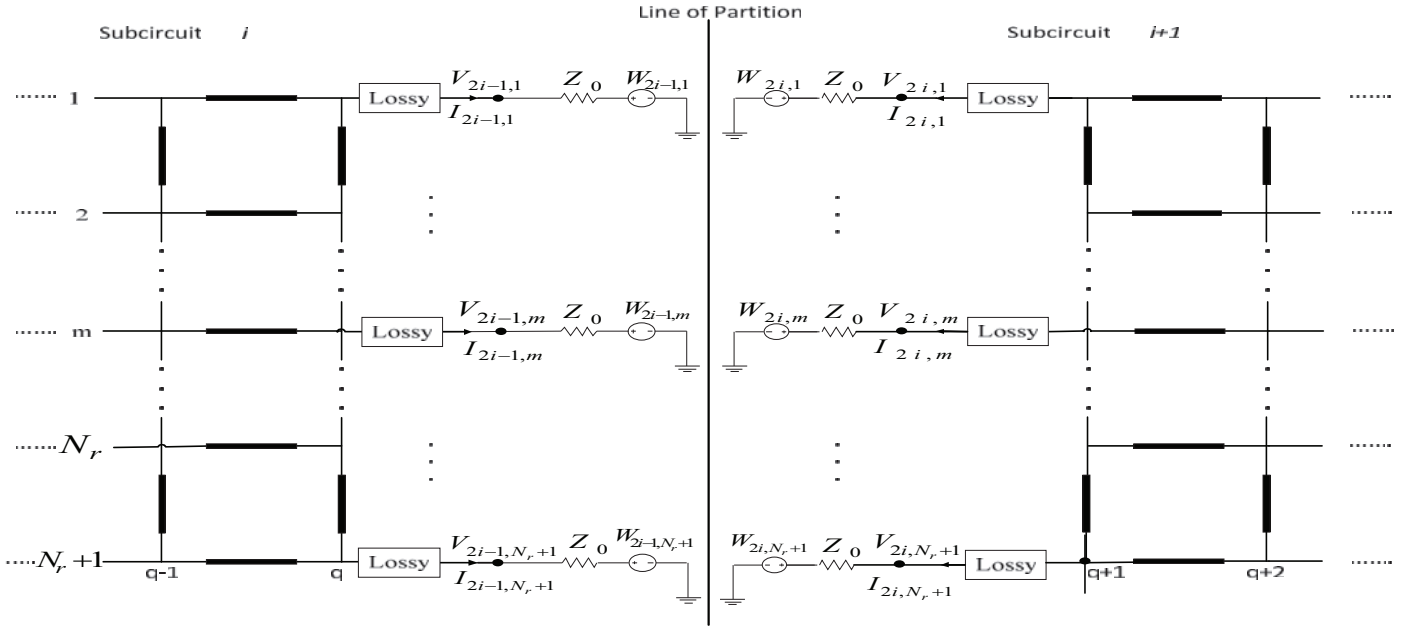

Fig. 3: Partitioning of the PDN parallel to the edges of the unit cell.

total rows achieved out of the discretization of Fig. 1(a), as illustrated in Fig. 3. The mathematical representation of the coupling at each such interface is given by the MoC equations [9]

$$\begin{aligned} W^{(j)}_{2i-1,m}(t) &= 2V^{(j)}_{2i,m}(t-\tau) - W^{(j)}_{2i,m}(t-\tau) \\ W^{(j)}_{2i,m}(t) &= 2V^{(j)}_{2i-1,m}(t-\tau) - W^{(j)}_{2i-1,m}(t-\tau); \quad 1 \le m \le N_r + 1 \end{aligned} \tag{2}$$

where $\tau = l\sqrt{LC/2}$ is the delay of the lossless section represented by MoC in Fig. 1(b) and the sources $W^{(j)}_{2i-1,m}(t)$, $W^{(j)}_{2i,m}(t)$ refer to the lumped sources arising from the MoC shown in Fig. 3. A crucial feature of the proposed partitioning methodology is that there exists a physical overlap of Δx between subcircuits of the first and second stages of partitioning. This corresponds to an overlap of $\Delta x/l$ columns of unit cells between the subcircuits which provide a greater exchange of information per iteration leading to accelerated convergence.

B. Iterative Solution of Subcircuits

It is observed from Fig. 2 that the PDN is partitioned into $N_1 + N_2 + 2$ subcircuits, where each subcircuit is coupled to the adjacent subcircuit across the i^{th} partitioning interface through the delayed sources $W^{(j)}_{2i-1,m}(t)$, $W^{(j)}_{2i,m}(t)$ (Fig. 3). Thus to begin the iterations, i.e. iteration count *k=0*, an initial guess of the waveforms of the relaxation sources $W^{(j,0)}_{2i-1,m}(t)$, $W^{(j,0)}_{2i,m}(t)$ is assumed where the additional superscript refers to the iteration count. Using the above relaxation sources as the excitation for the corresponding subcircuit, all the $N_1 + N_2 + 2$ subcircuits are solved individually either in sequence or in parallel. After any k^{th} iteration, the delayed sources need to be updated for the next $k+1^{th}$ iteration. This updating of the sources is done using the explicit MoC equations of (2) as

$$\begin{aligned} W^{(j,k+1)}_{2i-1,m}(t) &= 2V^{(j,k)}_{2i,m}(t-\tau) - W^{(j,k)}_{2i,m}(t-\tau) \\ W^{(j,k+1)}_{2i,m}(t) &= 2V^{(j,k)}_{2i-1,m}(t-\tau) - W^{(j,k)}_{2i-1,m}(t-\tau) \end{aligned} \tag{3}$$

where the terms on the right hand side of (3) are obtained from the previous (k^{th}) iteration. In order to consider the overlap between the subcircuits belonging to the first and second stage of partitioning, an additional constraint for updating the relaxation sources is used as below

$$\begin{aligned} W^{(1,k+1)}_{2i-1,m}(t) &= \alpha W^{(1,k+1)}_{2i-1,m}(t) + \beta W^{(2,k)}_{2i+(\Delta x/l)-1,m}(t) \\ W^{(1,k+1)}_{2i,m}(t) &= \alpha W^{(1,k+1)}_{2i,m}(t) + \beta W^{(2,k)}_{2i+(\Delta x/l),m}(t) \\ W^{(2,k+1)}_{2i-1,m}(t) &= \alpha W^{(1,k)}_{2i-(\Delta x/l)-1,m}(t) + \beta W^{(2,k+1)}_{2i-1,m}(t) \\ W^{(2,k+1)}_{2i,m}(t) &= \alpha W^{(1,k)}_{2i-(\Delta x/l),m}(t) + \beta W^{(2,k+1)}_{2i,m}(t) \end{aligned} \tag{4}$$

where α, β are the weights for the solution of each j^{th} partitioning stage and the waveforms of the right hand side of (4) are either already known from (3) (for waveforms with iteration count of *k+1*) or can be obtained from the previous (k^{th}) solution of the subcircits (for waveforms with iteration count of *k*). The displacement of the subscripts by $\Delta x/l$ ensures that only those relaxation sources located at the same position in both the first and second stage of partitioning are added together. Using the updated values of (4) as the new sources for the next $k+1^{th}$ iteration, the subcircuits are solved again. This cycle of iterations followed

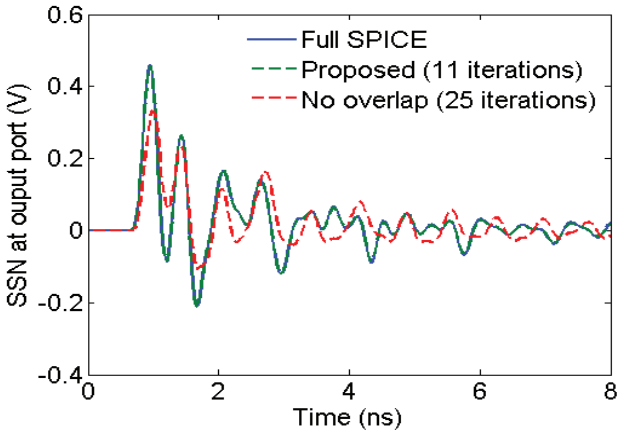

Fig. 4: Comparing the accuracy of proposed WR algorithm with full SPICE simulation.

by updating the relaxation sources continues till the absolute error satisfies a constraint as

$$\varepsilon = \frac{1}{2(N_r+1)}\left\{\frac{1}{N_1}\sum_{m=1}^{N_r+12N_1}\sum_{i=1}\left|W_{i,m}^{(1,k+1)} - W_{i,m}^{(1,k)}\right| + \frac{1}{N_2}\sum_{m=1}^{N_r+12N_2}\sum_{i=1}\left|W_{i,m}^{(2,k+`)} - W_{i,m}^{(2,k)}\right|\right\} \le \eta \quad (5)$$

where η is the predefined error tolerance.

IV. Numerical Example

An example is presented in this section to demonstrate the validity of the proposed waveform relaxation algorithm. The subcircuits for each iteration were solved and the relaxation sources updated using (3) in SPICE and a customized C++ code was used to automatically extract the waveforms for the relaxation sources and perform the additional overlap equation of (4). The invocation of SPICE and the C++ code for every subcircuit and iteration was automated using MATLAB 2010b.

A simple rectangular PDN of size a = 10 cm by b = 5 cm as shown in Fig. 1(a) is considered. The signal and ground planes are made of copper with thickness t = 0.025 mm, separated by a FR4 dielectric medium of thickness d = 1.11mm and dielectric constant $\varepsilon_r = 4.5$. The input is a ramp current signal of rise time $T_r = 0.2ns$ and amplitude of 0.1 A with a source resistance of 10 Ω in parallel. The input port is located at (9 cm, 4.5 cm) and the observation port is located at (0.5 cm, 0.5 cm). The DEPACT model of [6] required the discretization of the plane into 200 unit cells of dimensions l = 0.5 cm ($N_c = 20, N_r = 10$ in Fig. 1(b)).

To demonstrate the efficiency and accuracy of the proposed algorithm compared to traditional full SPICE solution, the PDN is solved using three techniques – the full SPICE solution using DEPACT [6], the WR algorithm of [8] without overlap and the proposed algorithm. For the work of [8], the PDN is partitioned column wise into 21 subcircuits. Meanwhile, the proposed algorithm partitions the PDN in the first stage into $N_1 = 11$ subcircuits and in the second stage into $N_2 = 11$ subcircuits as well. This ensures an overlap of Δx = 0.5 cm or $\Delta x / l$ = 1 unit cell between the subcircuits of the first and second stages of partitioning. In this work, the values of $\alpha = \beta = 0.5$ in (4) (i.e. equal weights are used for the overlapping of the subcircuits). Both the WR algorithms are performed using a Gauss-Jacobi iterative scheme where the computational cost is divided over 8 processors with the error tolerance set to $\varepsilon = 1e-5$. Figure 4 illustrates the accuracy of the proposed WR algorithm in comparison to the full SPICE simulation and the work of [8] where no overlap is involved. It is observed that without overlap, the WR algorithm fails to converge even after 25 iterations. On the other hand the proposed algorithm converges in 11 iterations. Considering the CPU expense, the full SPICE simulation requires 461 seconds to complete the transient analysis while the proposed algorithm uses only 118 seconds thereby providing a speed up of about 4 times.

References

[1] R.R. Tummala, E.J. Rymaszewski, and A.G. Klopfenstein, *Microelectronics Packaging Handbook, pt. I, second ed.* New York: Chapman Hall, 1997.

[2] I. Novak, "Reducing simultaneous switching noise and EMI on ground/power planes by dissipative edge termination," *IEEE Trans Adv. Packag.,* vol. 22, no. 3, pp. 274-283, Aug. 1999.

[3] K. Lee and A. Barber, "Modeling and analysis of multichip module power supply planes," *IEEE Trans Comp. Packag. and Manufacturing Tech.,* vol. 18, no. 4, pp. 628-639, Nov. 1995.

[4] J. H. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method," *IEEE Trans Adv. Packag.,* vol. 24, no. 3, pp. 334-346, Aug. 2001.

[5] L. Smith, R. Raymond, and T. Roy, "Power plane SPICE models and simulated performance for materials and geometries," *IEEE Trans. Adv. Packag.*, vol. 24, no. 3, pp. 277–287, Aug. 2001.

[6] S. Roy and A. Dounavis, "Efficient modeling of power/ground planes using delay extraction based transmission lines", *IEEE Trans.Components, Pachag. And Manuf. Tech.,* vol. 1, no. 5, pp. 761-771.

[7] R. Achar *et. al,* "Parallel and scalable transient simulator for power grids via waveform relaxation (PTS-PWR),". *IEEE Trans. VLSI Systs.,* vol. 19, no. 2, pp. 319-332.

[8] S. Roy and A. Dounavis, "Waveform relaxation based analysis of noise propagation in power distribution networks," in *Proc. 20th Topical Meeting Elect. Perform. Electron. Packag*, 2011, pp. 255–258.

[9] F. H. Branin, Jr., "Transient analysis of lossless transmission lines," *Proc. IEEE*, vol. 55, no. 11, pp. 2012–2013, Nov. 1967.