Waveform Relaxation based Analysis of Noise Propagation in Power Distribution Networks

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***Abstract*—In this paper, a waveform relaxation algorithm is presented to efficiently model power distribution networks. The proposed algorithm is based on physically partitioning the large circuit into smaller disjoint subcircuits. A key feature of the partitioning scheme is that it ensures that the noise injected by each transient source is localized within the subcircuit where the source resides thereby leading to efficient convergence of the algorithm. The iterative solution of the subcircuits is parallelizable and scales efficiently with the number of processors. A numerical example has been provided to illustrate the validity of the proposed algorithm over full SPICE simulations.**

Keywords- Convergence, delay extraction, power distribution networks, signal integrity, transmission lines, waveform relaxation

I. INTRODUCTION

With the progressive increase in operating frequencies, scaling of supply voltage and high switching speed of logic circuits, effects like ground bounce, electromagnetic interference (EMI) and delta-I noise arising in the power distribution networks (PDNs) can lead to undesirable voltage fluctuations in chip, board and packaging levels [1]-[2]. Hence PDNs are fast emerging as a critical area for signal integrity (SI) verification for high speed packages.

A popular methodology for modeling PDN structures is based on deriving equivalent circuit models that can be easily solved using commercial circuit simulators with integrated circuit (IC) emphasis like SPICE [2]-[7]. These equivalent circuit models are typically based on discretizing the planar structure into an orthogonal grid of transmission lines. Various SPICE models have been provided to represent these transmission line segments such as the conventional lumped model [4], W-element [5] and DEPACT [6]. However, irrespective of the accuracy of the model involved, due to the two dimensional (2D) discretization of the structure, such models typically result in large number of circuit nodes and correspondingly large CPU costs.

Recently, a waveform relaxation (WR) algorithm based on a lumped resistive-capacitive (RC) equivalent model for PDNs has been proposed for efficient SI analysis [7]. However, with the increase of switching speed in modern IC's, broadband macromodels capable of including inductive effects, propagation delay and skin effect losses need to be considered. In [6], the DEPACT macromodel was used to efficiently model PDNs while capturing the high frequency performance of the PDN with sufficient accuracy. Recent works have combined the DEPACT macromodel with waveform relaxation algorithms for transmission line problems where it has been shown that the natural interface of the MoC can be used to partition the transmission line networks into smaller disjoint subcircuits [9].

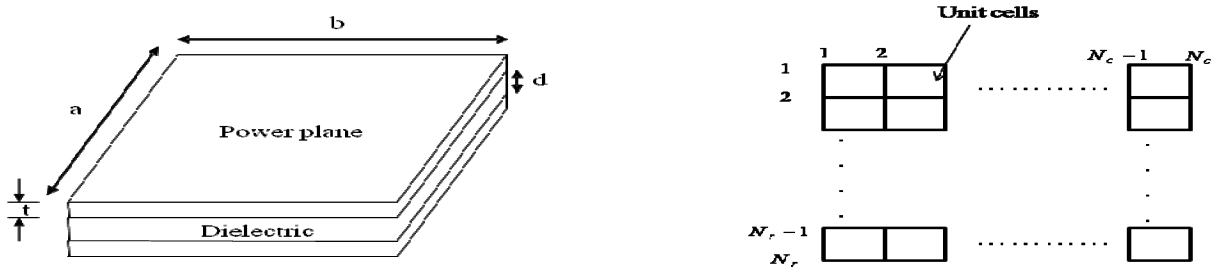
In this work, the DEPACT based waveform relaxation algorithm of [9] has been extended to PDNs. A methodology to physically partition the PDNs based on the location of the decoupling capacitors has been provided to improve the convergence of the WR algorithm. The proposed algorithm displays good scalability with number of CPUs. A numerical example has been provided to illustrate the validity and efficiency of the proposed over full simulation of the equivalent SPICE circuit.

II. REVIEW OF THE DEPACT MACROMODELING OF POWER DISTRIBUTION NETWORKS

This section reviews the application of the DEPACT macromodel to PDN structures.

A. PDN Modeling using DEPACT

Without loss of generality, a single layer, rectangular PDN is considered in Fig. 1(a). Traditional SPICE modeling of such structures requires the discretization of the 2D surface into rectangular unit cells as shown in Fig. 1(b) [2]-[7]. The equivalent circuit representing a unit cell can be obtained from the physical and electrical parameters of the plane using a quasi-static model provided the dielectric separation between the power and ground plane pairs is much smaller compared to the dimensions of the plane [4]. Considering a square unit cell of dimensions (l) with a dielectric separation of (d) between planes, thickness of metal (t), metal conductivity (σ), loss tangent (δ) and relative permittivity (ε_r), the equivalent electrical parameters are



(a) (b)

Fig. 1: Modeling of PDN based on discretization of the structure into unit cells. (a) Rectangular PDN structure. (b) Discretization of structure into unit cells.

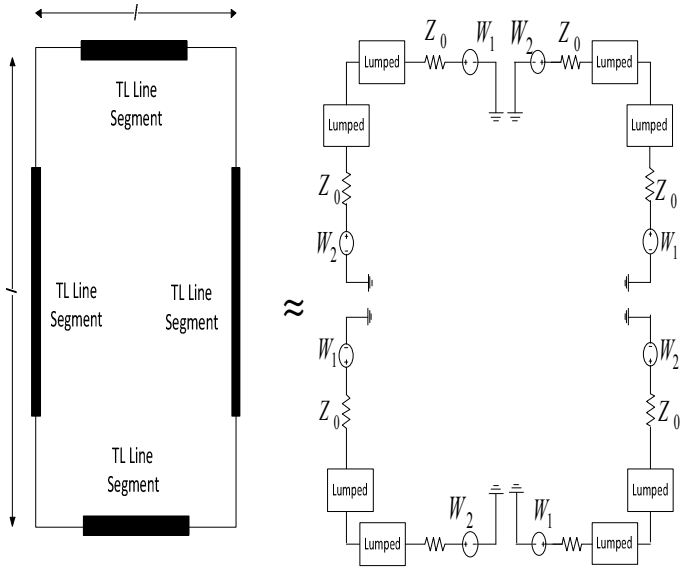


Fig. 2: DEPACT representation of unit cell.

$$\widetilde{R} = \frac{2}{\sigma t}, \widetilde{C} = \varepsilon_o \varepsilon_r \frac{l^2}{d}, \widetilde{L} = \mu_o d,$$
$$\widetilde{G} = \omega C \tan(\delta), \widetilde{R}_s = 2\sqrt{\frac{s\mu_0}{\sigma}} \quad (1)$$

where '$s = j2\pi f$' is the Laplace transform variable, 'f' is the instantaneous frequency, ε_o and μ_o are the permittivity and the permeability of free space, ε_r is the relative permittivity of the dielectric and $\widetilde{R}, \widetilde{L}, \widetilde{C}, \widetilde{G}$ and $\widetilde{R}_s$ are the resistive, inductive, capacitive, conductive and skin effect losses contribution of the unit cell respectively [4]. Each unit cell can be modeled as a grid of 4 transmission lines segment where each line segment is represented by an equivalent circuit model using one DEPACT section as shown in Fig. 2. The lumped block represents the attenuation losses modeled using lumped circuit elements, Z_0 is the characteristic impedance of lossless line segment and the sources W_1, W_2 arise from the MoC equations [6]. Combining the equivalent model of each cell, the DEPACT model of the PDN is achieved. The following section explains the proposed WR based on the above DEPACT model of the PDN.

III. Proposed Waveform Relaxation Algorithm

This section describes the methodology to physical partition the PDN structure into disjoint subcircuits and the WR algorithm to iteratively solve the subcircuits.

A. Proposed Partitioning Scheme

The application of WR algorithms for PDN structures may suffer from slow convergence due to the fact that the circuit nodes of the discretized PDN are physically coupled in 2D space to other nodes [7]. As a result, large number of couplings needs to be resolved by the WR iterations, thereby requiring large number of iterations.

One methodology to ensure efficient convergence of WR algorithms for PDNs is to localize the noise contribution by each transient source within the subcircuit where the source is located [7]. This ensures that the noise propagation between the subcircuit from which the noise originates (active subciruit) to the remaining subcircuits (victim subcircuits) via the coupling is weak. As a result the propagated signal causes only small transient perturbations above the steady state response of the victim subcircuits and the steady state response of the PDN serves as good initial guess for the iterations leading to rapid convergence [7].

In the proposed work, a partitioning methodology is provided that ensures reasonable localization of the noise signal within the subcircuit of origin. This partitioning scheme is based on the fact that typical PDN designs include array of decoupling capacitors spread over the entire plane for the dedicated purpose of providing a low impedance path for the delta-I noise. Hence, by including sufficient decoupling capacitors within each subcircuit, the current drain paths required for the localization of the noise within the subcircuit is satisfied. This ensures that the noise signal coupled to the victim subcircuits is relatively weak. It has been demonstrated with a numerical example that even a few decoupling capacitors within a subcircuit leads to a significant improvement in the convergence properties. In this work, the actual physical partitioning of the PDNs is performed along a line parallel to the rows/columns of the orthogonal grid using the natural MoC interfaces as proposed in [6] and shown in Fig. 3.

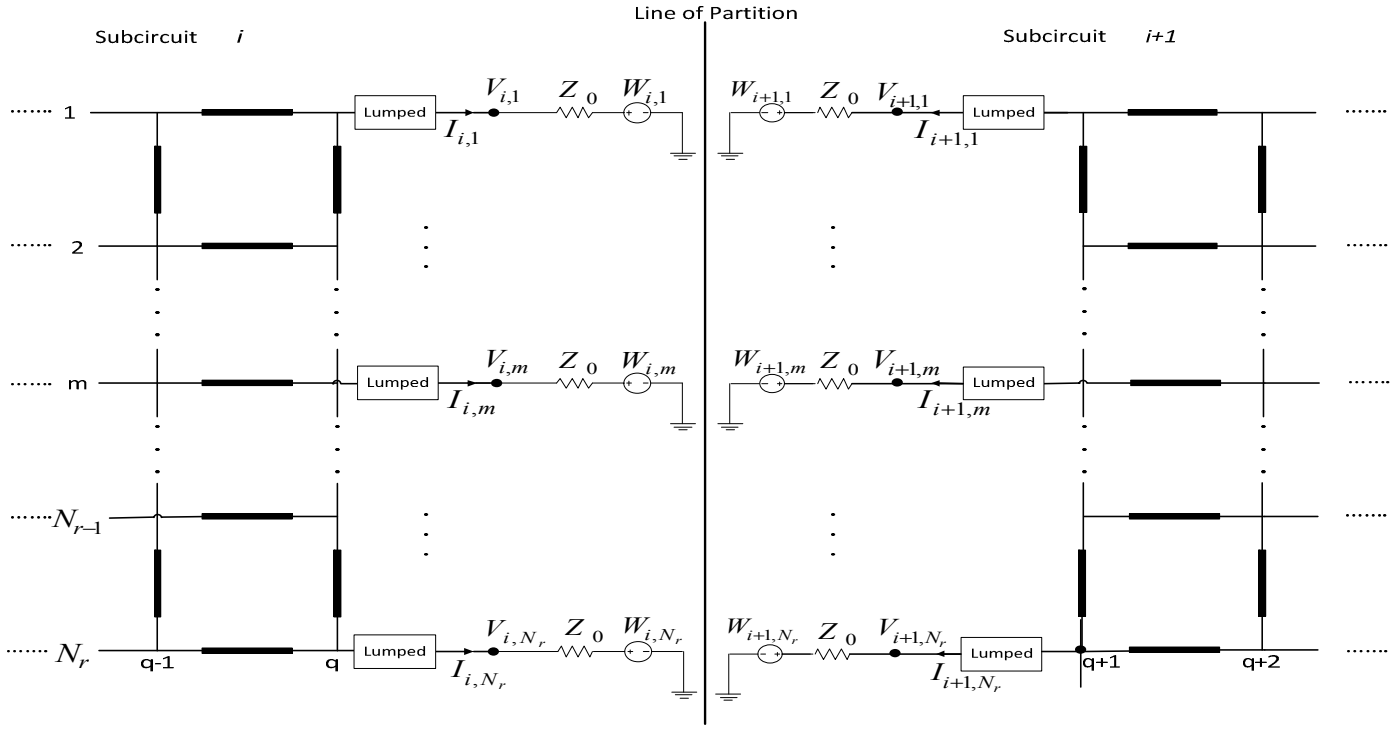


Fig. 3: Partitioning of the PDN parallel to the edges of the unit cell.

Figure 3 illustrates the partitioning between the q^{th} and $q+1^{\text{th}}$ column of the orthogonal grid to separate the i^{th} and the $i+1^{\text{th}}$ subcircuit. For this partition, there exists a total of N_r coupling between the subcircuits where N_r is the total rows obtained from the discretization of Fig. 1(b). The coupling between these two subcircuits are governed by the MoC equations given as

$$\begin{aligned} W_{i,m}(t) &= 2V_{i+1,m}(t-\tau) - W_{i+1,m}(t-\tau) \\ W_{i+1,m}(t) &= 2V_{i,m}(t-\tau) - W_{i,m}(t-\tau); \quad 1 \le m \le N_r \end{aligned} \tag{7}$$

The following section explains the iterative algorithm to solve the subcircuits.

B. Iterative Solution of Subcircuits

For every iteration k, an initial guess of the relaxation sources $W_{i,m}^{(k-1)}(t)$, $1 \le i \le N$, $1 \le m \le N_r$ are used to excite the corresponding i^{th} subcircuits and N is the total number of subcircuits. All the subcircuits are solved individually either in sequence or in parallel. A Gauss-Jacobi iterative algorithm requires the subcircuits to be solved with the condition (Fig. 3)

$$\begin{aligned} V_{i,m}^{(k)}(t) &= Z_0 I_{i,m}^{(k)}(t) + W_{i,m}^{(k-1)}(t) \\ V_{i+1,m}^{(k)}(t) &= Z_0 I_{i+1,m}^{(k)}(t) + W_{i+1,m}^{(k-1)}(t) \end{aligned} \tag{8}$$

On completion of the solving of each subcircuit, the results of (8) is used to update the relaxation sources as

$$\begin{aligned} W_{i,m}^{(k)}(t) &= 2V_{i+1,m}^{(k)}(t-\tau) - W_{i+1,m}^{(k-1)}(t-\tau) \\ W_{i+1,m}^{(k)}(t) &= 2V_{i,m}^{(k)}(t-\tau) - W_{i,m}^{(k-1)}(t-\tau) \end{aligned} \tag{9}$$

Using the updated values of (9) as the new sources for the next $k+1^{th}$ iteration, the subcircuits are solved again. This cycle of iterations followed by updating the relaxation sources continues till the absolute error satisfies

$$\varepsilon = \frac{1}{Np}\sum_{m=1}^{p}\sum_{i=1}^{N}\left|W_{i,m}^{(k+1)} - W_{i,m}^{(k)}\right| \le \eta \tag{10}$$

where η is the predefined error tolerance.

IV. Numerical Example

An example is presented in this section to demonstrate the validity of the proposed WR algorithm. The subcircuits for each iteration were solved and the relaxation sources updated using (9) in SPICE and a customized C++ code was used to automatically extract the waveforms for the relaxation sources. The invocation of SPICE and the C++ code for every subcircuit and iteration was automated using MATLAB 2010b.

A simple rectangular PDN of size 10 cm by 10 cm as shown in Fig. 4 is considered. The signal and ground planes are made of copper of thickness t = 0.025 mm and separated by a d = 0.7 mm thick FR4 dielectric. The input is a ramp current signal of rise time $T_r = 0.1ns$ and amplitude of 0.5 A with a source resistance of 10 Ω in parallel. The input port is

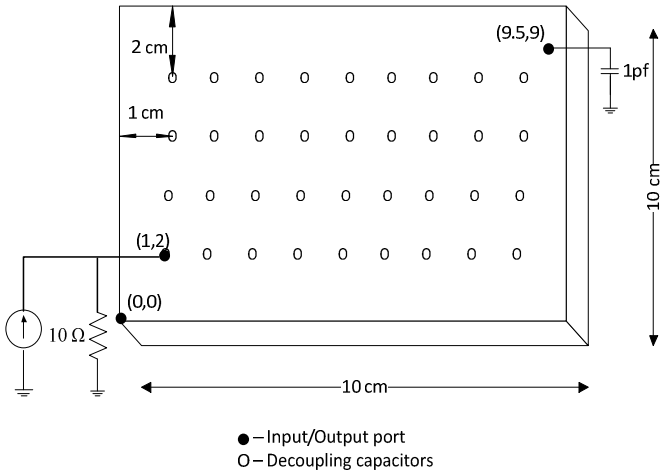


Fig. 4: Top view of the PDN structure considered.

TABLE I
COMPARISON OF CPU COST

Proposed algorithm (Gauss-Jacobi)		Full SPICE Simulation	Speed Up
# Processors	CPU Cost (sec)	CPU Cost (sec)	
1	501.35	577.60	1.15
2	266.60		2.16
4	126.80		4.55
8	87.80		6.58

located at (1 cm, 2cm) and the observation port at (9.5 cm, 9 cm). A regular distribution of decoupling capacitors modeled as a series RLC circuit of $R_d = 0.1\Omega$, $L_d = 2nH$ and $C_d = 10nF$ (as in [4]) was considered evenly distributed as shown in Fig. 4. The DEPACT model of [6] required the discretization of the plane into 400 square unit cells of dimensions 0.5 cm ($N_c = N_r = 21$ of Fig. 1(b)).

Based on the proposed partitioning scheme, the PDN is partitioned into 9 subcircuits where each subcircuit has dimensions of 10 cm by 1cm. The above partitioning ensures the presence of a column of decoupling capacitors in each subcircuit as natural drain paths for that subcircuit. To compare the convergence properties, a blind partitioning schemes using the same DEPACT model is also implemented where each column of the PDN grid is treated as a separate subcircuit leading to a total of 21 subcircuits, each subcircuit corresponding to a column of the PDN grid. It is noted that such blind partitioning schemes do not take into account the proposed attempt at noise localization as each subcircuit may not contain any decoupling capacitors and depend heavily on the adjacent subcircuits for its current requirements. It is observed that the proposed partitioning scheme converges within 8 iterations for an error tolerance of $\varepsilon = 1e-4$ while the blind partitioning scheme requires 18 iterations.

Next, Fig. 5 compares the noise propagated from the input port to the output port as predicted using the proposed WR algorithm and the full SPICE simulation using the DEPACT

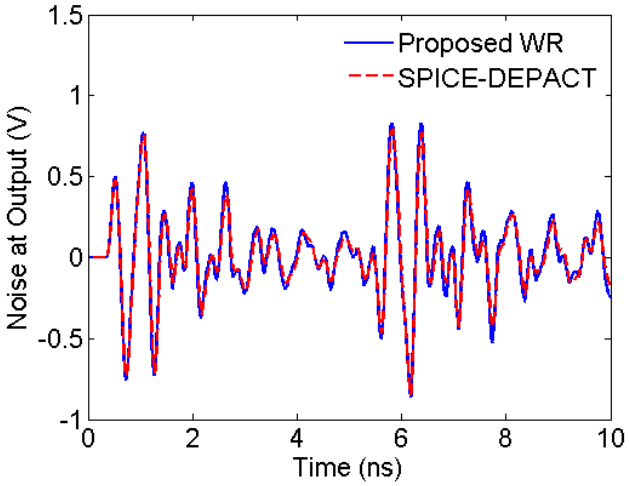


Fig. 5: Comparing the accuracy of proposed WR algorithm with full SPICE simulation.

macromodel of [6]. It is shown that the proposed algorithm shows good agreement with the full SPICE simulation.

Finally the scalability of the proposed algorithm is illustrated by performing the above analysis using the Gauss-Jacobi variation of the iterations with parallel processing of the subcircuits. The results are shown in Table I. It is observed that the proposed algorithm is highly parallelizable and that there is a significant scaling of the CPU cost as the number of processors increases.

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