RLC Interconnect Modeling using Delay Algebraic Equations

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***Abstract*— This paper presents a model for fast transient analysis for single line resistance-inductance-capacitance (RLC) on-chip interconnects. The proposed algorithm, based on a modified Lie formula, is used to convert the solution of the transmission line network into delay algebraic equations, which can be solved in a closed form manner. The proposed algorithm is not limited to fixed number of coupled RLC lines or to specific topologies and can be used to model both identical and non-identical multi-conductor lines and loads.**

I. Introduction

As modern generation of integrated circuit (IC) technology size decreases, clock speeds are expected to increase beyond the 10 GHz range [1]. However to eliminate large interconnect latencies, scaling of interconnect geometries has not been so rapid, leading to longer wire delays [2]. At such high speeds of operation, the high-frequency effects in the inductively-prominent on-chip interconnect ceases to be negligible [3], [4]. Moreover with the diminishing size of modern VLSI circuits, the inductive coupling of the on-chip interconnect affect a substantially larger physical area of the IC [5]. Thus signal integrity impairment owing to effects like attenuation, crosstalk, ringing and spurious glitches are a primary source of concern for modern IC designers. Although accurate SPICE simulation techniques for coupled RLC interconnects do exist [4], such methods use numerical integration or convolution which is computationally expensive for layout optimizations in early stages of the design cycles. For iterative layout design of densely populated ICs, accurate analytic models are needed to efficiently predict the transient response of RLC interconnects.

In the past, on-chip interconnects were modeled as RC lines and single pole Elmore-based models [6]-[9] were most widely used to estimate signal delay. However, in current integrated circuit designs, wire inductance can no longer be ignored due to higher operating speeds and RLC models are required. As a result, the issue of developing closed form expressions for far end response of RLC interconnects has been a topic of intense research [10]-[19]. However, these algorithms may have limitations in accuracy, due to the type of approximations made to derive the models. For example, the Bessel function model of [13]-[16] is not suitable for coupled line structures beyond three coupled lines due to the model complexity involved and [17] assumes periodic input and provides steady state solution only.

In [20], the DEPACT algorithm is developed for SPICE analysis of high speed interconnects. The formulation of [20] uses modified nodal analysis (MNA) to describe the network equations and provides the complete solution for both the far end and near end responses of interconnects for any linear and nonlinear load terminations. In this paper, the concepts developed in [20] are further extended to create an efficient solution algorithm for the far end responses of coupled RLC interconnects when the lines are terminated by resistances and capacitances as discussed in the literature [7]-[19]. The method approximates the transfer function for the far end of a single line as one delay algebraic equation only and does not use the MNA formulation. As a result, the proposed algorithm will be significantly faster for solving the far end responses compared to [20] for the case when the near and far end of the lines are terminated with resistances and capacitances, respectively. This will be illustrated with numerical examples in section IV.

II. Analysis of Single RLC Interconnect

This section briefly reviews the transmission line theory and describes the DEPACT algorithm [20] which will be used to develop the proposed delay model.

The solution of Telegraphers equations for on-chip RLC interconnects are can be written as an exponential matrix function as

$$\begin{bmatrix} V(l,s) \\ -I(l,s) \end{bmatrix} = e^{\boldsymbol{\Phi}} \begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix} \tag{1}$$

where

$$\boldsymbol{\Phi} = \boldsymbol{A} + s\boldsymbol{B}; \quad \boldsymbol{A} = \begin{bmatrix} 0 & -Rl \\ 0 & 0 \end{bmatrix}; \quad \boldsymbol{B} = \begin{bmatrix} 0 & -Ll \\ Cl & 0 \end{bmatrix} \tag{2}$$

's' is Laplace transform variable; V and I represent the terminal voltage and current variables of the transmission line, respectively; R, L and C are the per-unit-length resistance, inductance and capacitance matrices, respectively and l is the length of the transmission line. The exponential matrix of (1) can be subdivided into four block matrices described in terms of *cosh* and *sinh* functions as

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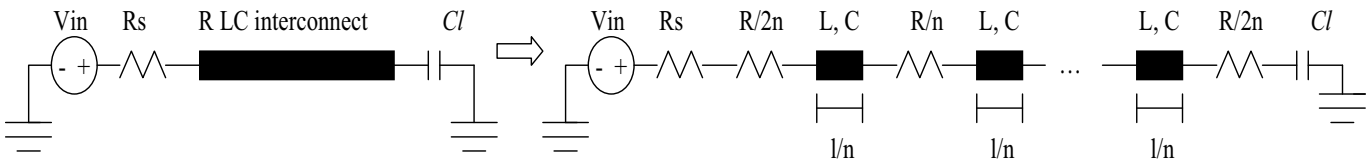


Fig. 1 Circuit model of distributed RLC interconnect

$$e^{\begin{bmatrix} 0 & -(\boldsymbol{R}+s\boldsymbol{L})l \\ -s\boldsymbol{C}l & 0 \end{bmatrix}} = \begin{bmatrix} \cosh(l\sqrt{ZY}) & -Y_0^{-1}\sinh(l\sqrt{YZ}) \\ -Y_0\sinh(l\sqrt{YZ}) & \cosh(l\sqrt{YZ}) \end{bmatrix} \quad (3)$$

where $Y_0 = \sqrt{Y/Z}$, $Z = (R + sL)$ and $Y = sC$. Equation (1) does not have a direct representation in the time-domain which makes it difficult to analytically predict the delay of transmission lines.

A. Review of DEPACT Model

The basic idea of the DEPACT algorithm is to separate the delay terms from $e^{(\mathbf{A}+s\mathbf{B})}$, however, this is not a simple task since the matrices $\boldsymbol{A}$ and s$\boldsymbol{B}$ do not commute, (i.e. $e^{(\mathbf{A}+s\mathbf{B})} \neq e^{\mathbf{A}}e^{s\mathbf{B}}$). To approximate $e^{(\mathbf{A}+s\mathbf{B})}$ in terms of a product of exponentials, a modified Lie product is used as

$$e^{\mathbf{A}+s\mathbf{B}} \approx \prod_{i=1}^{n} \boldsymbol{\Psi}_i + \varepsilon_n \quad \text{and} \quad \boldsymbol{\Psi}_i = e^{\frac{\mathbf{A}}{2n}} e^{s\frac{\mathbf{B}}{n}} e^{\frac{\mathbf{A}}{2n}} \quad (4)$$

where *'n'* is the number of sections. The associated error of the approximation is $\| \varepsilon_n \| \cong O(1/n^2)$. Provided sufficient lumped sections, '*n*', is used, the convergence of the modified Lie product is guaranteed [20]. Equation (4) shows that the exponential function of (2) can be divided into subsections of $e^{\mathbf{A}/2n}$ and $e^{s\mathbf{B}/n}$. The matrix $e^{s\mathbf{B}/n}$ represents a lossless transmission line, which can be expressed in the time domain as delay algebraic equations [20], [21] and $e^{\mathbf{A}/2n}$ represents the attenuation matrix which can be modeled as resistances. This fact will be used to derive an efficient delay model for single line RLC interconnects.

III. Development of Delay Model

The development of the proposed model begins with the description of the single RLC line case. The frequency domain solution at the far end is expressed as

$$V_f = \frac{V_{in}}{(1 + sR_sC_l)\cosh(\Gamma l) + (R_sY_0 + sC_lY_0^{-1})\sinh(\Gamma l)} \quad (5)$$

where $\Gamma = \sqrt{YZ}$, R_s is the driver resistance at the near end, C_l is the load capacitance at the far end and V_{in} is the input voltage (as shown in Fig. 1).

TABLE I
Variation of p.u.l. Parameters with Interconnect Width in Example 1

Interconnect Width (*w*) μm	P.u.l. resistance (R) Ω/cm	P.u.l. inductance (L) nH/cm	P.u.l. capacitance (C) pF/cm
2	71.8	12.468	1.228
5	28.7	10.645	1.808
10	14.4	9.276	2.776

For ease of presentation and without loss of generality, the proposed model is derived for the case when the order of (4) is set to *n*=1. The exponential function of (1) is approximated as

$$e^{\mathbf{A}+s\mathbf{B}} \approx e^{\mathbf{A}/2}e^{s\mathbf{B}}e^{\mathbf{A}/2} = \begin{bmatrix} 1 & -Rl/2 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh(s\tau_n) & -\frac{1}{Y_n}\sinh(s\tau_n) \\ -Y_n\sinh(s\tau_n) & \cosh(s\tau_n) \end{bmatrix} \cdot \begin{bmatrix} 1 & -Rl/2 \\ 0 & 1 \end{bmatrix} \quad (6)$$

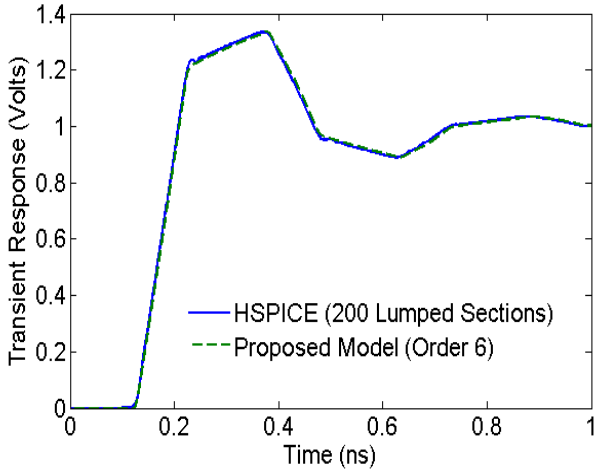
where $\tau_n = l\sqrt{LC}/n$ and $Y_n = \sqrt{C/L}$. Multiplying the matrices of (6) and equating the terms with (3) yields the following approximations

$$\begin{aligned} \cosh(l\sqrt{ZY}) &\approx \cosh(s\tau_n) + \frac{RlY_n}{2}\sinh(s\tau_n) \\ Y_0^{-1}\sinh(l\sqrt{YZ}) &\approx Rl\cosh(s\tau_n) + \left(\frac{1}{Y_n} + \frac{(Rl)^2Y_n}{4}\right)\sinh(s\tau_n) \\ Y_0\sinh(l\sqrt{YZ}) &\approx Y_n\sinh(s\tau_n) \\ \cosh(l\sqrt{YZ}) &\approx \cosh(s\tau_n) + \frac{RlY_n}{2}\sinh(s\tau_n) \end{aligned} \quad (7)$$

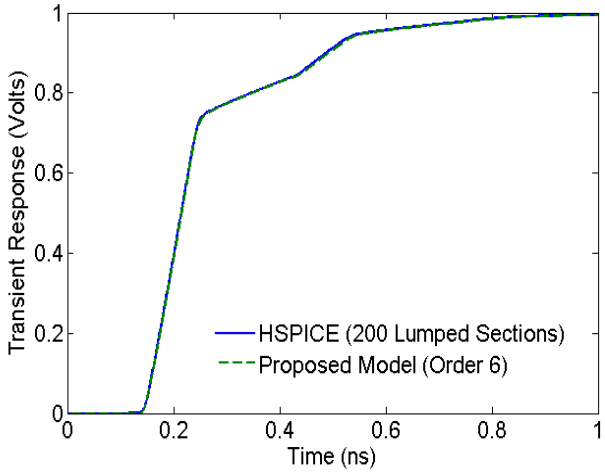
Using (7), the *cosh* and *sinh* functions of (5) can be expressed in the time domain as delay algebraic equations. Substituting (7) in (5) and taking the Laplace inverse results in a delay differential equation, as

$$\alpha_0 V_f(t) + \beta_0\frac{dV_f(t)}{dt} + \alpha_1 V_f(t-2\tau_n) + \beta_1\frac{dV_f(t-2\tau_n)}{dt} = 2V_{in}(t-\tau_n) \quad (8)$$

where



(a)



(b)

Fig. 2: Transient response for far end. (a) Line width (w) is 2µm, Rs=20 Ω, Cl=10 fF. (b) Line width (w) is 5µm, Rs=100 Ω, Cl=100 fF.

TABLE II
COMPARISONS OF 50% DELAY AND OVERSHOOT OF PROPOSED MODEL WITH HSPICE, DEPACT MACROMODEL AND MODIFIED BESSEL FUNCTION MODEL. THE LINE LENGTH IS 1 CM. (EXAMPLE 1)

Width (µm)	Rs (Ω)	Cl (fF)	HSPICE Conventional Lumped Model (200 Lumped Sections)		DEPACT Macromodel (Order 6)		Proposed Model (Order 6)		Bessel Function Model using 3 Reflections and 1st Order Bessel Function	
			50% Delay (ps)	Overshoot (V)	50% Delay (ps)	Overshoot (V)	50% Delay (ps)	Overshoot (V)	50% Delay (ps)	Overshoot (V)
2	20	10	167.11	1.333	166.75	1.339	168.46	1.338	166.78	1.325
	50	50	181.20	1.145	180.93	1.144	180.99	1.146	180.60	1.140
	100	100	202.40	1.000	202.00	1.000	202.26	1.000	201.80	1.000
5	20	10	177.61	1.368	177.21	1.417	178.62	1.413	177.00	1.407
	50	50	192.00	1.118	191.78	1.128	192.34	1.122	191.46	1.128
	100	100	215.63	1.000	214.67	1.000	215.49	1.000	214.77	1.000
10	20	10	199.15	1.377	198.89	1.380	200.25	1.382	198.84	1.389
	50	50	216.00	1.042	216.25	1.042	216.60	1.040	216.34	1.040
	100	100	242.33	1.000	242.11	1.000	242.14	1.000	241.94	1.000
Average Error %					0.19	0.58	0.30	0.52	0.29	0.65
Maximum Error %					0.44	3.58	0.81	3.29	0.40	2.85

TABLE III
CPU COMPARISONS OF PROPOSED MODEL WITH MODIFIED BESSEL FUNCTION MODEL, DEPACT MACROMODEL AND HSPICE FOR EXAMPLE 1

Width (µm)	CPU Expense for Example 1 using Proposed Model		CPU Expense for Example 1 using Modified Bessel Function Model		CPU Expense for Example 1 using DEPACT Macromodel		CPU Expense for Example 1 using HSPICE Conventional Lumped Model			
	Order n	CPU Time (ms)	Order of Bessel Function	CPU Time (ms)	Order n	CPU Time (ms)	No. of Lumped Sections (Equation (30))	CPU Time (ms)	No. of Lumped Sections	CPU Time (ms)
2	6	0.071	1	0.450	6	10	25	29	200	300
5							28	30		
10							32	35		

$$\alpha_0 = 1 + \frac{RlY_n}{2} + R_s Y_n \tag{9}$$

$$\beta_0 = R_s C_l (1 + \frac{RlY_n}{2}) + C_l (Rl + \frac{1}{Y_n} + \frac{(Rl)^2 Y_n}{4}) \tag{10}$$

$$\alpha_1 = 1 - \frac{RlY_n}{2} - R_s Y_n \tag{11}$$

$$\beta_1 = R_s C_l (1 - \frac{RlY_n}{2}) + C_l (Rl - \frac{1}{Y_n} - \frac{(Rl)^2 Y_n}{4}) \tag{12}$$

Solving (8) using numerical integration techniques like Backward Euler's equation, (8) can be expressed as a delay algebraic equation.

$$V_f(t) = \frac{1}{(\alpha_0 + \frac{\beta_0}{h})}(2V_{in}(t-\tau_n) + \frac{\beta_0}{h} V_f(t-h) - (\alpha_1 + \frac{\beta_1}{h}) V_f(t-2\tau_n) + \frac{\beta_1}{h} V_f(t-2\tau_n - h)) \tag{13}$$

where h is the step size. For the general case when the order of (4) is set to n=N, the time domain expression of (5) is obtained in similar manner and is expressed as

$$V_f(t) = \alpha_0 V_{in}(t-\tau_v) - \sum_{k=1}^{N} \alpha_k V_f(t-\tau^k) - \sum_{k=1}^{N+1} \beta_k V_f(t-\tau^{k-1}-h) \quad (14)$$

where $\tau_v = l\sqrt{LC}$, $\tau^k = 2k\tau_n$ and the values α_k and β_k are constant coefficients derived by substituting (4) in (5) and using Backward Euler's rule to convert to algebraic form.

Although (14) is the solutions of the delay differential equation obtained by numerical integration techniques similar to that used in SPICE, the number of equation to be solved to obtain the far end transient response is only one. In contrast the number of equations to be solved by [20] would depend on the discretization involved in formulation of the MNA matrix. For the single line example shown in Fig. 1 the number of MNA equations due to *n* sections will be *n**6+1 (6 equations are required for the lossless line [20] and 1 equation for the resistance). Thus, the proposed model provides a more efficient method to obtain the transient response for the case when the near and far ends of transmission lines are terminated with resistances and capacitances, respectively.

IV. Numerical Examples

A coupled RLC interconnect example is presented in this section to demonstrate the validity and efficiency of the proposed method. The results were obtained using MATLAB R2008a operating on DELL T7400 64-bit workstations with clock speed 3.16 GHz and are also compared with SPICE analysis. Within the context of this section SPICE analysis refers to using the conventional lumped model .

A single RLC line shown in Fig. 1 is considered. The interconnect structure is analyzed for a height of h = 1.2 μm and the conductor width is varied for w = 2 μm, w = 5 μm and w = 10 μm. The corresponding per-unit-length parameters are presented in Table I. The length of the line is set to 1 cm. The input signal is a ramp with a rise time of 0.1 ns. For this example the order of (5) is selected to be n=6 for all interconnect widths. The 50% delay and overshoot calculated with the proposed model are compared with SPICE analysis for various resistive and capacitive line termination values of R_s and C_l and the results are shown in Table II. In addition, the results of the 1st order Bessel function model [17] and the DEPACT macromodel [20] are also listed. Fig. 2 shows sampled far end responses corresponding to the highest 50% delay error (Fig. 2a) and the lowest 50% delay error (Fig 2b). Table III lists the CPU expense to solve (14) and compares the results with SPICE analysis of different sized lumped models, DEPACT macromodel and the modified Bessel function model. For this example, the proposed model provides a speed-up of 6 times compared to the Bessel functional model, a speed up of 100 times compared to the DEPACT macromodel and of more than 300 times to the SPICE conventional lumped model.

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