Binary Optical Switch and Programmable Optical Logic Gate Based on the Integration of GaAs/AlGaAs Surface-Emitting Lasers and Heterojunction Phototransistors

Bo Lu, Ping Zhou, Yin-Chen Lu, Julian Cheng, *Senior Member, IEEE*, R. E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, *Member, IEEE*, S. A. Chalmers and G. A. Vawter, *Member, IEEE*

***Abstract*— Optical switches based on GaAs/AlGaAs vertical-cavity surface-emitting lasers and heterojunction phototransistors are combined monolithically into new switching configurations that perform optical logic and spatial routing in a dynamically programmable manner. Using simple voltage control, many different logic and routing configurations, including AND and OR gates with variable fan-out, can be implemented using the same hardware.**

I. Introduction

WE DESCRIBE the first experimental demonstration of a novel optical switch that can be dynamically reconfigured to perform both optical logic and the spatial routing functions, thus providing the basis for functionally flexible, programmable optical logic architectures. The technology is based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) and heterojunction phototransistors (HPTs) or photothyristors (PNPNs) to form a new class of two-dimensional binary optical switch nodes which, in addition to logic and routing, also possess reconfigurability and a fan-out capability. Efficient VCSEL-based optical switches have been described previously, [1], [2] and single-stage optical logic gates based on latching PNPN/VCSEL switches [1] and non-latching HPT/VCSEL switches [1]–[3] have demonstrated the basic Boolean functions—AND, OR, INVERT, NAND, NOR, and XOR. More complex Boolean functions can be derived by optically cascading sequential logic gate arrays, which requires critical optical packaging. This can be minimized by reconfiguring a programmable logic gate array after each processing cycle in conjunction with an optical buffer memory, [1] so that a single logic array can be used repeatably to simplify both the optical and optoelectronic hardware. To apply this minimalist approach to arbitrary optical logic functions requires a greater level of integration and programming of the spatial routing [4] and logic functions. We will show below that our new optoelectronic switching technology can combine the functions of routing, logic, and fan-out in a single, *dynamically programmable* switching fabric.

The designs of the 1×2 and 2×2 binary optical switch, plus their principal modes of logic and routing operations, are shown in Fig. 1. The optical input port contains two nearly contiguous but electrically-isolated HPT segments, each controlled by a separate bias voltage (V_1 or V_2) and each serially connected to a different VCSEL output port. Optical input data impinge upon both segments in equal proportions, and depending on the state of (V_1, V_2), which can be either ON or OFF, the photoinduced and amplified current from the HPT is routed alternatively to VCSEL #1 (1, 0), to VCSEL #2 (0, 1), or to both VCSELs (1, 1), where the data is regenerated as an amplified optical output. Thus alternate routing as well as an optical fan-out of 2 can be achieved.

The 2×2 switch consists of two 1×2 switches that concatenate two nodes each containing a segmented HPT and a VCSEL. Every HPT is connected to two VCSELs (at least one of which is associated with another node), and the VCSEL at each node is similarly connected to two HPTs at different sites. The in-plane interconnection of nodes functionally defines a logic or a spatial routing function. Two nodes may share only one (*e.g.*, Omega network) or both (*e.g.*, Banyan network) input and output ports, depending on the routing network topology. Routing is controlled by the states of the voltages (V_1, V_2) and (V_2', V_1'), which provide a larger number of routing configurations, including the important bypass (1, 0, 0, 1) and exchange (0, 1, 1, 0) operations [4]. A reconfigurable multi-stage switching network can be realized by optically cascading arrays of suitably interconnected 2×2 switches, [4] which define a specific routing topology with surface-normal optical inputs and outputs.

The VCSEL at each node is connected to two HPTs from different nodes and thus *sums* the amplified photocurrents generated by optical inputs A and B . Since the VCSEL is a thresholding device, these sums can determine the logic outcome A-OR-B $(A+B)$ or A-AND-B $(A \cdot B)$, depending on whether the two optical inputs can individually or collectively produce a sufficient current to switch on the VCSEL. By controlling the prebias or the threshold of each switch, either

Manuscript received November 10, 1993; revised December 23, 1993.

B. Lu, P. Zhou, Y.-C. Lu and J. Cheng are with the University of New Mexico, Center for High Technology Materials, Albuquerque, NM 87131.

R. E. Leibenguth, A. C. Adams, and J. L. Zilko are with AT&T Bell Laboratories Breinigsville, PA 18031.

K. L. Lear, J. C. Zolper, S. A. Chalmers and G. A. Vawter are with the Sandia National Laboratory, Albuquerque, NM 87185.

IEEE Log Number 9216576.

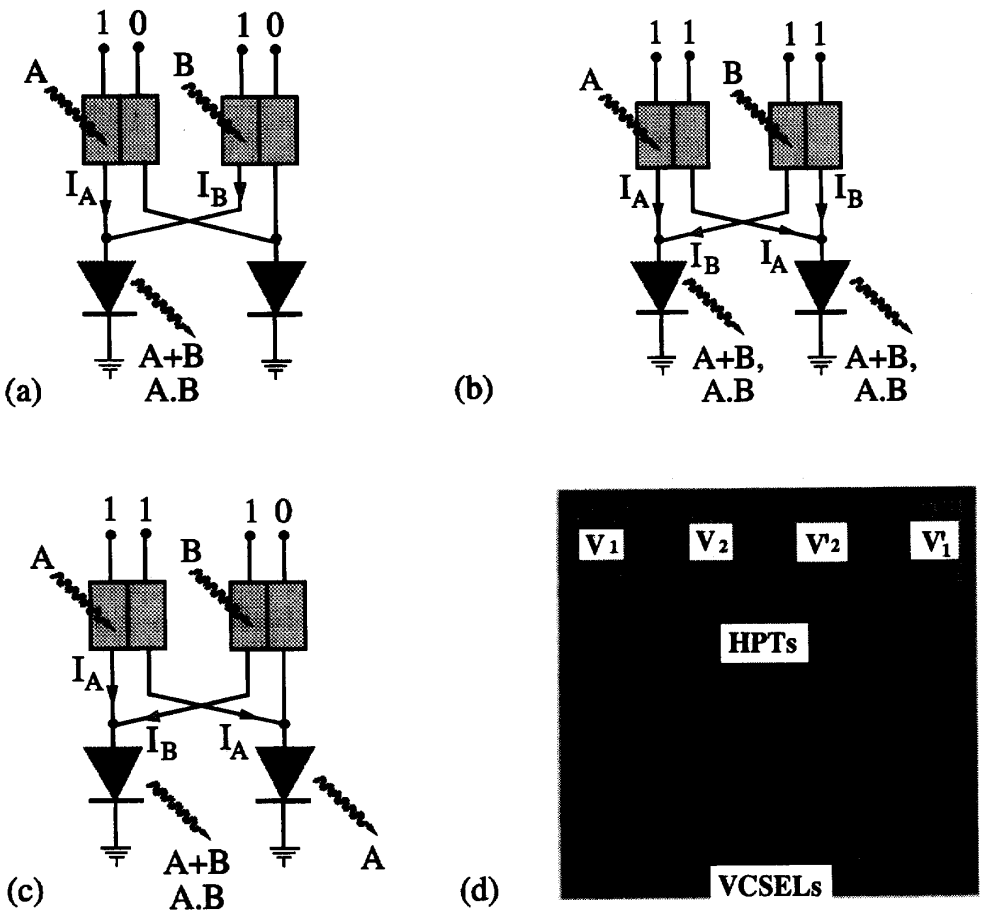

Fig. 1. The design and operating principles of a 2 × 2 binary optical switch, showing the logic configurations (a) (1, 0, 1, 0), (b) (1, 1, 1, 1), and (c) (1, 1, 1, 0) with variable fan-out. The monolithic layout of the switch is shown in (d). Depending on the optical input signal and bias levels, either A-OR-B logic or A-AND-B logic can be implemented.

AND or OR logic operation can be realized, and the optically amplified logic output can emerge from either or both VCSELs. The control voltages (V_1, V_2, V_2', V_1') completely specify the logic and routing functions of the switch. When either $V_1 = V_1'$ or $V_2 = V_2'$ is activated (Fig. 1a), the optical logic output emerges from port A (1, 0, 1, 0) or port B (0, 1, 0, 1), respectively, with a fan-out of 1. When both nodes are in the ON-state (1, 1, 1, 1), the logic output emerges from both ports with a fan-out of 2 (Fig. 1(b)). In the (1, 1, 1, 0) or the (0, 1, 1, 1) configuration (Fig. 1(c)), the logic output emerges from one of the output ports, while A or B is routed to the other. The 2 × 2 switch thus performs the binary optical logic functions $(A \cdot B)$ and $(A + B)$, and routes the output to either or both output ports, with all the controls provided by a set of control voltages.

The binary switch, whose detailed structure and fabrication are described elsewhere [5], consists of an *n-p-n* GaAs/AlGaAs HPT structure (emitter-up configuration) that is epitaxially regrown on a top-surface-emitting GaAs/AlGaAs VCSEL structure (lasing wavelength ≅ 850 nm) by molecular beam epitaxy (MBE), and the two are electrically isolated by an undoped GaAs layer. The monolithic 2 × 2 switch layout (Fig. 1(d)) shows two segmented HPT input ports and two VCSEL output ports, with counter-propagating optical inputs and outputs occurring at the same (epitaxial) surface. The active area (20 μm diameter) of each VCSEL is defined by a single 335 keV proton implant, and all the VCSELs and HPTs are electrically isolated by a multiple-energy, multiple-dose proton implant. The HPT segments at each node are isolated by a narrow etched trench. The threshold of the VCSELs is 4–6 mA, their slope efficiency η_s is between 30–60%, and the optical current gain β of the HPTs ranges from 70 to 100.

To demonstrate the logic operation of the HPT/VCSEL switch, input optical data containing a dc and a pulsed component is incident on both HPT segments. The dc intensity is adjusted so that the amplified photocurrent prebiases the VCSEL below threshold, while the pulsed optical logic inputs then singly or collectively bring the VCSEL above threshold to produce a logic output. Taking into account various systemic losses (≅ 75%), a total input intensity of ≅ 500 μW, including

100–200 μW for the data pulses, is needed to bring the VCSEL above threshold to a region of high slope efficiency.

The 2 × 1 mode of operation (logic with a fan-out of 1) is selected by setting the (pulsed) control voltages of the 2 × 2 switch for the (1, 0, 1, 0) configuration (Fig. 1(a)). The amplitude of these voltages (5.5 V), chosen to bias the VCSEL above threshold (2.3 V) and to bias the HPTs in the gain region (2 V), is also partly distributed across the series resistance of the VCSEL ($\cong$ 100 Ω). The inputs A and B are synchronous optical pulse patterns (850 nm, 10 MHz, 30–50 ns pulse width) that are incident on the HPTs in channels 1 and 2, respectively. In the (1, 0, 1, 0) configuration, their amplified photocurrents are routed to and summed by VCSEL #1. By adjusting the dc components of A and B to prebias the VCSEL at different levels below threshold (100 μW each for $A+B$, and 0 μW for $A \cdot B$), the pulsed logic inputs of A and B (200 μW) can then either individually or collectively drive the VCSEL above threshold to produce the amplified optical logic outputs $(A+B)$ and $(A \cdot B)$, respectively. In the experimental demonstration of $(A+B)$ logic in Fig. 2(a), VCSEL #1 is switched on whenever pulses appear in either or both inputs A and B (total power $\geq$ 550 μW). The logic output can emerge from either channel 1 or channels 2 by selecting the (1, 0, 1, 0) or (0, 1, 0, 1) configuration, respectively. When pulses are present in both A and B, the larger summed photocurrent drives the VCSEL further above threshold, thus producing a higher output power (250 μW average) than when only A or B is present. This is not a serious defect for cascaded OR-gate operation, since switching can be effected by any optical signal exceeding an optical threshold. However, it does broaden the optical output pulse, since the HPT must disccharge further before its collector current falls below the VCSEL threshold. Part of the broadening is also due to differences in the charging delays in the HPT associated with the individual photocurrents produced by A and B, which may not be exactly the same due to differences in optical coupling into the HPT. Both of these effects can be substantially reduced by improved design.

By removing the dc bias, the amplitudes of the pulses in A or B alone no longer have sufficient intensity to switch on the VCSEL $(1+0 = 0+1 = 0)$. Only when pulses are present in both A and B will sufficient photocurrent be generated to collectively bring the VCSEL above threshold $(1+1=1)$. The $(A \cdot B)$ logic operation is demonstrated in Fig. 2(b), using 200 μW pulses (50 ns wide) without a dc prebias. The total power incident on A and B is thus 400 μW, and the average output power of the VCSEL is 100 μW. The expected optical gain ($G \cong 5$) based on the values of β and η_s is not observed, due largely to gain compression in the HPT at above-threshold current densities. With improvements in η_s and β, a much higher optical gain can be achieved to facilitate the optically cascaded operation of multi-stage switching or sequential optical logic.

Logic operations $(A \cdot B)$ and $(A \cdot B)$ with a fan-out of two are experimentally demonstrated in Figs. 3(a) and 3(b), respectively, using a 2 × 2 switch operating in the (1, 1, 1, 1) configuration (Fig. 1(b)). The logic outputs, which are qualitatively similar to those of Fig. 2, now emerge from both output channels (fan-out of 2). For these experiments,

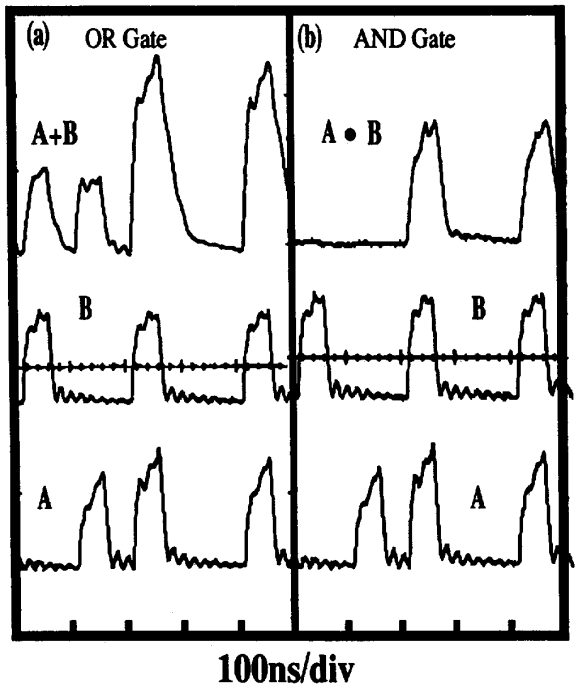

Fig. 2. Experimental demonstration of the optical logic functions (a) $A+B$, and (b)$A \cdot B$, using the a 2 × 2 optical switch operating in the (1, 0, 1, 0) configuration.

$\beta \geq 100$, and the VCSELs have a threshold of 4 mA. Another logic configuration that further demonstrates the flexibility of the 2 × 2 switch is the (1, 1, 1, 0) mode shown in Fig. 1(c) and experimentally demonstrated in Fig. 4(a), in which the logic output $(A+B)$ or $(A \cdot B)$ emerges from one output port (VCSEL #1), while A or B is routed to the other (VCSEL #2) under the control of the routing voltage pulses. Here A and B are two continuous pulse trains with different frequencies and amplitudes. Output channel 1 contains only the pulses of A, while output channel 2 contain the pulses of both A and B, which are logically summed. Note that the (1, 1, 1, 0) and (1, 0, 1, 0) configurations are logically identical, differing only in the presence of the control voltage V_2, which causes a second photocurrent I_A to be generated and routed to VCSEL #2 to produce a replica of the input A. Since the two segments of each HPT are electrically isolated, neither V_2 nor the photocurrent that it produced can affect the operation of the remaining logic function, which is otherwise identical to that of the (1, 0, 1, 0) case.

Fig. 4(b) shows the optical response of the HPT/VCSEL switch to an optical input pulse (20 ns wide) with a sub-threshold dc optical prebias. The rise time of the output pulse is $\cong$ 3 ns, but its pulse width ($\cong$ 15 ns) appears to be narrower than that of the input pulse. The switching speed is governed mainly by the fall time of the HPT, which is quite long due to its large area (40 μm × 80 μm). But since lasing ceases as soon as the collector current falls below threshold, this occurs in a time ($\cong$ 15 ns) shorter than that required to fully discharge the junctions to their sub-threshold prebias level ($\cong$ 20 ns).

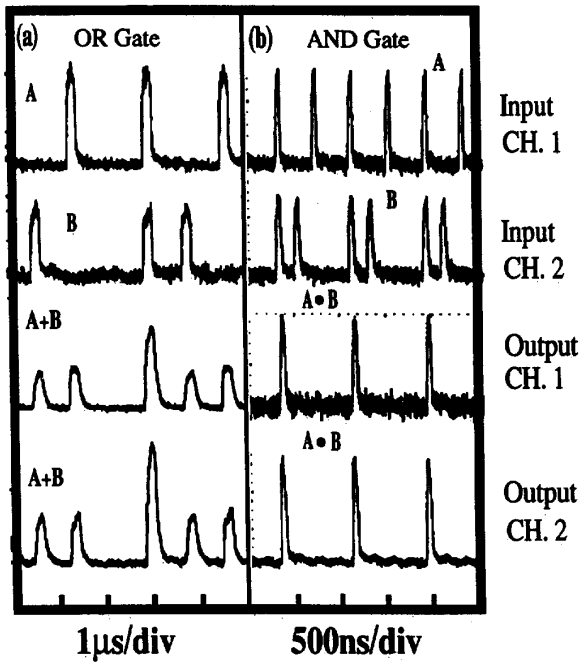

Fig. 3. Experimental demonstration of the logic function (a) $A + B$, and (b) $A \cdot B$, with an optical fan-out of two, using a 2 × 2 switch operating in the (1, 1, 1, 1) configuration.

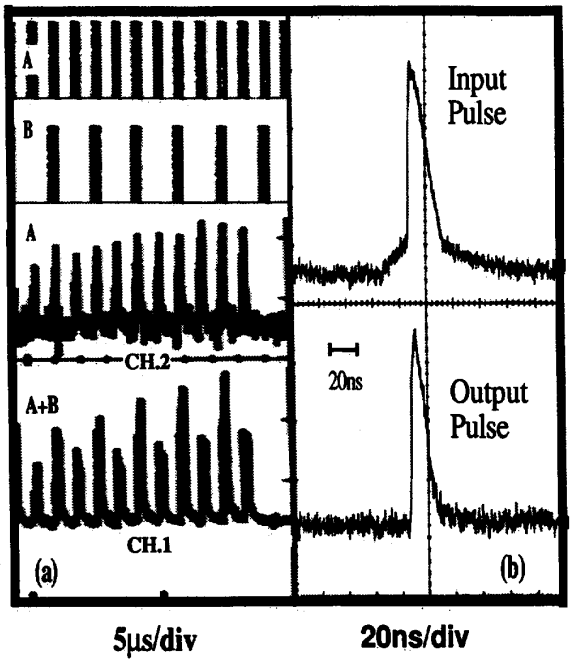

Fig. 4. (a) Experimental demonstration of the (1, 1, 1, 0) configuration, showing the routing of logic output $(A + B)$ to channel 1, and the input A to channel 2, under pulsed control voltages (which ended before the last two data pulses of A). (b) The optical response of a single element of the 2×2 switch with a sub-threshold prebias to a 20-ns wide optical pulse incident on a single HPT.

This differs from Fig. 2, in which the optical output pulse is broadened, in two ways. First, the VCSEL is driven not as far above threshold and thus the HPT needs not discharge as much, and second, there is no differential charging delay since a single optical input is used. Logic operations at 20–50 Mb/s can be achieved using the present devices, and by reducing the HPT size, improving β and η_s, a switching speed in the hundreds of Mb/s range is possible.

In conclusion, we have described the design and experimental demonstration of a reconfigurable binary optical switch that can perform optical routing and logic functions in many different spatial configurations. By combining logic and routing in a single programmable switching fabric, we have a potential technology for a programmable optical logic gate array.

ACKNOWLEDGMENT

The work at UNM was supported by AFOSR (Bolling AFB), ARPA, and Rome Labs (Griffiss AFB). The Sandia effort was supported by DOE Contract No. DE-AC04-94AL85000. We gratefully acknowledge the technical assistance of J. Escobedo of Sandia Labs.

REFERENCES

[1] J. Cheng and P. Zhou, "Integrable surface-emitting laser-based optical switches and logic gates for parallel digital optical computing," *Appl. Opt.*, Special Issue on Optical Computing, vol. 31, no. 26, pp. 5592–5603, 1992.

[2] W. K. Chan, [30] W. K. Chan, J. P. Harbison, A. C. von Lehmen, L. T. Florez, C. K. Nguyen and S. A. Schwarz, "Optically-controlled surface-emitting lasers," *Appl. Phys. Lett.* vol. 58, pp. 2342–44, May 1991.

[3] Y. H. Lee, et. al., "Active optical NOR logic devices using surface-emitting lasers," *IEEE Photon. Technol. Lett.*, vol. 4, pp. 479–482, 1992.

[4] J. Cheng, P. Zhou, S. Z. Sun and D. R. Myers, "Surface-emitting laser-based smart pixels for two-dimensional optical logic and reconfigurable optical interconnections," *IEEE J. of Quantum Electron.*, vol. 29, no. 2, pp. 741–756, Special issue on Smart Pixels.

[5] P. Zhou and J. Cheng, et. al., "Monolithic optotelectronic switch based on the integration of a GaAs/AlGaAs heterojunction bipolar transistor and a GaAs vertical-cavity surface-emitting laser," *IEEE Photon. Technol. Lett.*, vol. 5, pp. 1035–1038, 1993.