

Reconfigurable Binary Optical Routing Switches with Fan-Out Based on the Integration of GaAs/AlGaAs Surface-Emitting Lasers and Heterojunction Phototransistors

Bo Lu, Ping Zhou, Yin-Chen Lu, Julian Cheng, *Senior Member, IEEE*, R. E. Leibenguth, A. C. Adams, J. L. Zilko, J. C. Zolper, *Member, IEEE*, K. L. Lear, *Member, IEEE*, S. A. Chalmers and G. A. Vawter

Abstract—The design, fabrication, and experimental demonstration of dynamically reconfigurable binary optical switches based on the integration of GaAs/AlGaAs vertical-cavity surface-emitting lasers and heterojunction phototransistors are reported. These new monolithic optical switches can perform spatial routing and optical amplification functions on input optical data with a fan-out of two, and can be programmed using simple voltage control. The 1×2 and 2×2 devices provide the basis for a high performance, two-dimensional optical switching fabric with electrical interfaces for optical switching and interconnection networks.

I. INTRODUCTION

MONOLITHIC arrays of optical switches based on the integration of GaAs/AlGaAs vertical-cavity surface-emitting lasers (VCSELs) and heterojunction phototransistors (HPT) represent a promising two-dimensional approach to high-throughput optical data processing [1] and optical switching networks. [2] VCSEL-based optical switches with alternatively non-latching or latching switching characteristics have been demonstrated by integrating VCSELs with HPTs or phototransistors (PNPNs), respectively. Both of these switches can perform digital optical logic processing functions. [1] They can also be further combined monolithically into more complex binary switch nodes that can spatially reconfigure the surface-normal optical signal paths. [3] These binary optical switches can perform a variety of spatial switching functions, including bypass and exchange, which provide the basis for a compact, multi-stage optical switching network. In addition to forming a switching fabric capable of spatially routing high speed optical data amongst a large number of parallel optical channels, each switch also provides a high speed optical-to-electrical interface between the optical switching network and its electronic control functions. [4] To be a practical switching technology, these switching nodes must be dynamically reconfigurable, [5–7] and must be able to

accommodate a variety of different network topologies (*e.g.*, Omega or Banyan), and some degree of optical fan-out must be provided for multi-cast and broadcast operations. Although our earlier binary 2×2 optical switch design [2] is capable of performing optical bypass-exchange operations, it lacks a fan-out capability, and was experimentally demonstrated using principally PNP/VCSEL switches. In this paper, we report a new and improved device design for the monolithic, 1×2 and 2×2 , HPT/VCSEL binary optical switches, and demonstrate their operation as dynamically reconfigurable optical signal routing switches with a variable fan-out capability. We will show that packets of optical data can be routed rapidly to one or more destinations by means of simple voltage control.

The circuit design and the operation principles of the binary optical switches are shown in Fig. 1. The 1×2 switch (Fig. 1(a)) contains a segmented HPT optical input port, each half of which is controlled by a separate bias voltage (V_1 or V_2) and is serially connected to a different VCSEL output port. The optical input data impinges on both HPT segments in equal proportions, and depending on the state (V_1, V_2) of the control voltages, the photoinduced and amplified current from the HPT is routed alternatively to VCSEL #1 (1,0), to VCSEL #2 (0,1), or to both VCSELs (1,1), where the data is regenerated as an amplified optical output (Fig. 1(c)). Thus alternate routing as well as an optical fan-out of 2 can be achieved. A 2×2 switch can be realized by combining two 1×2 switch nodes, which may (as in Fig. 1(b)) share the same two input and output ports. In this case, routing is controlled by the state of the voltages (V_1, V_2, V_2', V_1'), which provide a larger number of routing configurations, including the important bypass (1,0,0,1) and exchange (0,1,1,0) operations (Fig. 1(c)). Although it is less readily apparent, each 1×2 switch can also be interconnected with other 1×2 switches with which it shares only one common input (segmented HPT) or output port (VCSEL), but not both, to form a different 2×2 switch configuration (2 inputs, 2 outputs) that can be used to implement an Omega network topology. Every HPT is connected to two VCSELs (at least one of which is non-local), and the VCSEL at each node is similarly connected to two HPTs at different sites. It is the different pairing of switch nodes, or sites, that functionally defines a specific routing network topology.

Manuscript received October 29, 1993.

B. Lu, P. Zhou, Y.-C. Lu and J. Cheng are with the University of New Mexico, Center for High Technology Materials, Albuquerque, NM 87131.

R. E. Leibenguth, A. C. Adams and J. L. Zilko are with AT&T Bell Laboratories, Breinigsville, PA 18031.

J. C. Zolper, K. L. Lear, S. A. Chalmers and G. A. Vawter are with Sandia National Laboratory, Albuquerque, NM 87185.

IEEE Log Number 9215892

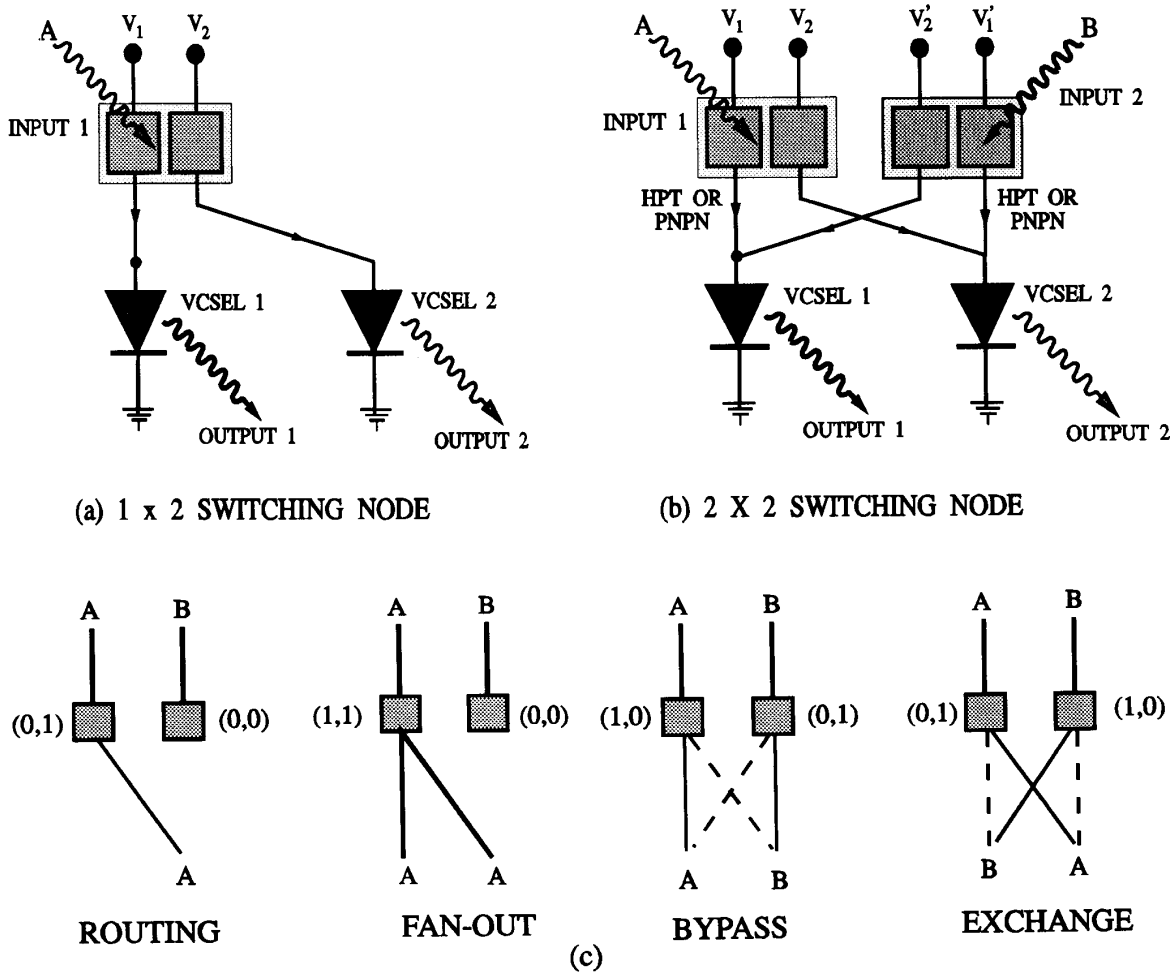


Fig. 1. Circuit design of the monolithic (a) 1×2 and (b) 2×2 binary optical switches, and (c) some of their reconfigurable modes of switching operation.

A cross-sectional view of the new epilayer structure for a 2×2 binary HPT/VCSEL optical switch and its device design are shown in Fig. 2(a), while a photomicrograph of the monolithic switch is shown in Fig. 2(b). The VCSEL and HPT epilayers are vertically stacked together and are electrically isolated by a thick, low-doped GaAs layer, and an emitter-up configuration is chosen for the HPT. The detailed epilayer structure is described in Ref. 4, and is grown by molecular beam epitaxy (MBE) on an n -GaAs substrate. The 2×2 switch contains two segmented HPTs and two VCSELs. Each GaAs/AlGaAs VCSEL has a nominal active area diameter of $20 \mu\text{m}$, which is defined by proton-implantation (335 keV , $4 \times 10^{14}/\text{cm}^2$ dose). Each HPT input port contains two nearly contiguous but electrically-isolated $40 \mu\text{m}$ by $80 \mu\text{m}$ segments. The VCSELs and HPTs are individually isolated by a multiple-energy, multiple-dose proton-implant. The device fabrication started with the etching of two mesas using a (1:1:40) $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution to define the areas of the emitter segments and of the collector ($70 \mu\text{m}$ by $115 \mu\text{m}$), stopping at the AlAs stop-etch layer. The latter is then

removed, followed by metallization of the n -type emitter and collector contacts. Next, separate proton implants are used to define the current confinement in the VCSEL and to isolate the individual VCSELs and HPTs. The upper (p -type) and lower (n -type) contacts of the VCSEL are then deposited, and the VCSEL implant and the contacts are simultaneously annealed. A photosensitive polyimide layer is then deposited to provide electrical isolation for the metal interconnection layer, which connects the HPT emitter to the VCSEL p -contact. Finally holes are opened to provide access to the various contacts. The threshold current of the VCSELs is between 4 to 6 mA, the differential slope efficiency is $\eta_S \cong 30\% - 60\%$, and their series resistance is typically $\cong 100\Omega$ (due to a non-optimum p -contact). The small signal current gain β of the HPTs varies from 60 to 100 across the range of operating current densities. The external quantum efficiency η_e of each HPT segment is estimated to be $\cong 25\%$, taking into account the input partition (each segment of an HPT receives less than half the incident light), the Fresnel reflection loss at the top surface ($\cong 30\%$), the absorption in the GaAs cap layer of the

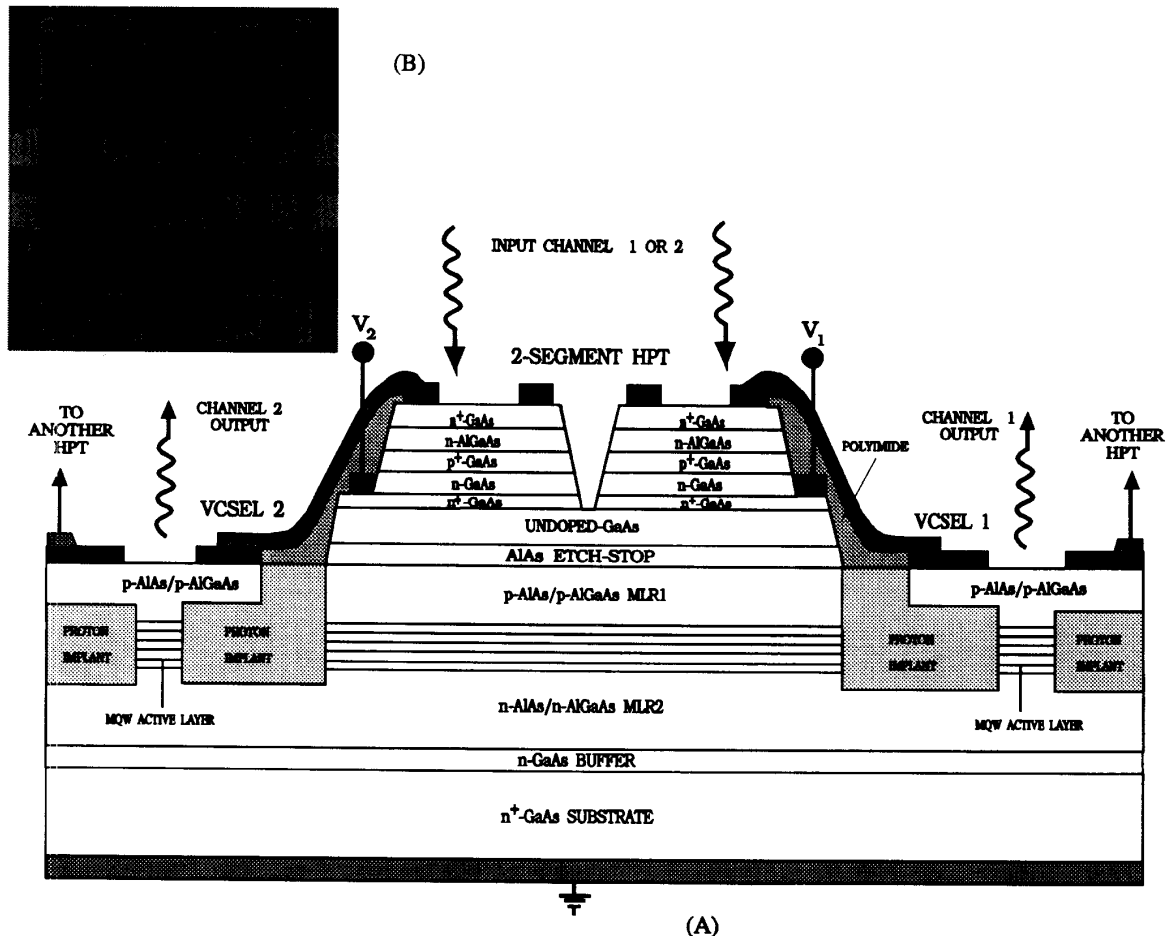


Fig. 2. (a) The epitaxial layer structure and schematic device design of a binary optical switch containing two VCSEL optical output ports and two segmented HPT optical input ports (only one is shown). (b) Photo micrograph showing the monolithic circuit layout of an array of 2×2 switches.

HPT, and the internal quantum efficiency of the collector-base junction.

To demonstrate the operation of the HPT/VCSEL switch, the input light from an external laser source containing both a dc optical bias and a modulated ac component is incident on a segmented HPT through a butt-coupled multi-mode optical fiber. The size of the segmented HPT was chosen to capture most of the fiber's optical output. The HPT/VCSEL optical switch is a non-latching threshold switch, in which the photocurrent induced by the optical input is multiplied by the average current gain $\langle\beta\rangle$ of the HPT to switch on the VCSEL. The switching threshold is thus the input optical power ($\cong 350 \mu\text{W}$) required to bias the VCSEL at its lasing threshold (6 mA). From this, the value of $\eta_e\langle\beta\rangle$ is determined to be 25. By prebiasing the VCSEL near threshold, the optical switching energy and turn-on delay are both reduced, and the switch possesses linear optical amplification characteristics above threshold. Switching is produced by the modulated optical input data pulses ($\cong 150 \mu\text{W}$), which should produce an amplified optical output with a differential optical gain

$G = \eta_e\eta_s\beta$. With $\eta_e\langle\beta\rangle \cong 25$, and $\eta_s \cong 30\%$, an optical gain of about 8 is expected. However, the observed optical gain is much lower ($\cong 1-2$) due to gain compression in the HPT at the current densities above threshold ($> 2 \text{ kA/cm}^2$), where the overall current gain $\langle\beta\rangle$ ($\cong 100$) far exceeds the differential current gain β (≤ 20).

The modes of operation of the 1×2 switch have been demonstrated using the 2×2 switch (Fig. 1(b)) by setting V_1' and V_2' equal to 0, *i.e.*, operating in the $(V_1, V_2, 0, 0)$ state. In the upper traces of Fig. 3, the control voltages V_1 and V_2 are shown as synchronous, complementary gating pulses ($\cong 5.5 \text{ V}$), while the optical input incident on HPT #1 is a train of 850 nm optical pulses ($\cong 50 \text{ ns}$ wide, $\cong 1 \text{ MHz}$ frequency) with a dc optical prebias. Since the VCSEL threshold voltage is 2.3 V, while the saturation voltage of the HPT is only about 2 V, a significant part of the 5.5 V routing voltage is dropped across the series resistance of the VCSEL. As the control voltage toggles between V_1 and V_2 , the regenerated optical input is seen to emerge alternately from either channel 1 (VCSEL #1), *i.e.*, the (1, 0) state, or from channel 2 (VCSEL #2),

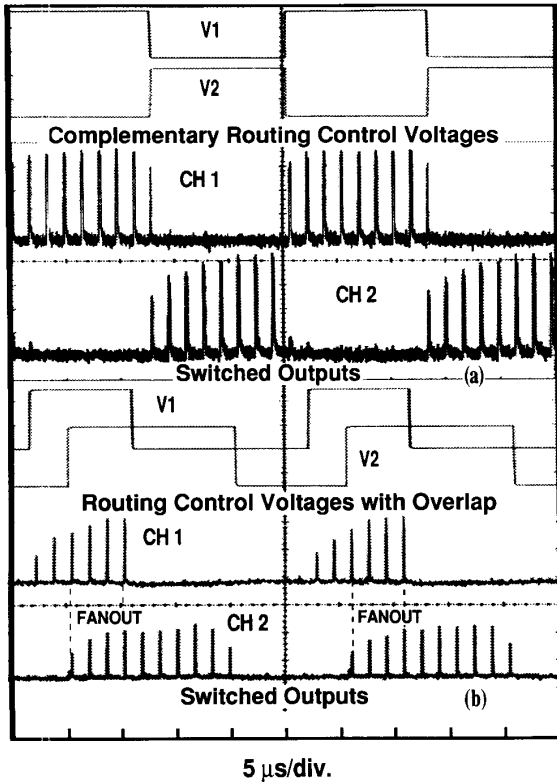


Fig. 3. The experimental demonstration of the operations of a 1×2 binary optical switch, showing the complementary routing control voltages and the optical output channels for the cases of (a) non-overlapping, and (b) overlapping control voltages, with the latter showing an optical fan-out of 2.

i.e., the (0, 1) state. In the upper output traces in Fig. 3(a), the control voltages V_1 and V_2 do not overlap in time, while for the lower output traces they partially overlap. In the latter case, the overlapping of V_1 and V_2 produces the (1, 1) state with a fan-out of 2, in which the input data emerges from both VCSEL output ports. Thus the optical input data can be routed in packet form to either or both output ports in a completely controllable and reconfigurable manner.

Fig. 4 illustrates the operation of the 2×2 optical switch in the bypass (1, 0, 0, 1) and exchange (0, 1, 1, 0) modes, in which the complementary voltage pairs $V_1 = V_1'$ and $V_2 = V_2'$ are alternately set equal to 1 and 0. Here optical INPUT 1 and INPUT 2 are two optical pulse trains characterized by different frequencies (0.6 MHz and 1.2 MHz) and amplitudes, which are incident on the segmented HPT #1 and HPT #2, respectively. As the control voltages ($\cong 6.5$ V) toggle between the (1, 0, 0, 1) and the (0, 1, 1, 0) states, the output traces show that the regenerated channel #1 input data is switched alternately between the channel #1 and channel #2 output ports, while at the same time, the channel #2 input data is switched between the channel #2 and channel #1 output ports, respectively. The former thus represents the bypass (or straight-through) configuration, and the latter the exchange (or crossover) configuration. Other 2×2 routing configurations have also been experimentally demonstrated.

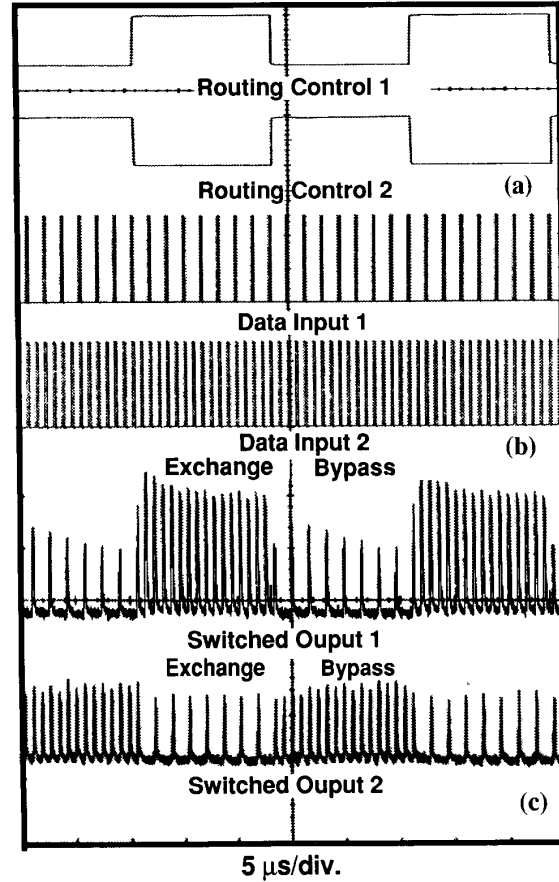


Fig. 4. Experimental demonstration of a 2×2 binary optical switch, showing (a) the control voltages, (b) the input optical channels, and (c) the output optical channels, indicating the optical bypass and exchange operations.

The optical pulse response of the switch shows a rise time of $\cong 3$ ns. However, it has a longer decay time, which is limited by the large size ($40 \mu\text{m}$ by $80 \mu\text{m}$) and large effective capacitance of the HPT, which limit the minimum optical pulse width used in this experiment to about 20 ns. Although both the HPT and the VCSEL can be optimized to respond more rapidly to an input optical signal, the current design was chosen to facilitate the ease of optical coupling rather than maximizing the switching speed. The rise time of the switched output is limited by the time needed to charge the collector current to bias the VCSEL above its lasing threshold. The time for bringing these particular HPTs from a zero bias to threshold is about 1 to 2 μs . By superimposing a dc optical or electrical threshold pre-bias on the optical data pulses, the precharge time has been greatly reduced to $\cong 3$ ns. To further reduce the decay time, the active area of the HPTs must be scaled down, and several other different approaches are under investigation.

II. CONCLUSION

In conclusion, we have described the design and fabrication of monolithic, 1×2 and 2×2 HPT/VCSEL binary optical

switches. We have experimentally demonstrated their operation, for the first time, as a flexible spatial routing switch with fan-out, which can be programmed simply and rapidly to route optical data packets amongst parallel optical data channels through a number of reconfigurable paths in the switching fabric. High performance switching has been achieved using switches that are capable of accommodating a variety of different switching network topologies, while providing multicast capabilities. The present devices are capable of routing 50 Mb/s data packets (20 ns clock period), but the next generation of switch designs under study will be able to push this into the hundreds of Mb/s regime. The switching pulse energy, currently at 100–150 μ W, can be lowered by increasing the HPT current gain β to >500 , and improving the input power efficiency from 25% to 40–50%, thereby reducing the input switching power to a few tens of μ W. Improving the slope efficiency of the VCSEL by reducing its self-heating and mode misalignment would also increase the optical output power. An optical gain of over 100 is potentially achievable with a binary optical switch.

ACKNOWLEDGMENT

The work at UNM was supported by Rome Laboratories (Griffiss AFB), the Advanced Research Projects Agency-MTO, and the Air Force Office of Scientific Research (Bolling AFB). The work performed at Sandia was supported by DOE

Contract No. DE-AC04-76DP00789. We gratefully acknowledge the technical assistance of J. Escobedo of Sandia National Laboratory.

REFERENCES

- [1] J. Cheng and P. Zhou, "Integrable surface-emitting laser-based optical switches and logic gates for parallel digital optical computing," *Applied Optics, Special Issue on Optical Computing*, vol. 31, no. 26, pp. 5592–5603, 1992.
- [2] J. Cheng, P. Zhou, S. Z. Sun and D. R. Myers, "Surface-emitting laser-based Smart Pixels for two-dimensional optical logic and reconfigurable optical interconnections," *IEEE J. of Quantum Electron.*, vol. 29, no. 2, pp. 741–756., Special issue on Smart Pixels.
- [3] J. Cheng and P. Zhou, "Smart Pixels for two-dimensional arrays," *IEEE Circuits and Devices*, vol. 9, no. 2, pp. 19–27, March, 1993.
- [4] P. Zhou, J. Cheng, J. C. Zolper, K. L. Lear, S. A. Chalmers, G. A. Vawter, R. E. Leibenguth and A. C. Adams, "Monolithic optoelectronic switch based on the integration of a GaAs/AlGaAs heterojunction bipolar transistor and a GaAs Vertical-Cavity Surface-Emitting Laser," *IEEE Photons Technol. Lett.*, vol. 5, no. 9, pp., Sept. 1993.
- [5] H. S. Hinton and A. L. Lentine, "Multiple quantum-well technology takes SEED," *IEEE Circuits and Devices*, vol. 9, no. 2, pp. 12–18, March 1993.
- [6] F. B. McCormick, F. A. P. Tooley, T. J. Cloonan, J. L. Brubaker, A. L. Lentine, et al., "Experimental investigation of a free-space optical switching network using S-SEEDs," *Applied Optics*, vol. 31, pp. 5431–5446, 1992.
- [7] K. Noguchi, T. Sakano and T. Matsumoto, "A Multichannel free-space optical switch based on multistage network configuration," *J. Lightwave Technol.* vol. 9, 1726–1732, 1991.
- [8] T. Sakano, K. Noguchi and T. Matsumoto, "Multiprocessor system using an automatically rearrangeable free-space multichannel optical switch: COSINE-2," *Appl. Optics* vol. 32, pp. 3690–3699, 1993.