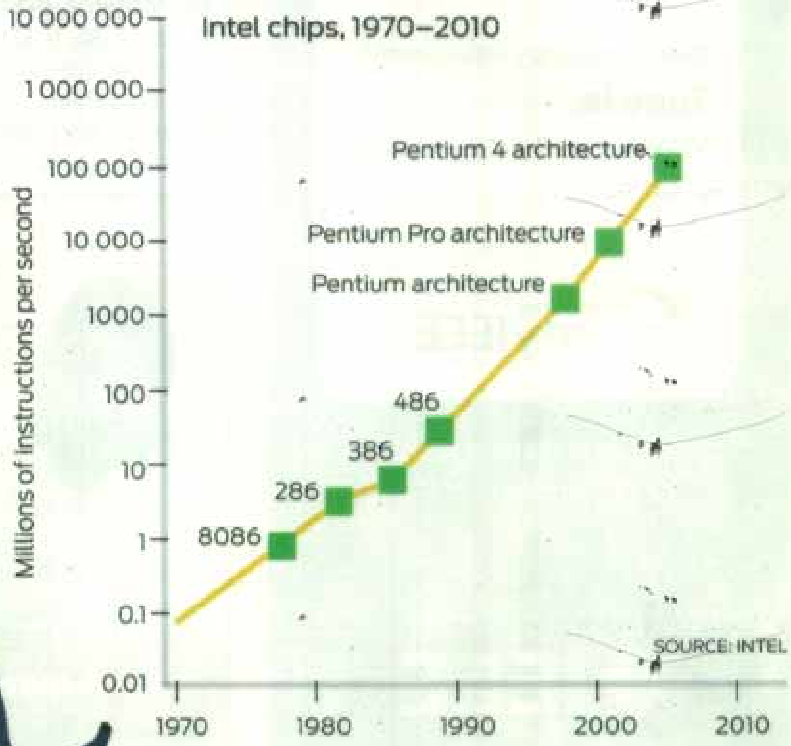
# ECE 562

Week 8 Lecture 2

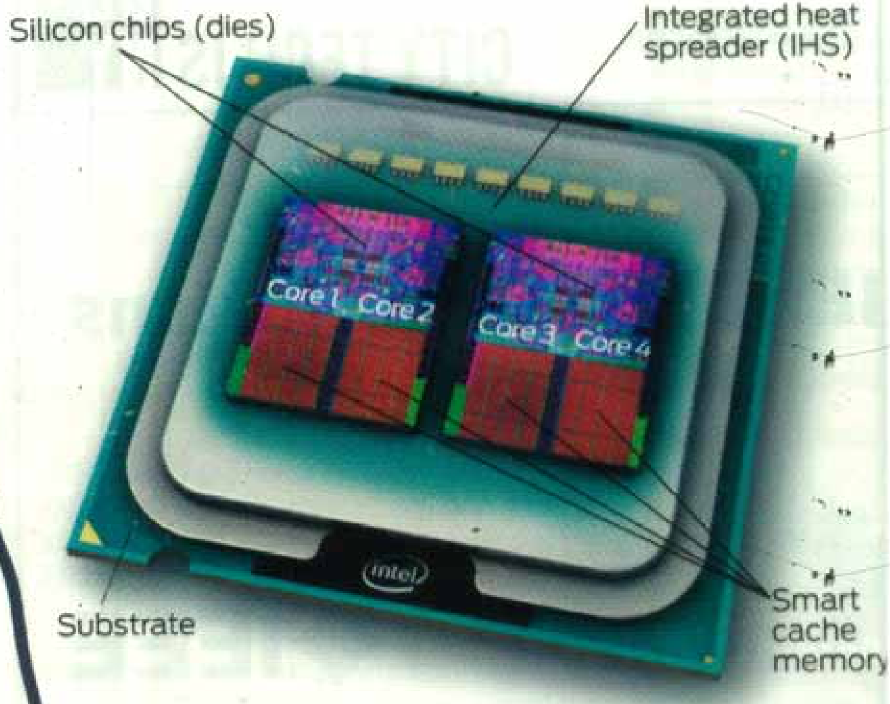
Fall 2008

# Week 8 Lecture 2
# Summary

| Slides | Topic |
|---|---|
| 3-9 | MPU performance and power conversion |
| 10-14 | Fuel cell power sources |
| 15-31 | Power regulation for LED's |
| 32-44 | DCM convertors and mode boundaries |
| 45-54 | Problem 5.4 and 5.5 |



Intel chips, 1970–2010
Millions of instructions per second
10 000 000
1 000 000
100 000
10 000
1000
100
10
1
0.1
0.01
1970
1980
1990
2000
2010
8086
286
386
486
Pentium architecture
Pentium Pro architecture
Pentium 4 architecture
SOURCE: INTEL


Silicon chips (dies)
Integrated heat spreader (IHS)
Core 1
Core 2
Core 3
Core 4
intel
Substrate
Smart cache memory

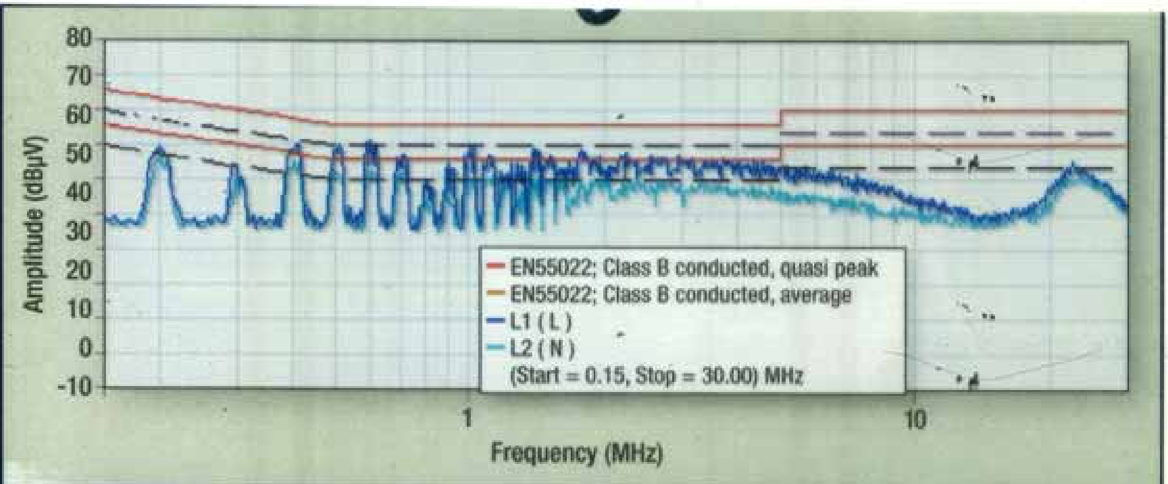



**Fig. 1.** *In a typical ac-dc power-supply design, the process of changing high-voltage dc to a chopped or a pulsed waveform produces harmonics that must be limited in amplitude to obtain EMI regulatory approvals such as EN55022.*

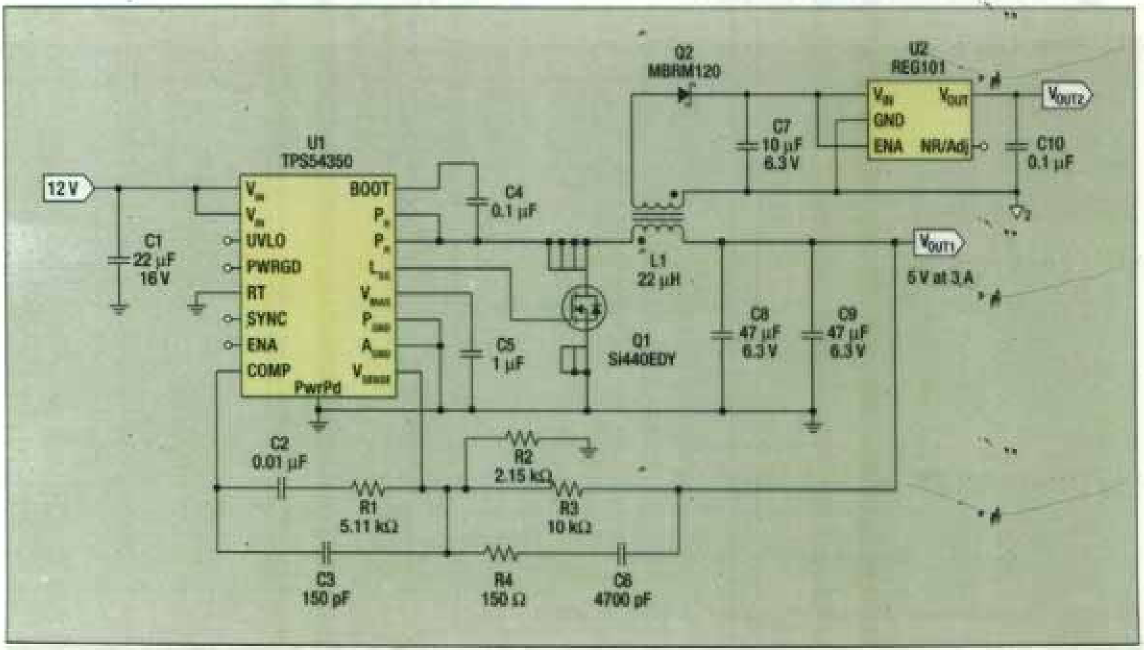



**Fig. 2.** *An isolated output voltage is achieved by using a coupled inductor in combination with a linear regulator.*

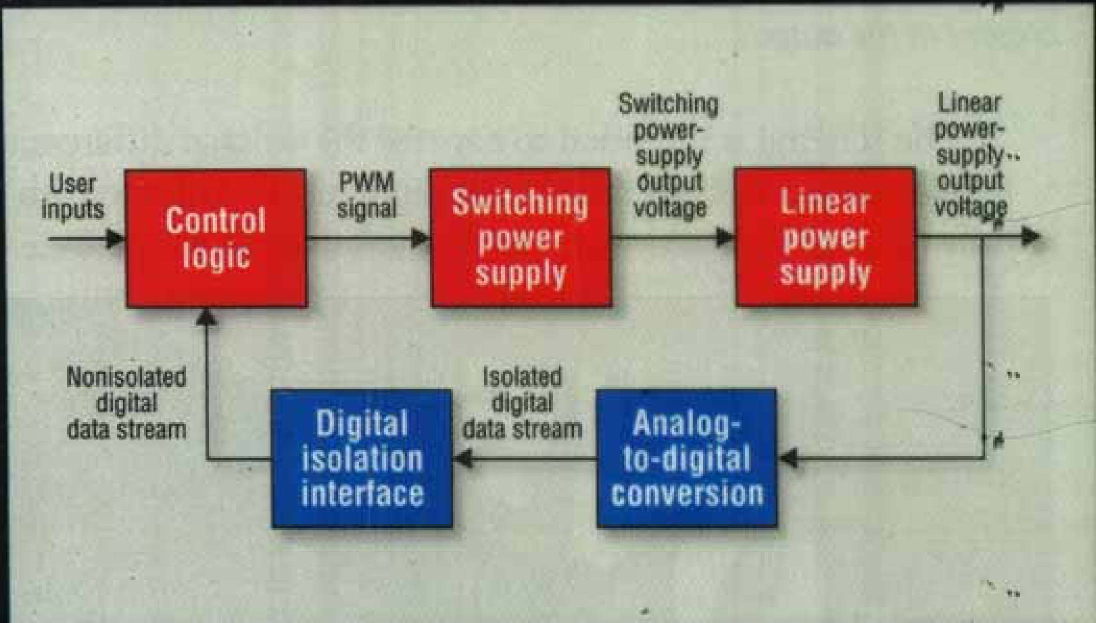
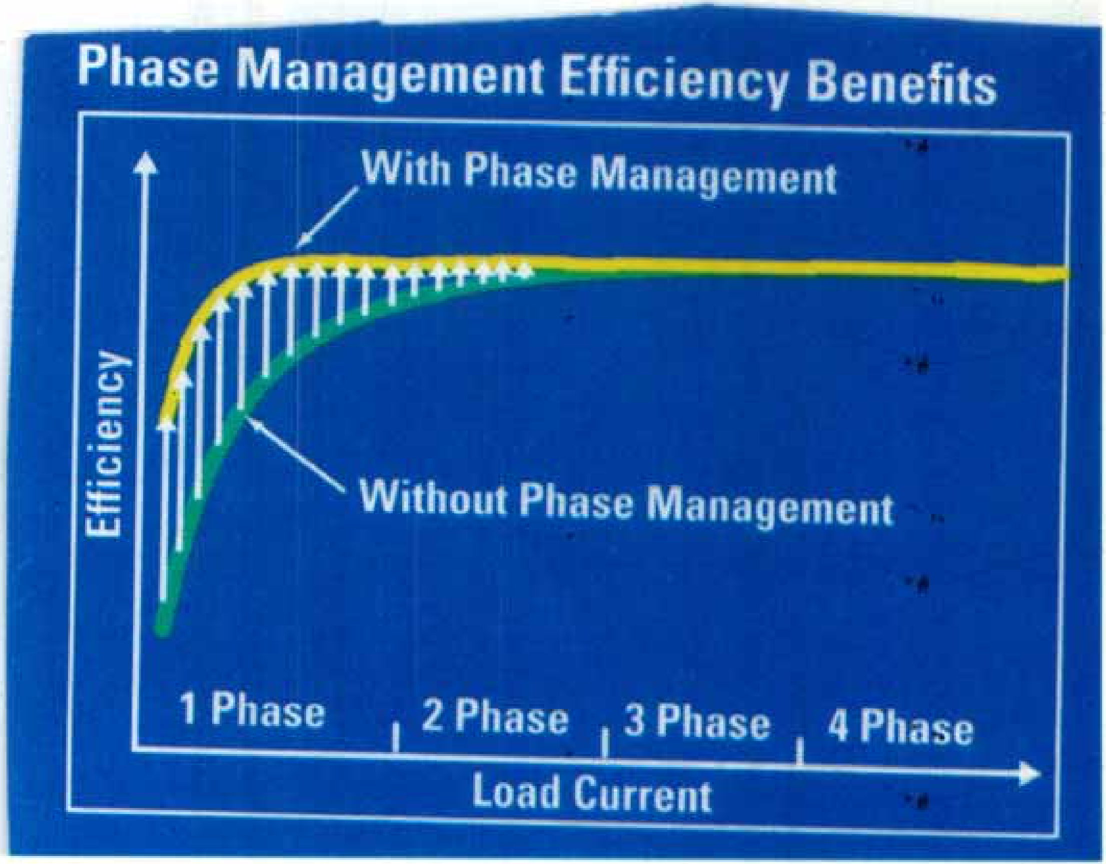
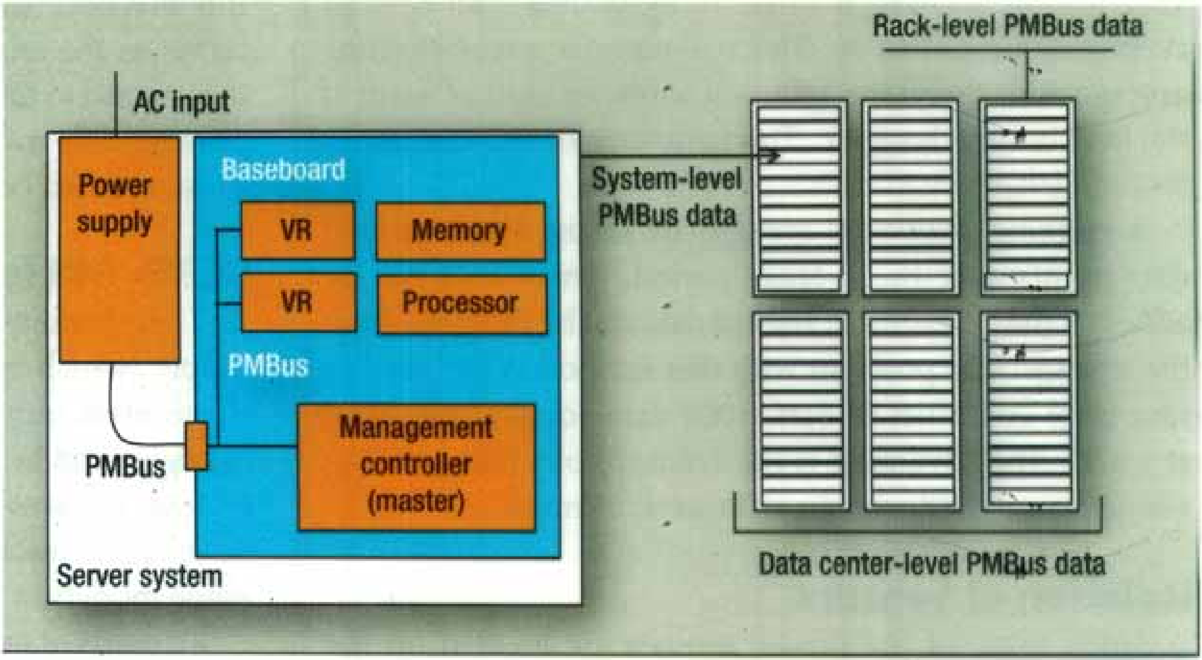
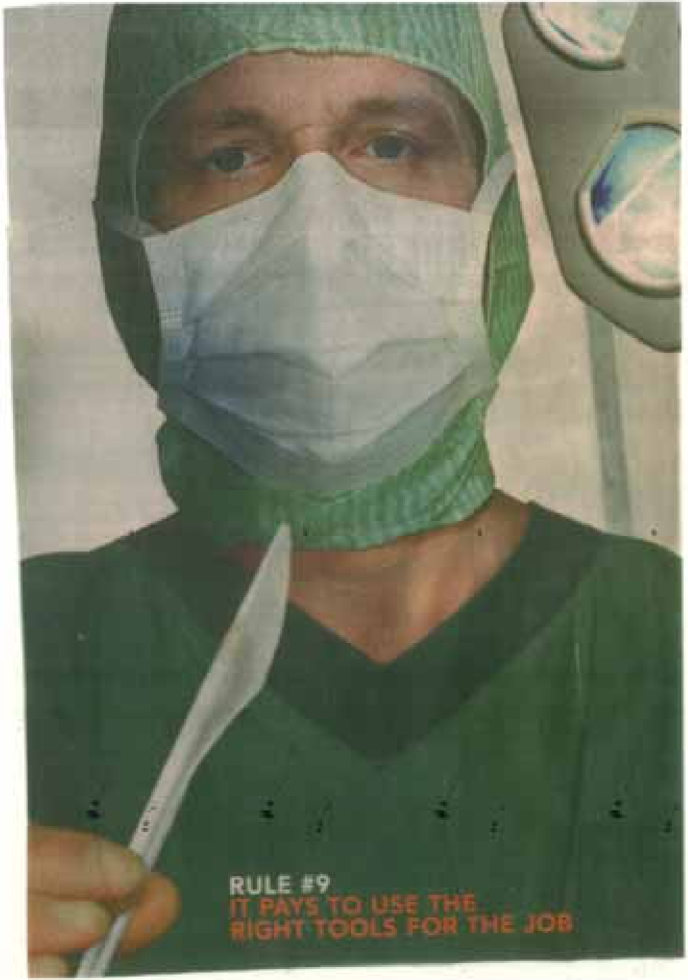



**Fig. 2.** *This diagram shows a closed-loop control scheme for the switching power supply in a multistage digital power converter.*


Phase Management Efficiency Benefits
With Phase Management
Without Phase Management
Efficiency
1 Phase
2 Phase
3 Phase
4 Phase
Load Current




*he ability of ac-dc power supplies and dc-dc converters to communicate using PMBus ommands makes it possible to monitor power consumption at the server system, rack nd data center levels.*


RULE #9
IT PAYS TO USE THE
RIGHT TOOLS FOR THE JOB

# The New Juice Box

## Methanol, butane and other gase

Associated Press

Toshiba's direct methanol fuel cell wa
certified as the smallest in the world

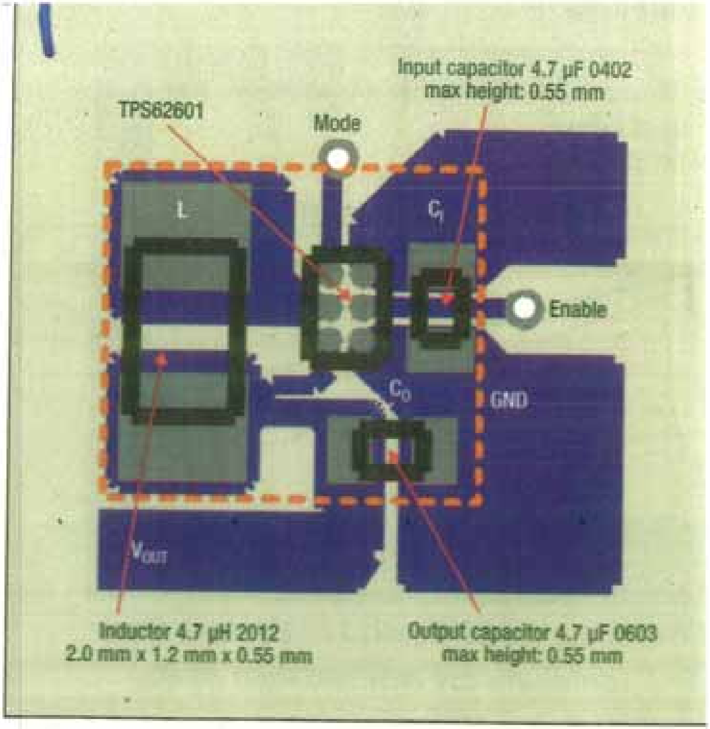
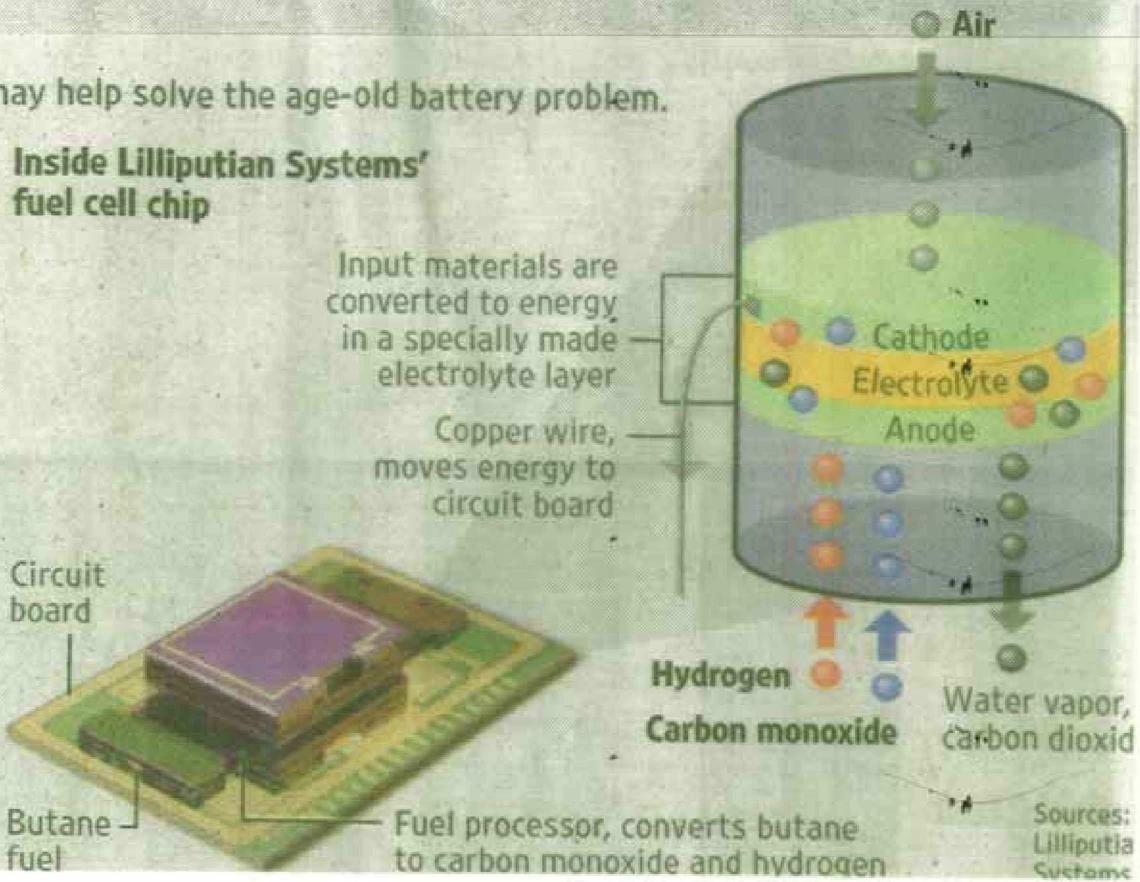



**Fig. 1.** *With its 6-MHz switching frequency and 6-pin wafer-level chip-scale packaging, the TPS62601 500-mA synchronous buck converter requires less than 13 mm² of pc-board area for a complete dc-dc converter design.*

may help solve the age-old battery problem.

**Inside Lilliputian Systems' fuel cell chip**

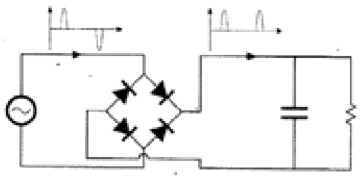


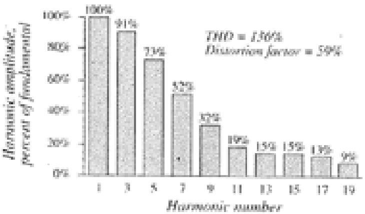

Sources: Lilliputia Systems

# Trust is never given, it is earned.

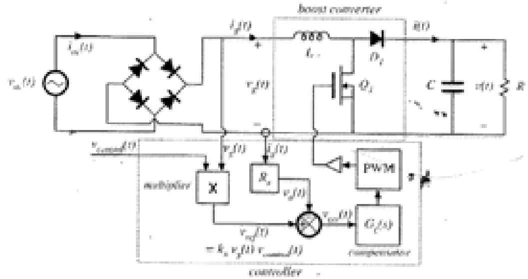
# Part IV. Modern rectifiers,
## and power system harmonics

### *Pollution of power system by rectifier current harmonics*

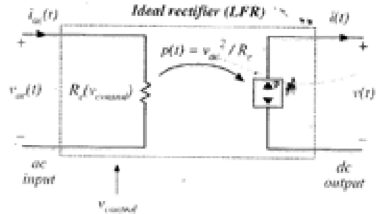





### *A low-harmonic rectifier system*




### *Model of the ideal rectifier*



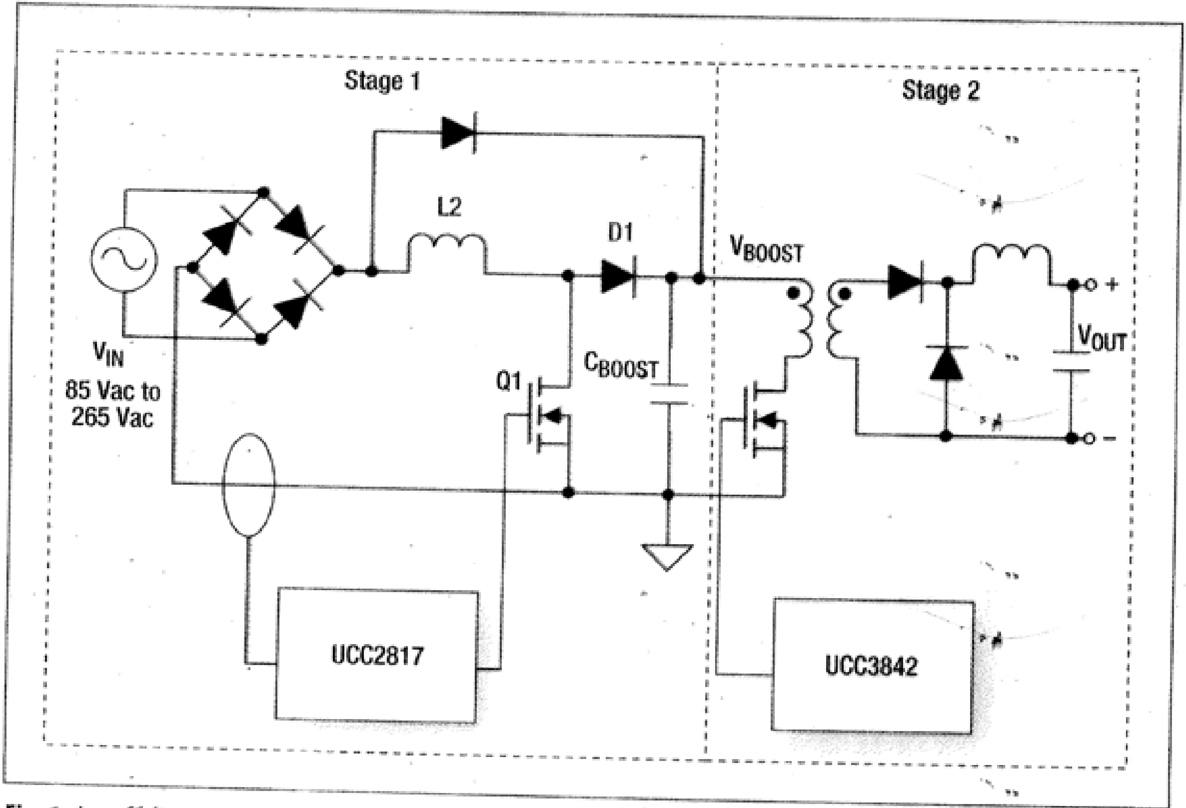



**Fig. 1.** *In off-line power supplies, a two-stage approach to power-factor correction is common. The front end, Stage 1, is a boost converter that shapes the input current and produces a high dc voltage, which is then stepped down by the converter in Stage 2.*

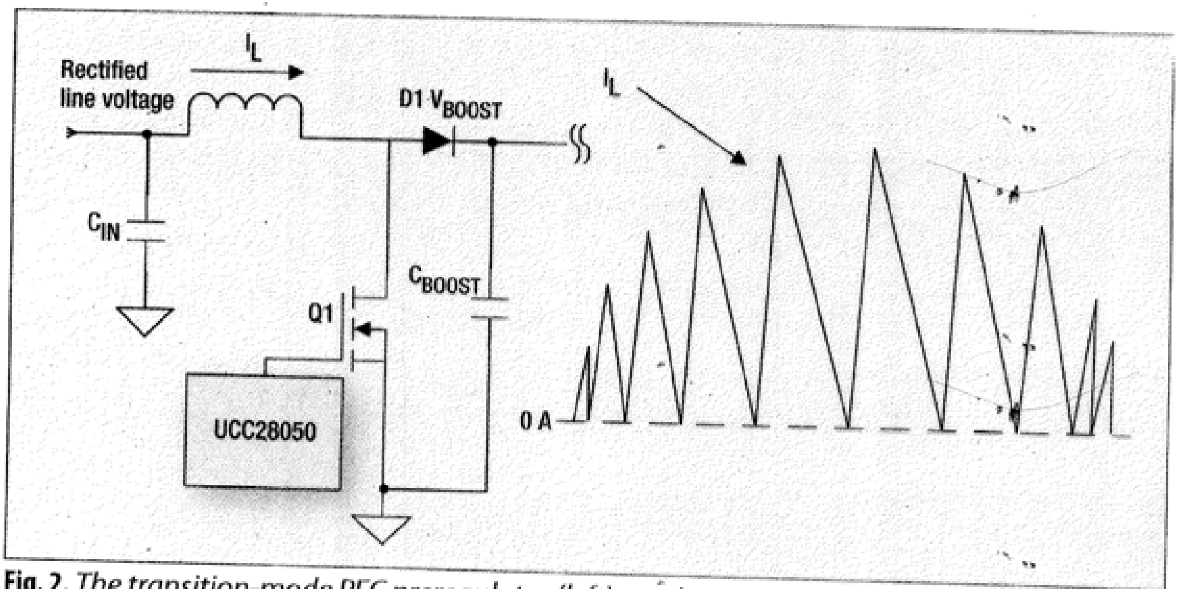


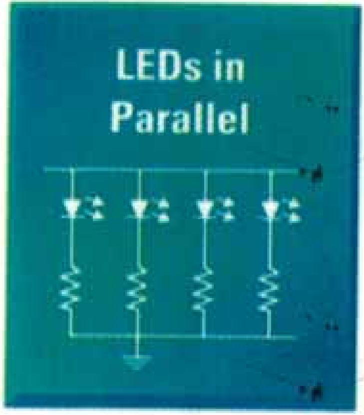

**Fig. 2.** *The transition-mode PFC preregulator (left) employs zero-current switching, whereby the controller waits for the inductor to completely de-energize before turning on the boost FET for the next switching cycle. A drawback of this circuit is that inductor ripple current (right) is twice the average input current.*

**Figure 1. The light fixture** of the future may look very different from the lamp of today. Form will follow function to reflect the many ways in which LEDs can be used. In this fixture, the white bulbs incorporate blue-emitting LEDs, each covered by a phosphor that converts the blue light to white.

## Parallel Topologies

LEDs in parallel: When LEDs are connected off one wire, next to each other in a row; positive (+) to separate grounds (GND).

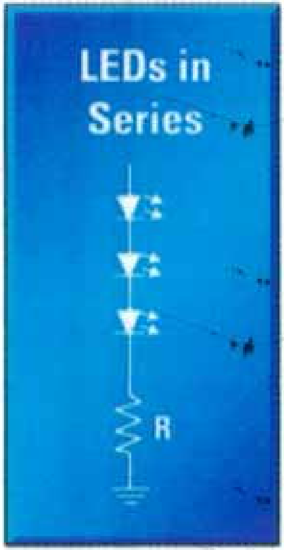
Advantage: Not restricted to one power rail; good for keypad applications.



# Series Topologies

LEDs in series: When all LEDs are connected off one wire in a column, one after another; positive (+) to negative (-).

Advantages: Single output pin, guaranteed current matching.



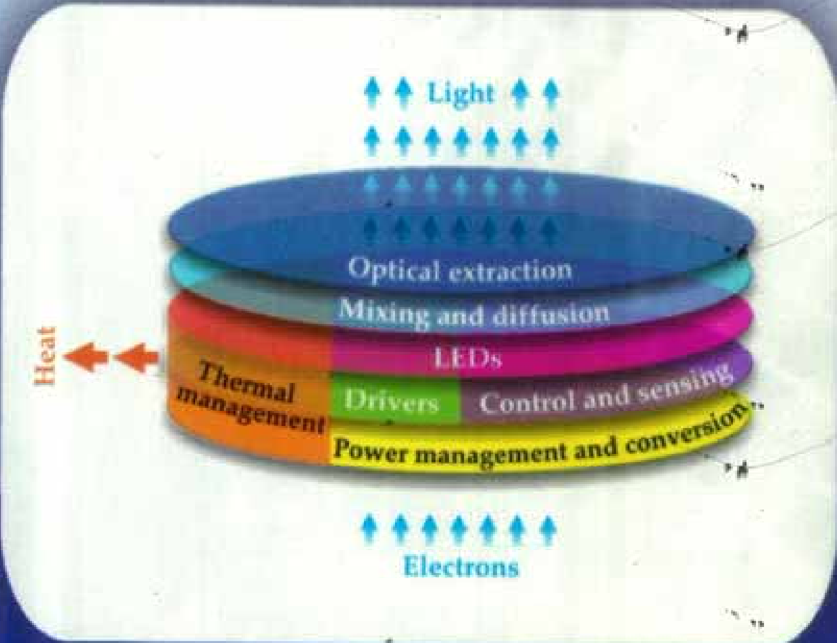



**Figure 2. An LED luminaire** includes a number of tightly integrated technologies, discussed in the text, that work together to convert electrical energy into light.

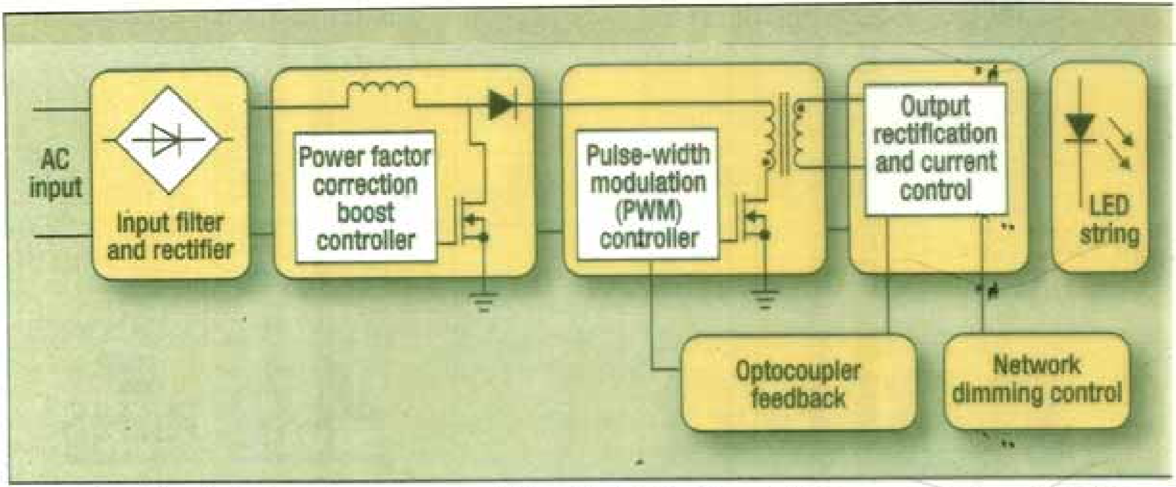
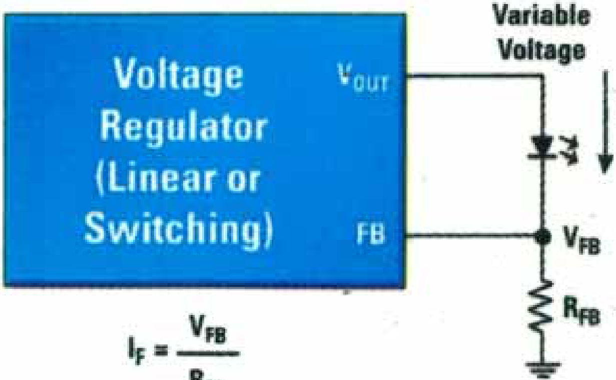


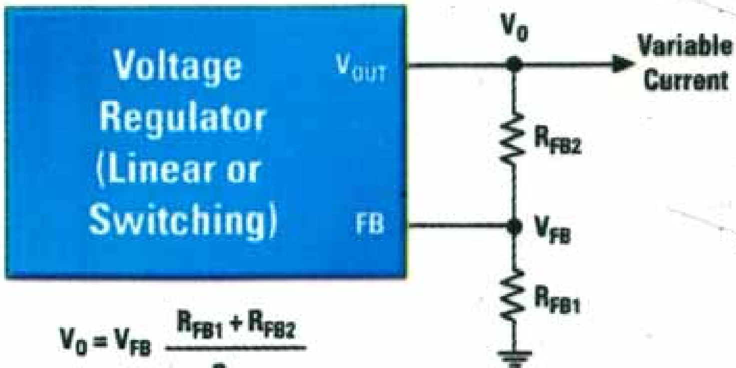

**Fig. 1.** *All of the global requirements for driving high-brightness LED lamps can be met by this two-stage design topology. This approach supports LED string lengths up to 60 devices.*

# Constant Current Regulator



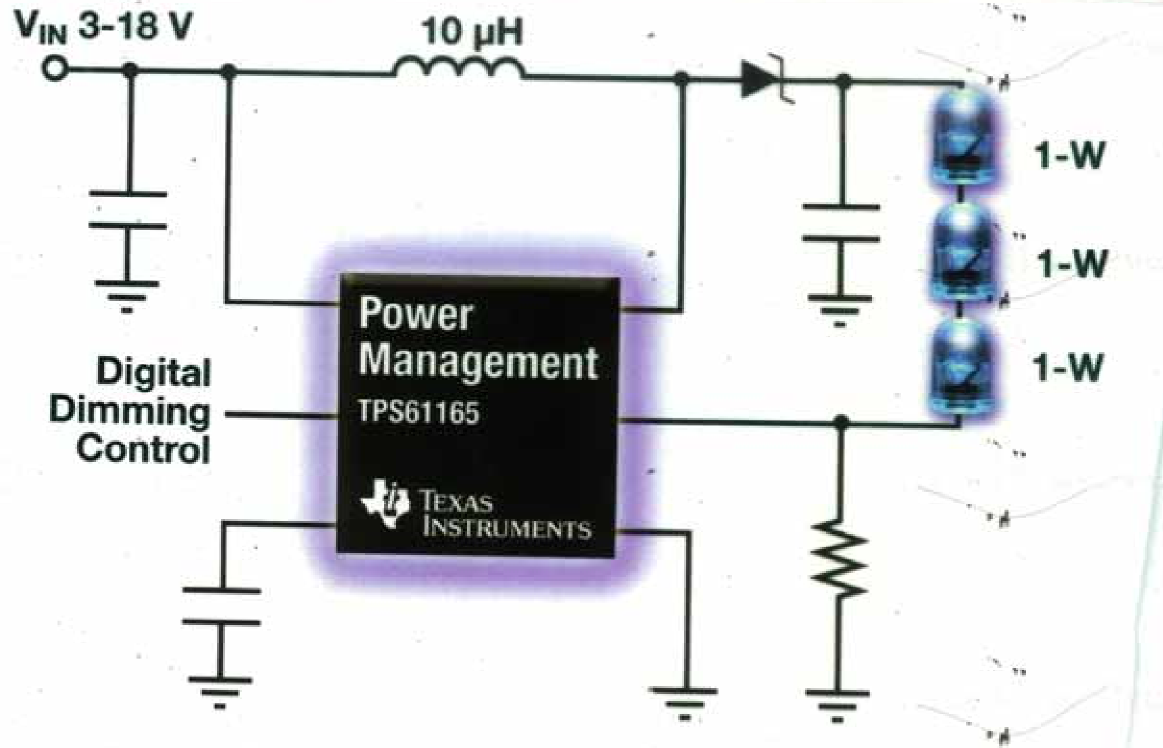

$$I_F = \frac{V_{FB}}{R_{FB}}$$

# Constant Voltage Regulator

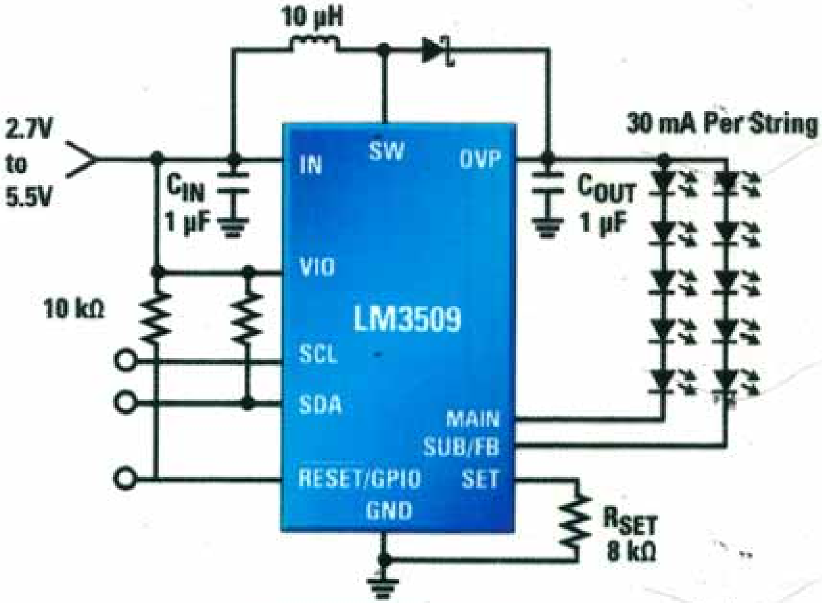



$$V_O = V_{FB} \frac{R_{FB1} + R_{FB2}}{R_{FB1}}$$

# 38-V, 1.2-A Switch Boost Converter



## LM3509 Typical Application Circuit




Dual White LED Bias Supply

| Product family | Metric | Threshold |
|---|---|---|
| Switching regulators/controllers ($V_{IN}/V_{OUT} \geq 7$) | Peak efficiency | ≥ 85% |
| Switching regulators/controllers ($F_{SW} \geq 2$ MHz, $V_{IN}/V_{OUT} \geq 1.5$) | | ≥ 90% |
| Switching regulators/controllers (all others, $V_{IN}/V_{OUT} \geq 1.5$) | | ≥ 95% |
| Switching controllers for isolated power supplies | | ≥ 90% |
| Low-noise linear regulators | $e_N/P_{OUT}$ | ≤10 μVrms/mW |
| LED drivers (boost) | Peak efficiency | ≥ 85% |
| LED drivers (buck) | | ≥ 90% |
| LED drivers (buck-boost) | | ≥ 80% |

**Table.** *PowerWise criteria for power management and LED lighting ICs.*

Industry's first high-current flash LED driver
LM3553
National Semiconductor
LM3553
PowerWise®
LED Driver
Enables single or dual flash LED operation

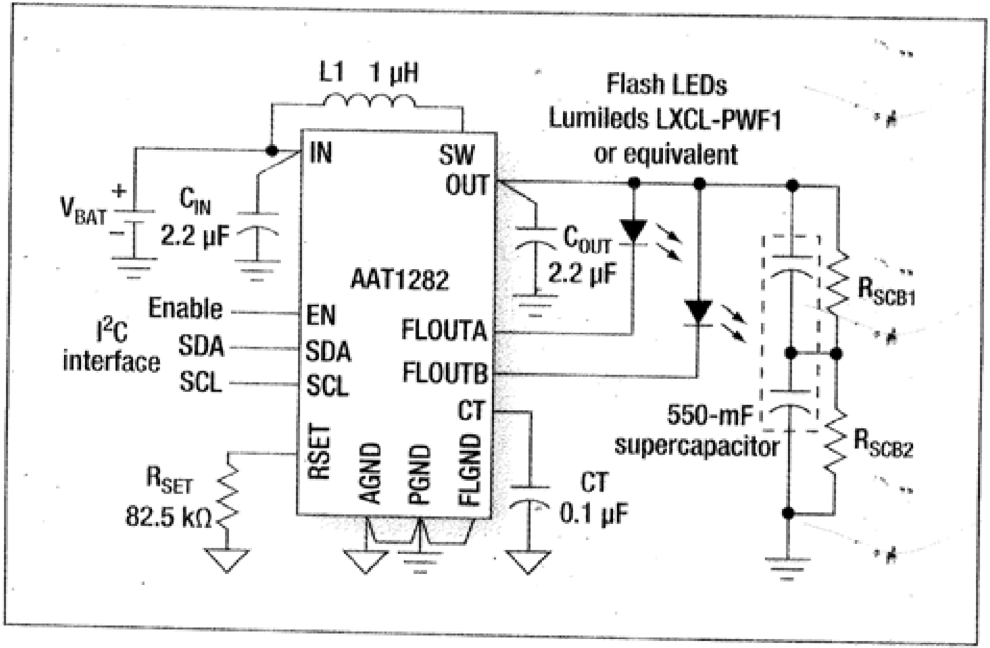



**Fig. 1.** *A 2-A flash LED driver, the AAT1282 stores its output in a supercapacitor, enabling it to drive high-intensity WLEDs in high-megapixel cameras without draining the battery.*

## Applications

- High-power LEDs used in single-cell, battery-powered applications or point-of-load designs with a 9-V or 12-V bus
- White LED backlighting for media form factors up to 9"
  - Ultra-mobile PCs
  - LCD photo frames
  - Industrial laser diodes
  - Medical and industrial lighting

## Features

- Wide input voltage range up to 18V

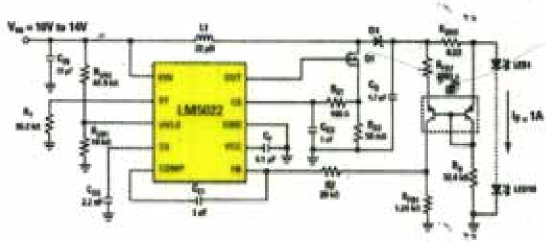
# LM5022 60V Low Side Controller for Boost and SEPIC

## Theory of Operation

The LM5022 is a high voltage low-side N-channel MOSFET controller ideal for use in boost and SEPIC regulators. It contains all of the features needed to implement single ended primary topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent input voltage feed-forward.

The LM5022 includes a start-up regulator that operates over a wide input range of 6V to 60V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 2 MHz and total propagation delays less than 100 ns.

## Typical Application Circuit

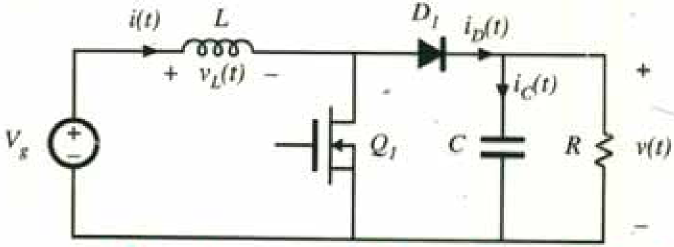


DCM

# 5.3. Boost converter example

Fig 5.12 P 118

Surprise M (D) DCM linear




if $i_L$ runs dry → $D_1$, $D_2$, $D_3$ ⇒ DCM

$i_L$ never < 0

Mode boundary:

$I > \Delta i_L$ for CCM

$I < \Delta i_L$ for DCM

Previous CCM soln: Ch 1-4

$$I = \frac{V_g}{D'^2 R} \qquad \Delta i_L = \frac{V_g}{2L} DT_s$$

DCM R↑ $I_L$↓

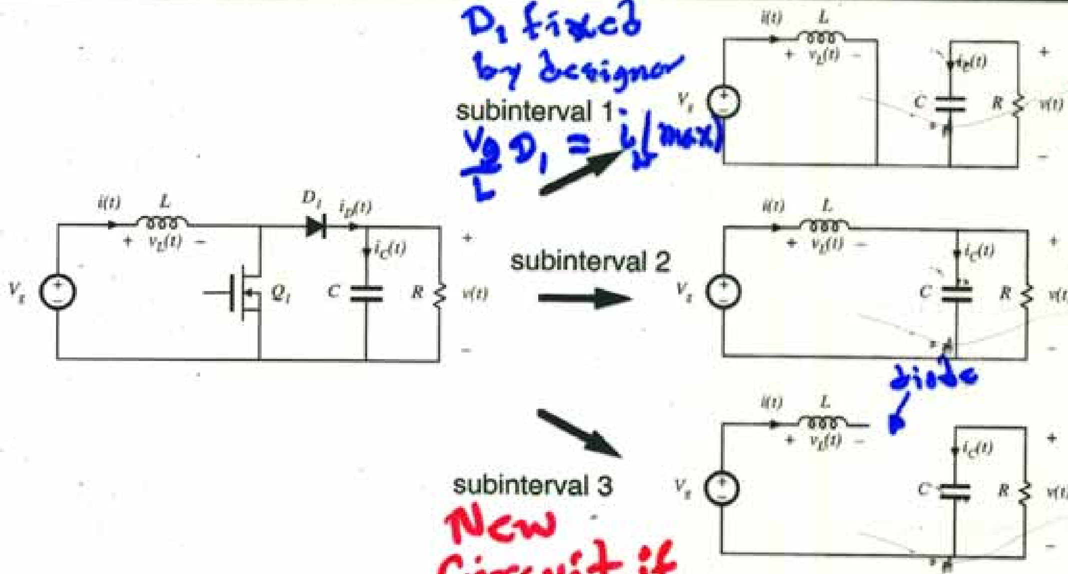
ripple ≠ f(R) $\Delta i_L \sim 1/L$



Can vary $I_L$ and $\Delta i_L$ independently

Fig 5.15 p120

# Conversion ratio: DCM boost




$D_1$ fixed by designer

$\frac{V_g}{L} D_1 = i_L(\max)$

$D_1$

$D_2$

diode

$D_3$

New Circuit if $i_L < 0$



Need 3 Eqs for $D_1$, $D_2$, $D_3$

Defined as?

why max @ D=1/3

# Mode boundary

I > Δi

$$\frac{V_g}{D'^2 R} > \frac{D T_s V_g}{2L} \quad \textit{for CCM}$$

$$\frac{2L}{R T_s} > D D'^2 \quad \textit{for CCM}$$

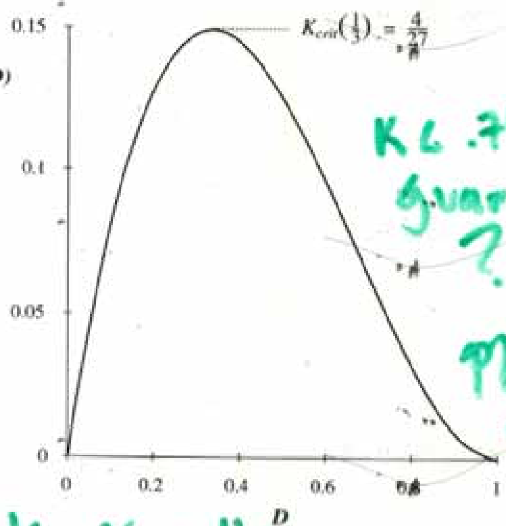
Δi > I

$$K > K_{crit}(D) \quad \textit{for CCM}$$
$$K < K_{crit}(D) \quad \textit{for DCM}$$

where $K = \frac{2L}{R T_s}$ and $K_{crit}(D) = D D'^2$

$K_c = [D - 2D^2 + D^3]$

$dK_c/dD = 0 \Rightarrow D = 1/3 \quad K_c = 4/29$




K < .75 Kc guarantee?

Pbm 5.11

CCM - DCM

# Mode boundary

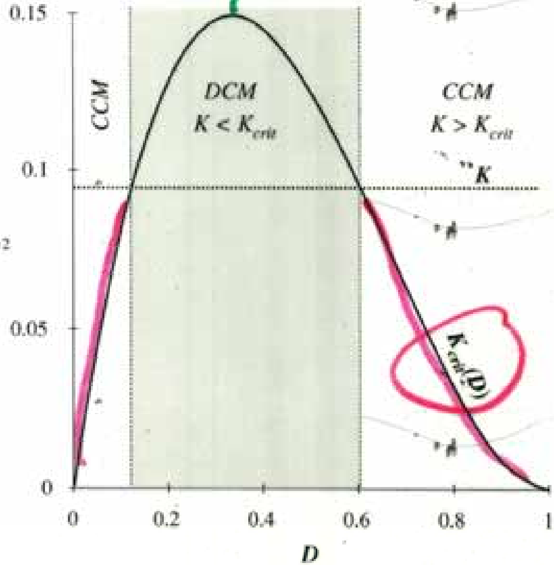
How to find $[K_c]_{max}$?

$K > K_{crit}(D)$ for CCM

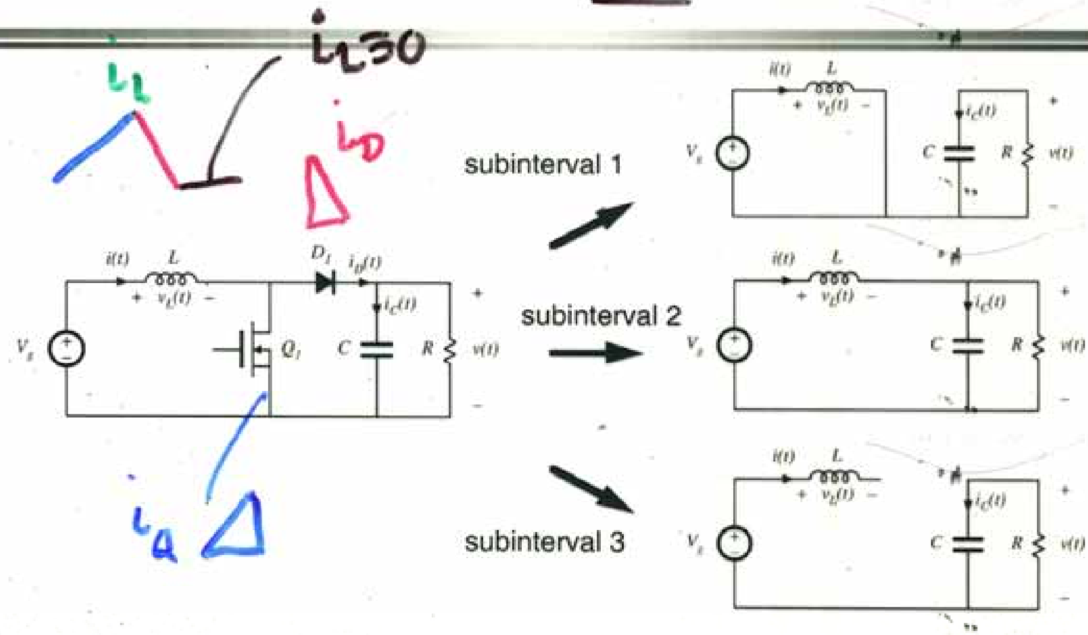
$K < K_{crit}(D)$ for DCM

where $K = \frac{2L}{RT_s}$ and $K_{crit}(D) = DD'^2$

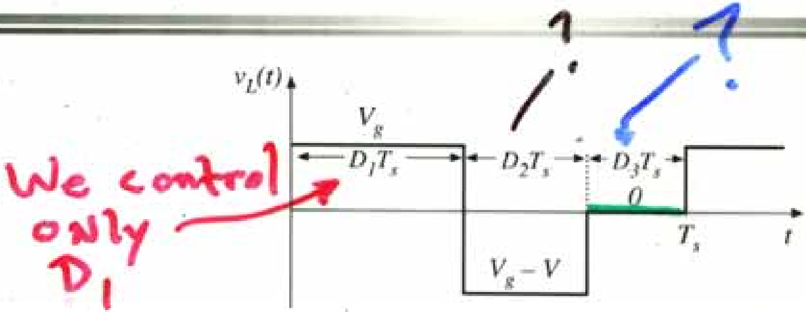
Goal Pbm 5.4



# Conversion ratio: DCM boost



# Inductor volt-second balance




Volt-second balance:

$$D_1 V_g + D_2 (V_g - V) + D_3 (0) = 0$$

Solve for $V$:

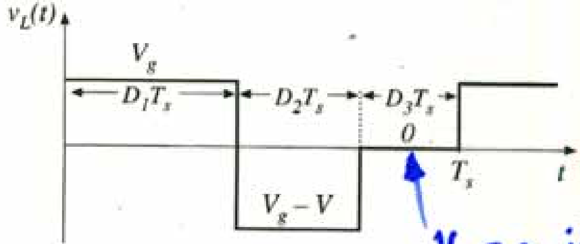
$$V = \frac{D_1 + D_2}{D_2} V_g$$

note that $D_2$ is unknown

For steady state:

# Inductor volt-second balance

Fig 5.16 p 121




Volt-second balance:

$$D_1V_g + D_2(V_g - V) + D_3(0) = 0$$

Solve for $V$:

$$V = \frac{D_1 + D_2}{D_2} V_g$$

note that $D_2$ is unknown

# Capacitor charge balance

node equation:

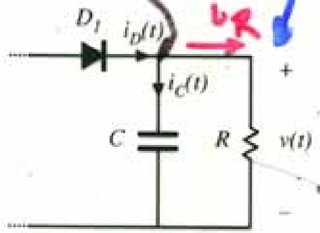
$$i_D(t) = i_C(t) + v(t) / R$$

capacitor charge balance:

$$\langle i_C \rangle = 0$$

hence

$$\langle i_D \rangle = V / R$$




must compute dc component of diode current and equate to load current (for this boost converter example)

# Inductor and diode current waveforms

peak current:

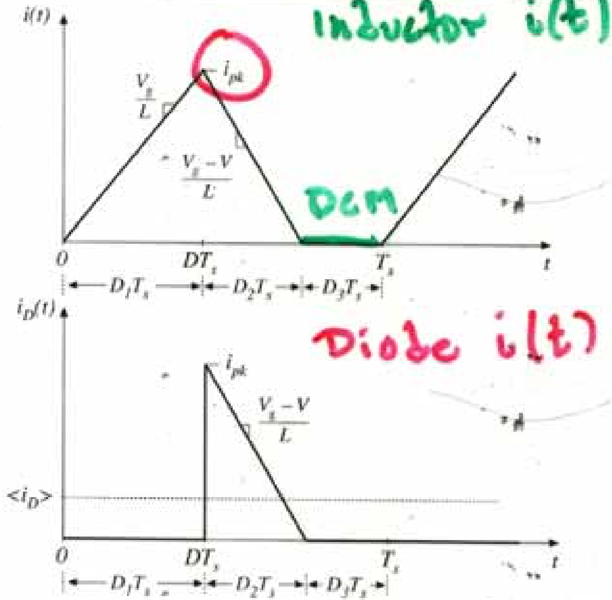
$$i_{pk} = \frac{V_g}{L} D_1 T_s$$

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_D(t)\, dt = \frac{1}{2}\, i_{pk}\, D_2 T_s$$






FET i(t) = ?

# Equate diode current to load current $I_{Load} = \frac{V}{R}$

average diode current:

$$\langle i_D \rangle = \frac{1}{T_s}\left(\frac{1}{2}\, i_{pk}\, D_2 T_s\right) = \frac{V_g D_1 D_2 T_s}{2L}$$

(3) equate to dc load current:

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R} = I_{load}(DC)$$

# Solution for $V$

Two equations and two unknowns ($V$ and $D_2$):

$$V = \frac{D_1 + D_2}{D_2} V_g$$ (from inductor volt-second balance)

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$ (from capacitor charge balance)

Eliminate $D_2$ , solve for $V$. From volt-sec balance eqn:

$$D_2 = D_1 \frac{V_g}{V - V_g}$$

Substitute into charge balance eqn, rearrange terms:

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

# Solution for $V$

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

Use quadratic formula:

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + 4D_1^2 / K}}{2}$$

Note that one root leads to positive $V$, while other leads to negative $V$. Select positive root:

$$\frac{V}{V_g} = M(D_1, K) = \frac{1 + \sqrt{1 + 4D_1^2 / K}}{2}$$

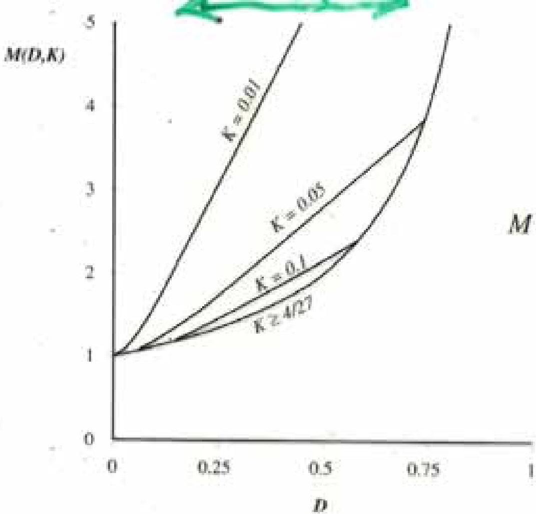
| | |
|---|---|
| where | $K = 2L / RT_s$ |
| valid for | $K < K_{crit}(D)$ |

Transistor duty cycle $D$ = interval *1* duty cycle $D_1$

$\frac{V_o}{V_g}$ (DCM) > $\frac{V_o}{V_g}$ (CCM)

# Boost converter characteristics

$\frac{V_o}{V_g}$ ~ "linear" for range of D




$$M = \begin{cases} \frac{1}{1-D} & \text{for } K > K_{crit} \\ \frac{1+\sqrt{1+4D^2/K}}{2} & \text{for } K < K_{crit} \end{cases}$$

Slope DCM

Approximate $M$ in DCM:

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}}$$

National Website
LM264

Problem 5.4

This is the Watkins-Johnson converter, realized using single-quadrant switches that constrain $i(t)$ to be positive.

a)

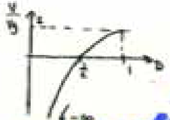
CCM analysis

HW Ch 2

volt-second balance

$$D(V_g - V) + D'(-V_g) = 0$$

$$\Rightarrow V = V_g \frac{D - D'}{D} = V_g \frac{2D-1}{D}$$



charge balance

$$D\left(I - \frac{V}{R}\right) + D'\left(-\frac{V}{R}\right) = 0$$

(1) $\Rightarrow I = \frac{V}{DR} = \frac{V_g}{R} \frac{2D-1}{D^2}$

note $I > 0$ for $D > \frac{1}{2}$

$I < 0$ for $D < \frac{1}{2}$

inductor current ripple

(2) $2\Delta i = \frac{V_g}{L} D' T_s \Rightarrow \Delta i = \frac{V_g D' T_s}{2L}$

Compare I Δi Allows?

$\frac{V_g - V_o}{2L} T_{sw}$

Mode boundary ← CCM to DCM

DCM occurs when $\Delta i > I$

(3) $\frac{V_g D' T_s}{2L} > \frac{V_g}{R} \frac{2D-1}{D^2}$

Be careful! $(2D-1)$ is negative when $D < \frac{1}{2}$

For $D > \frac{1}{2}$:

$$\underbrace{\frac{D^2 D'}{2D-1}}_{K_{crit}} > \underbrace{\frac{2L}{RT_s}}_{K} \quad \text{for DCM}$$

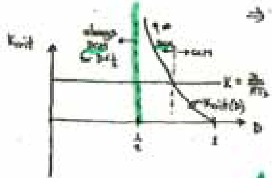
either DCM or CCM depending on?

b) For $D < \frac{1}{2}$ : must reverse direction of inequality

$$\underbrace{\frac{D^2 D'}{2D-1}}_{K_{crit}} < \underbrace{\frac{2L}{RT_s}}_{K} \quad \text{for DCM}$$

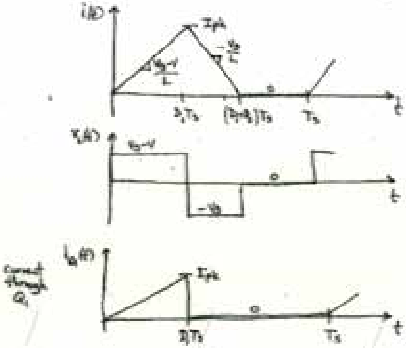
since $K_{crit} < 0$ and $K > 0$, this inequality is always satisfied for $D < \frac{1}{2}$

⇒ converter always operates in DCM when $D < \frac{1}{2}$.




$D > \frac{1}{2}$
CCM or DCM
depends $K_c$ vs $K$

c) In DCM:



Solution of waveforms

$$I_{pk} = \frac{V_g - V}{L} D_1 T_s$$

$$\langle v_L \rangle = 0 = D_1 (V_g - V) + D_2(-V_g)$$ small ripple

$$\langle i_{in} \rangle = \frac{V}{R} = \frac{1}{2} D_1 I_{pk}$$ arch Δ

solve for V:

$$\frac{V}{R} = \frac{1}{2} D_1 \frac{V_g - V}{L} D_1 T_s = (V_g - V)\frac{D_1^2 T_s}{2L}$$

$$V = (V_g - V)\frac{D_1^2}{K} \Rightarrow V\left(1 + \frac{D_1^2}{K}\right) = \frac{D_1^2}{K} V_g$$

$$\frac{V}{V_g} = \frac{1}{\left(1 + \frac{K}{D_1^2}\right)}$$ in DCM

An algorithm for evaluation of $M(D_1, K)$ that works in both CCM and DCM:

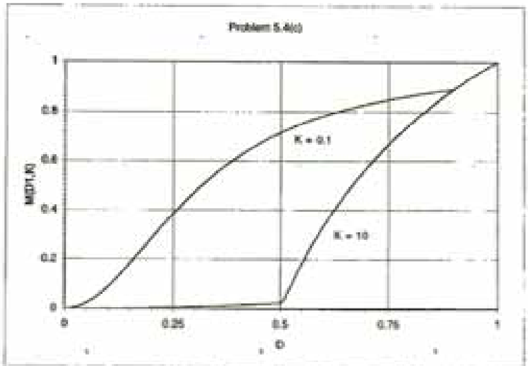
$$M(D_1, K) = \text{MAX}\left(\frac{1}{\left(1 + \frac{K}{D_1^2}\right)}, \frac{2D_1 - 1}{D_1}\right)$$

(take larger of CCM and DCM solutions; solutions intersect at mode boundary)

$T_{CCM}$

see plot on next page

Problem 5.4, part (c)
M(D1, K) for Watkins-Johnson converter with
single-quadrant switches

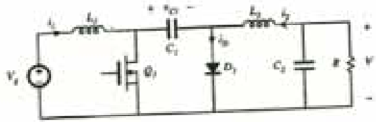



For a given D
two choices $V_o/V_g$
depending on chosen K

L12

...torial

...olution to Problem 5.5
...CM mode boundary analysis
... the Cuk converter




CCM analysis of the Cuk converter is given in Section 2.4. Some results:

$$V_{C1} = \frac{V_g}{D'}$$

$$V = -\frac{D}{D'} V_g$$

$$I_1 = \left(\frac{D}{D'}\right)^2 \frac{V_g}{R}$$

$$I_2 = \frac{D}{D'} \frac{V_g}{R}$$

(note that the polarity of $i_2$ is reversed in Section 2.4, and the quantities $v_{C1}$ and $V$ are called $V_1$ and $V_2$ respectively).

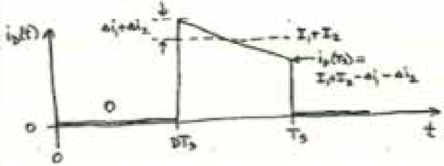
Inductor current ripples (from Eq. (2.57)):

$$\Delta i_1 = \frac{V_g D T_s}{2L_1}$$

$$\Delta i_2 = \frac{V_g D T_s}{2L_2}$$


## Sketch diode current waveform

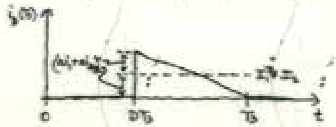
$$i_D(t) = \begin{cases} 0 & \text{during subinterval 1 (diode off)} \\ i_1(t) + i_2(t) & \text{during subinterval 2 (transistor off)} \end{cases}$$



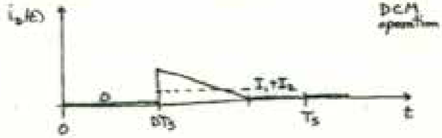

peak $i_D(t) = I_1 + I_2 + \Delta i_1 + \Delta i_2$

## CCM/DCM mode boundary

The dc components of inductor currents, $I_1$ and $I_2$, depend on the load resistance R. The inductor current ripples, $\Delta i_1$ and $\Delta i_2$, do not depend on the load resistance R. When we increase R, $(I_1+I_2)$ decreases but $(\Delta i_1 + \Delta i_2)$ does not change. If we increase R such that $(I_1+I_2) = (\Delta i_1 + \Delta i_2)$, then the diode current will be zero at the end of the switching period: $i_D(T_s) = (I_1+I_2) - (\Delta i_1 + \Delta i_2) = 0$.



If we further increase R, then $i_D(t)$ will reach zero before the end of the switching period. The diode then becomes reverse-biased, and the converter operates in the discontinuous conduction mode:




So the Cuk converter operates in DCM when

$$I_1+I_2 < \Delta i_1 + \Delta i_2$$

Substitute the CCM expressions for $I_1$, $I_2$, $\Delta i_1$, $\Delta i_2$ (note that the CCM analysis is valid at the CCM/DCM boundary):

$$\left(\frac{D}{D'}\right)^2 \frac{V_g}{R} + \frac{D}{D'}\frac{V_g}{R} < \frac{V_g DT_s}{2L_1} + \frac{V_g DT_s}{2L_2}$$

Rearrange terms:

$$\Rightarrow \quad 2\frac{L_1 \| L_2}{R T_s} < (D')^2$$

$$K < K_{crit}(D) \quad \text{for DCM}$$

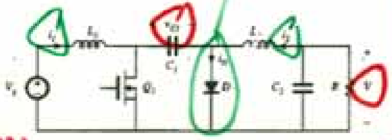
$$\text{with } K = \frac{2\, L_1\|L_2}{R T_s}, \quad K_{crit} = (D')^2$$

<u>End of problem 5.5:</u>

Tutorial

Solution to Problem 5.5
DCM mode boundary analysis
of the Cuk converter

Find: $i_D$ carries $i_1 + i_2$ AC and dc parts!



Cuk is a tandem buck then boost

$I_{in}$ not $I_{out}$ pulsing

Review

CCM analysis of the Cuk converter is given in Section 2.4. Some results:

Pg 24 — Eq 2.53

$$V_{C1} = \frac{V_g}{D'}$$

$$V = -\frac{D}{D'} V_g$$

$$I_1 = \left(\frac{D}{D'}\right)^2 \frac{V_g}{R}$$

$$I_2 = \frac{D}{D'} \cdot \frac{V_g}{R}$$

} f(R)

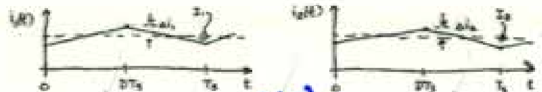
(note that the polarity of $i_2$ is reversed in Section 2.4, and the quantities $v_{c1}$ and $V$ are called $v_1$ and $v_2$ respectively).

Inductor current ripples (from Eq. (2.57)):

$$\Delta i_1 = \frac{V_g D T_s}{2L_1}$$

$$\Delta i_2 = \frac{V_g D T_s}{2L_2}$$

} f(L's)



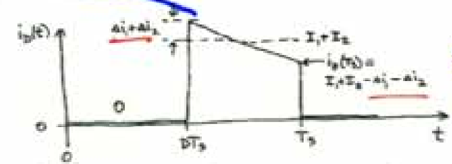
recall: my (web notes) Δi are in phase

Find $i_D$ during $D_1$ & $D_2$ CCM

a) Sketch diode current waveform

$$i_D(t) = \begin{cases} 0 & \text{during subinterval 1 (diode off)} \\ i_1(t) + i_2(t) & \text{during subinterval 2 (transistor off)} \end{cases}$$

Ipeak




CCM operation @ "the border" below

peak $i_D(t) = I_1 + I_2 + \Delta i_1 + \Delta i_2$

b) CCM/DCM mode boundary

The dc components of inductor currents, $I_1$ and $I_2$, depend on the load resistance R. The inductor current ripples, $\Delta i_1$ and $\Delta i_2$, do not depend on the load resistance R. When we increase R, $(I_1 + I_2)$ decreases but $(\Delta i_1 + \Delta i_2)$ does not change. If we increase R such that $(I_1 + I_2) = (\Delta i_1 + \Delta i_2)$ then the diode current will be zero at the end of the switching period: $i_D(T_s) = (I_1 + I_2) - (\Delta i_1 + \Delta i_2) = 0$.

Key use of CCM


CCM/DCM boundary

$i_D$ hits "0" @ $T_s$

If we further increase R, then $i_D(t)$ will reach zero before the end of the switching period. The diode then becomes reverse-biased, and the converter operates in the discontinuous conduction mode:

$\Delta i > I$ (DC) for diode in Cuk

$I_{DC}^{diode} = I_{L_1}(DC) + I_{L_2}(DC)$

$\Delta i^{diode} = \Delta i_{L_1} + \Delta i_{L_2}$


So the Cuk converter operates in DCM when

$$I_1 + I_2 < \Delta i_1 + \Delta i_2$$

Substitute the CCM expressions for $I_1$, $I_2$, $\Delta i_1$, $\Delta i_2$ (note that the CCM analysis is valid at the CCM/DCM boundary):

$$\left(\frac{D}{D'}\right)^2 \frac{V_g}{R} + \frac{D}{D'}\frac{V_g}{R} < \frac{V_g D T_s}{2L_1} + \frac{V_g D T_s}{2L_2}$$

Rearrange terms:

$$\Rightarrow \quad 2\frac{L_1 \| L_2}{R T_s} < (D')^2$$

$$K < K_{crit}(D) \quad \text{for DCM}$$

with $K = \dfrac{2 L_1 \| L_2}{R T_s}$, $K_{crit} = (D')^2$

End of problem 5.5