ECE 562

Week 8 Lecture 1

Fall 2008

Week 8 Lecture 1
Summary

Slides	Topic
3-15	Thyristors and SCR's
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27-29	Mode boundaries
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39-42	Discontinuous conduction mode
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47-57	Summaries

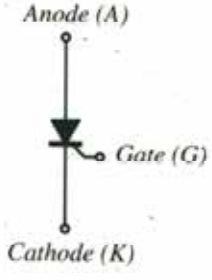
A.C. Power System Switches require V → 100kV I → 10kA

4.2.5. Thyristors (SCR, GTO, MCT)

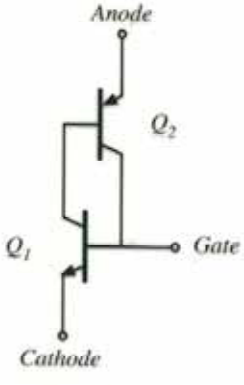
60 Hz ONly 16.66 ms ⇒ Slow switch OK

The SCR

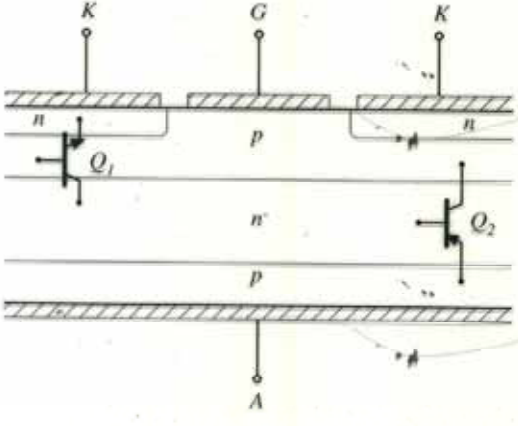
symbol



equiv circuit



construction



Figs 4.46 4.47 Pg 89 Lowest cost sw | First Pe⁻ sw

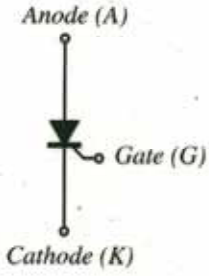
4.2.5. Thyristors (SCR, GTO, MCT)

old only active turn-ON but not turn-off

New Generation active (turn-off) (turn-ON)

The SCR

symbol



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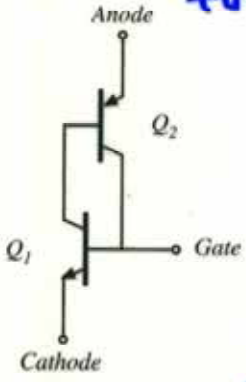

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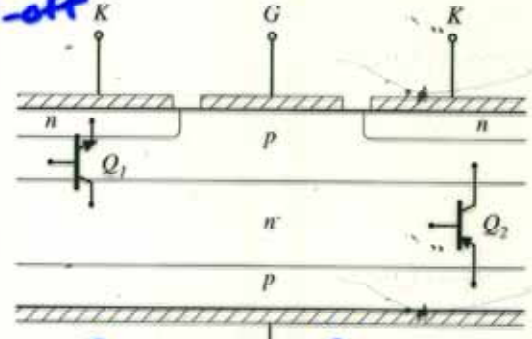

For SCR Latch-up is good!

For CMOS latch is bad effect

The Silicon Controlled Rectifier (SCR)

- Positive feedback —a latching device
- A minority carrier device
- Double injection leads to very low on-resistance, hence low forward voltage drops attainable in very high voltage devices
- Simple construction, with large feature size
- Cannot be actively turned off
- A voltage-bidirectional two-quadrant switch
- 5000-6000V, 1000-2000A devices

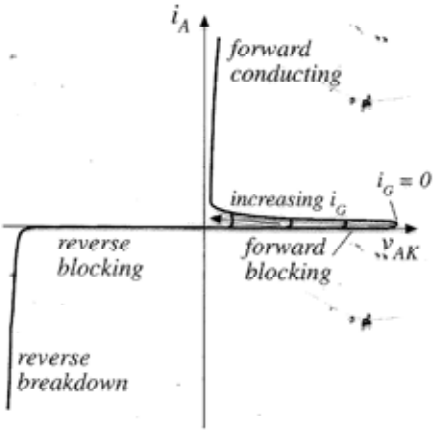

Fig 4.42 pg 90

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- Simple construction, with large feature size
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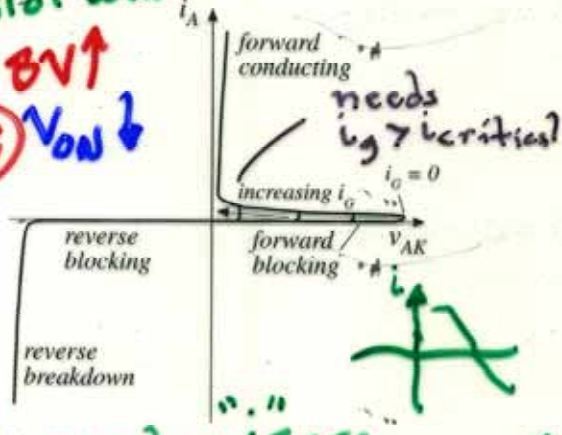
Best of both!
BV↑
V_{ON}↓



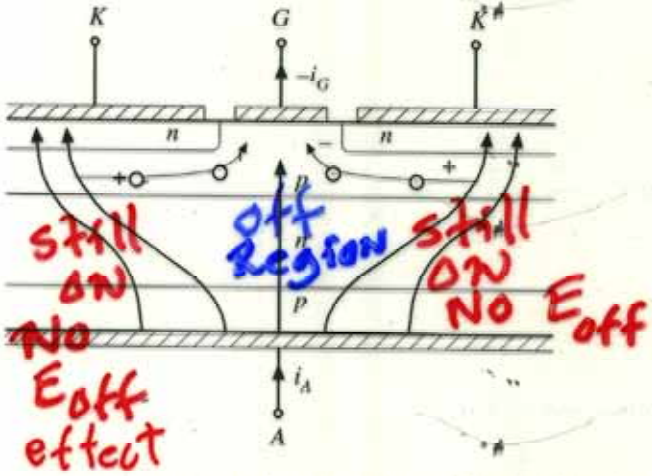
Needs a zero crossing to turn-off

MW switch for power mains

Fig 4.43 P 91

Why the conventional SCR cannot be turned off via gate control

- Large feature size
- Negative gate current induces lateral voltage drop along gate-cathode junction
- Gate-cathode junction becomes reverse-biased only in vicinity of gate contact



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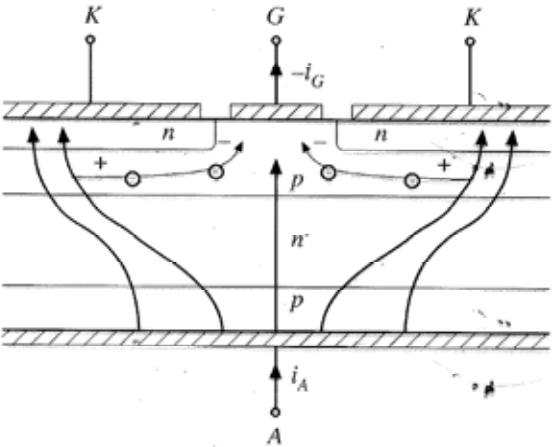
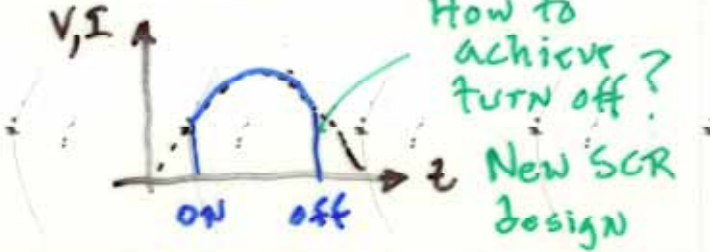


Δt is Variable $0 \rightarrow 180^\circ$

-diode

However conventional SCR NO ability for gate turn off before 180°



The Gate Turn-Off Thyristor (GTO)

- An SCR fabricated using modern techniques —small feature size
- Gate and cathode contacts are highly interdigitated
- Negative gate current is able to completely reverse-bias the gate-cathode junction

Turn-off transition:

- Turn-off current gain: typically 2-5
- Maximum controllable on-state current: maximum anode current that can be turned off via gate control. GTO can conduct peak currents well in excess of average current rating, but cannot switch off

New Device Design

The Gate Turn-Off Thyristor (GTO)

$I_{ON} = 4000\,A$, $V_{off} = 5000\,V$

- An SCR fabricated using modern techniques —small feature size
- Gate and cathode contacts are highly interdigitated
- Negative gate current is able to completely reverse-bias the gate-cathode junction

Active control of t_{off}

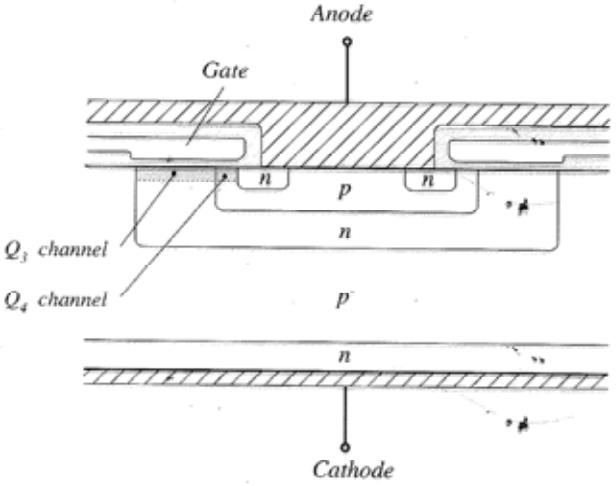
Turn-off transition:

- Turn-off current gain: typically 2-5
- Maximum controllable on-state current: maximum anode current that can be turned off via gate control. GTO can conduct peak currents well in excess of average current rating, but cannot switch off

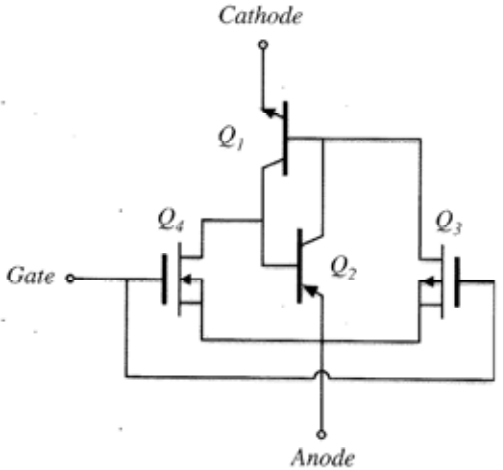
You pay to turn-off $\simeq \frac{1}{3} I_{ON}$ but only briefly limited I_{ON}

The MOS-Controlled Thyristor (MCT)

- Still an emerging device, but some devices are commercially available
- p-type device
- A latching SCR, with added built-in MOSFETs to assist the turn-on and turn-off processes
- Small feature size, highly interdigitated, modern fabrication



The MCT: equivalent circuit



- Negative gate-anode voltage turns p-channel MOSFET Q_3 on, causing Q_1 and Q_2 to latch ON
- Positive gate-anode voltage turns n-channel MOSFET Q_4 on, reverse-biasing the base-emitter junction of Q_2 and turning off the device
- Maximum current that can be interrupted is limited by the on-resistance of Q_4

Summary: Thyristors

- The thyristor family: double injection yields lowest forward voltage drop in high voltage devices. More difficult to parallel than MOSFETs and IGBTs
- The SCR: highest voltage and current ratings, low cost, passive turn-off transition
- The GTO: intermediate ratings (less than SCR, somewhat more than IGBT). Slower than IGBT. Slower than MCT. Difficult to drive.
- The MCT: So far, ratings lower than IGBT. Slower than IGBT. Easy to drive. Second breakdown problems? Still an emerging device.

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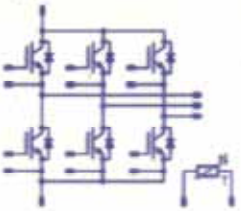
Summary of chapter 4

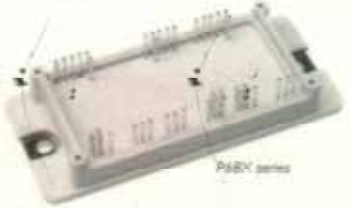
8. The diode and inductor present a "clamped inductive load" to the transistor. When a transistor drives such a load, it experiences high instantaneous power loss during the switching transitions. An example where this leads to significant switching loss is the IGBT and the "current tail" observed during its turn-off transition.
9. Other significant sources of switching loss include diode stored charge and energy stored in certain parasitic capacitances and inductances. Parasitic ringing also indicates the presence of switching loss.

High Power Sixpacks for Motor Drives

*flow*PACK 2 3rd gen up to 150A at 1200V



- IGBT4 technology for low saturation losses and improved EMC behavior
- Low inductance layout and compact design
- High power *flow* 2 housing



Summary of chapter 4

5. Majority carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, controlled essentially by the charging of the device capacitances. However, the forward voltage drops of these devices increases quickly with increasing breakdown voltage.
6. Minority carrier devices, including the BJT, IGBT, and thyristor family, can exhibit high breakdown voltages with relatively low forward voltage drop. However, the switching times of these devices are longer, and are controlled by the times needed to insert or remove stored minority charge.
7. Energy is lost during switching transitions, due to a variety of mechanisms. The resulting average power loss, or switching loss, is equal to this energy loss multiplied by the switching frequency. Switching loss imposes an upper limit on the switching frequencies of practical converters.

Summary of chapter 4

8. The diode and inductor present a "clamped inductive load" to the transistor. When a transistor drives such a load, it experiences high instantaneous power loss during the switching transitions. An example where this leads to significant switching loss is the IGBT and the "current tail" observed during its turn-off transition.
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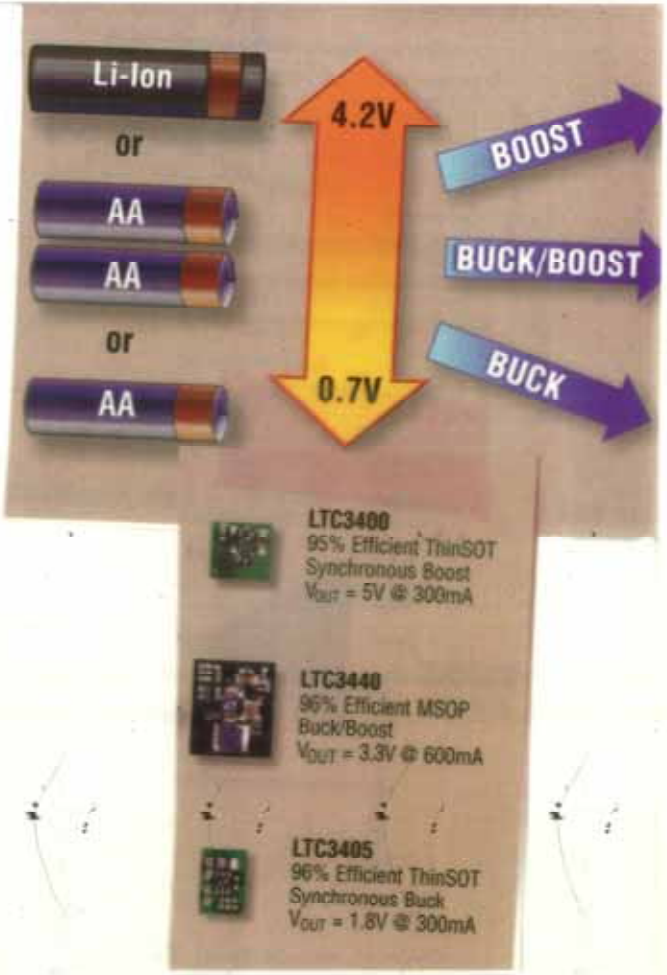

Li-Ion
or
AA
AA
or
AA
4.2V
0.7V
BOOST
BUCK/BOOST
BUCK
LTC3400
95% Efficient ThinSOT
Synchronous Boost
VOUT = 5V @ 300mA
LTC3440
96% Efficient MSOP
Buck/Boost
VOUT = 3.3V @ 600mA
LTC3405
96% Efficient ThinSOT
Synchronous Buck
VOUT = 1.8V @ 300mA

$K \equiv \frac{2L}{RT_{sw}}$

Chapter 5. The Discontinuous Conduction Mode

for same D — New V_o/V_g

3 Circuits, 3 intervals

5.1. Origin of the discontinuous conduction mode, and mode boundary ← Handy for critical conditions

5.2. Analysis of the conversion ratio $M(D,K)$

5.3. Boost converter example

5.4. Summary of results and key points

$K \geq K_c$

$\Delta i \geq I$

L too small Δi too big

unidirectional switch blocks $-i$

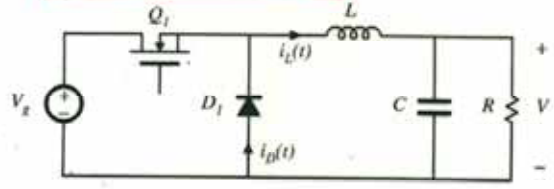
R_L too large or I_{DC} too small

Open ckt load all DCM

Reduction of load current

Fig 5.3 Pg 169

Increase R, until $I = \Delta i_L$



Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

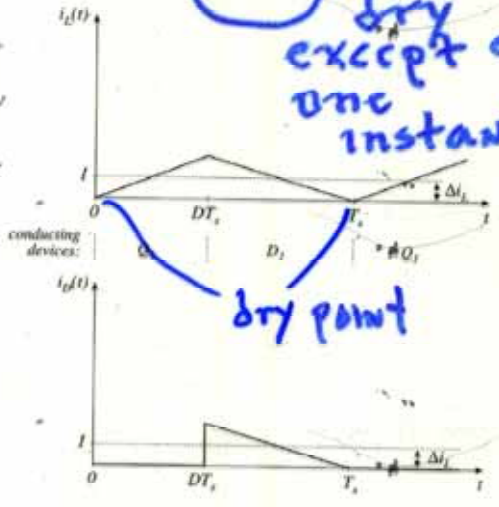
Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

CCM-DCM boundary

Not dry except at one instant



" What if inductor runs dry !! $i_2 = 0$

Chapter 5. The Discontinuous Conduction Mode

Go back to go and recalculate $M(D, R_L)$

Change is: DCM DC gain depends on load

5.1. Origin of the discontinuous conduction mode, and mode boundary

5.2. Analysis of the conversion ratio $M(D,K)$

5.3. Boost converter example

5.4. Summary of results and key points

Before M(D) only

$K \equiv \frac{2L}{RT_{SW}}$

Next M(K,D) !

Web L37 38 39

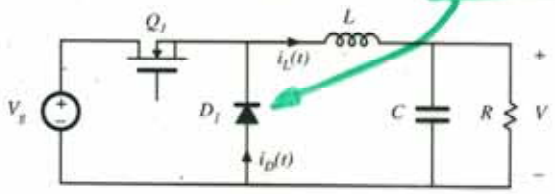
↑ Ch 5 HW

Pg 19-22 HW Hints

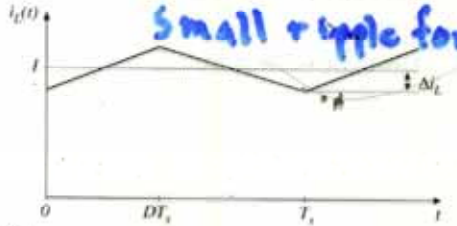
Web All foils

5.1. Origin of the discontinuous conduction mode, and mode boundary

Buck converter example, with single-quadrant switches



continuous conduction mode (CCM)



Small ripple for i_L

Minimum diode current is $(I - \Delta i_L)$

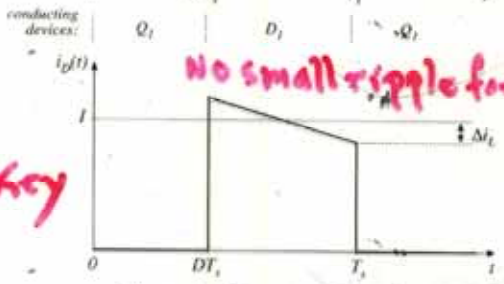
Dc component $I = V/R$

Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

Key

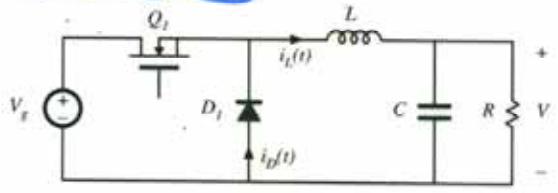


No small ripple for i_D

$R \to \infty$ $\Delta i > I$

Reduction of load current

Increase R until $I = \Delta i_L$



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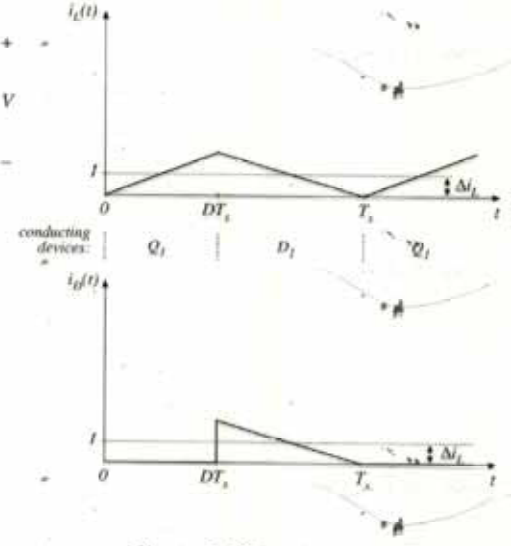
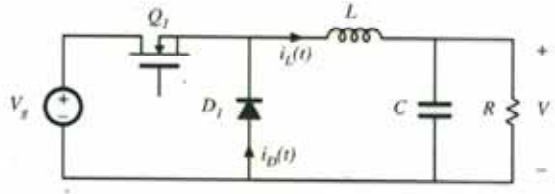
CCM-DCM boundary



Further reduce load current

Increase R some more, such that $I < \Delta i_L$



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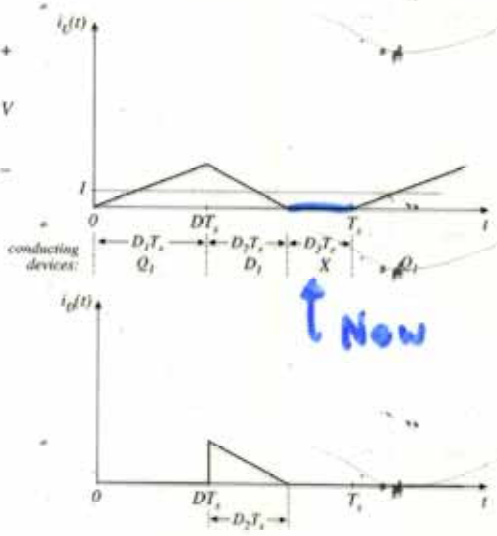
$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

The load current continues to be positive and non-zero.

Discontinuous conduction mode



Mode boundary

$$I > \Delta i_L \quad for\ CCM$$
$$I < \Delta i_L \quad for\ DCM$$

Insert buck converter expressions for I and Δi_L :

$$\frac{DV_g}{R} < \frac{DD'T_s V_g}{2L}$$

CCM Eqs. still valid

Simplify:

Key "K"

$$\frac{2L}{RT_s} < D'$$

This expression is of the form

$$K < K_{crit}(D) \quad for\ DCM$$

where $K = \frac{2L}{RT_s}$ and $K_{crit}(D) = D'$

L too small
R too big
K ↓

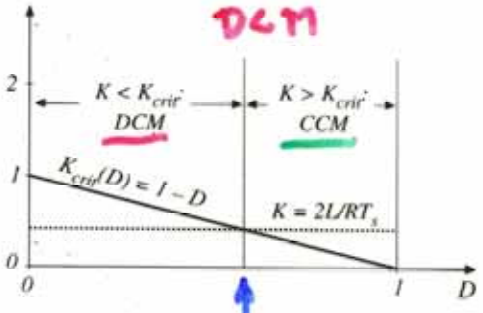
K6 depends on converter

set by design

fixed for each PWM topology

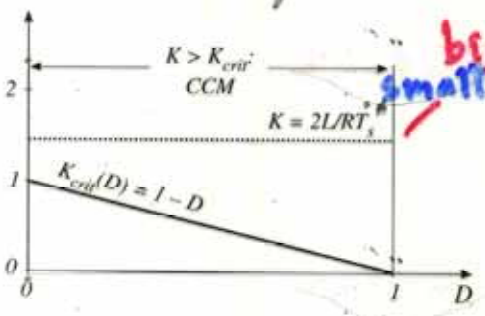
K and K_{crit} vs. D

for $K < 1$: Mixed modes CCM DCM



D (critical)

for $K > 1$: Only CCM



big L small R

Critical load resistance R_{crit} (for fixed L)

Solve K_{crit} equation for load resistance R:

$$R < R_{crit}(D) \quad \text{for CCM} \qquad \text{(big I)}$$

$$R > R_{crit}(D) \quad \text{for DCM} \qquad \text{(small I)}$$

where $$R_{crit}(D) = \frac{2L}{DT_s}$$

Summary: mode boundary

Table 5.1 p 112

$K > K_{crit}(D)$ or $R < R_{crit}(D)$ for CCM

$K < K_{crit}(D)$ or $R > R_{crit}(D)$ for DCM

Way of K — intuitive

Parallel to R_{Load} to ensure?

Table 5.1. CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1}(K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1}(R_{crit})$
Buck	$(1-D)$	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1-D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-boost	$(1-D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$2\frac{L}{T_s}$

Depends on circuit

Unique

Problem 5.1 Buck-boost in DCM

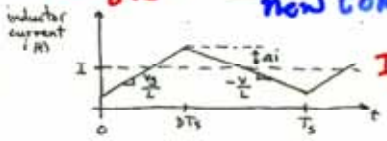
Derive

Eqs found in Table 5.2

a) $I > \Delta i \Rightarrow$ CCM, $I < \Delta \Rightarrow$ DCM

old

new conditions



I_{DC} ↓

from CCM solution: $I = \frac{-V}{D'R} = \frac{DV_g}{D'^2R}$

$\Delta i = \frac{DT_s V_g}{2L}$

start point good till CCM-DCM border

so converter operates in DCM when

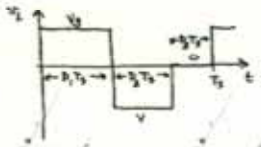
$$\frac{DV_g}{D'^2R} < \frac{DT_s V_g}{2L} \Rightarrow \frac{2L}{RT_s} < (D')^2$$

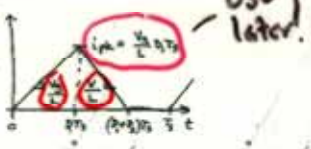
I Δi

or, $K < K_{crit}(D)$ where $K = \frac{2L}{RT_s}$, $K_{crit} = (D')^2$

$K < K_{crit} \Rightarrow$?

b) Inductor waveforms in DCM:





use later!

$\langle v_L \rangle = 0$ Eq

$\langle i_L \rangle = 0$ Eq

inductor volt-second balance

$$\langle v_L \rangle = 0 = D_1 V_g + D_2 V + D_3 \cdot 0 = D_1 V_g + D_2 V$$

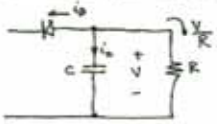
$$\Rightarrow V = -\frac{D_1}{D_2} V_g$$

problem – don't know D_2

(or, to use small ripple approximation here since $|v| \ll |V|$)

V fixed by feedback

capacitor charge balance



node equation:

$$i_D + i_c + \frac{V}{R} = 0$$

charge balance:

$$\langle i_c \rangle = 0$$

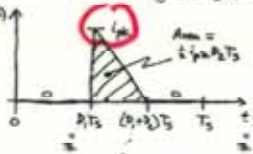
$$\Rightarrow \langle i_D \rangle = -\frac{V}{R}$$

dc load current is supplied by dc component of diode current

so sketch diode current and find its average value

$$i_D(t) = \begin{cases} 0 & \text{during } 0 < t < D_1 T_s \\ i(t) & \text{during } D_1 T_s < t < (D_1 + D_2) T_s \\ 0 & \text{during } (D_1 + D_2) T_s < t < T_s \end{cases}$$

can't use small ripple approximation here: $|v| \gg |V|$!



$$\langle i_D \rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t)\, dt$$

$$= \frac{1}{T_s} \left(\frac{1}{2} i_{pk} D_2 T_s \right)$$

$$= \frac{1}{2} D_2 i_{pk} = \frac{V_g D_1 D_2 T_s}{2L}$$

$R \to \infty$
$K \to 0$

so $\frac{-V}{R} = \frac{V_g D_1 D_2 T_s}{2L} = \frac{D_1}{D_2}\frac{V_g}{R}$

$\Rightarrow D_2^2 = \frac{2L}{RT_s} = K \Rightarrow D_2 = \sqrt{K}$ (take positive root since D_2 cannot be negative)

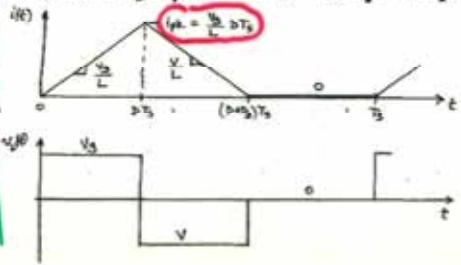
and hence $V = -V_g \frac{D_1}{\sqrt{K}}$

c) Plots see next page for $K = .1$ $\frac{V}{V_g}(D)$

d) For $D = 0.3$, $K_{crit} = (1-0.3)^2 = 0.49 \Rightarrow K < K_{crit} \Rightarrow$ DCM

$K = 0.1 \Rightarrow D_2 = \sqrt{0.1} = 0.32$ and $D_3 = 1 - D - D_2 = 0.38$

Plot



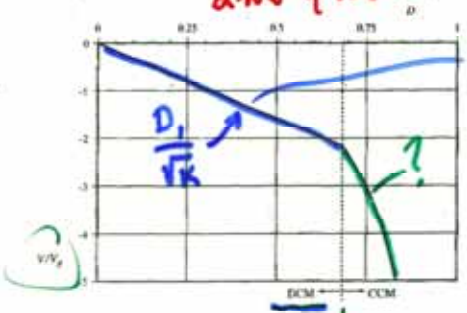
e) At no load, $R \to \infty$ so $K = \frac{2L}{RT_s} \to 0$, DCM. $\frac{V}{V_g} = -\frac{D}{\sqrt{K}} \to -\infty$

In ideal case, $V \to -\infty$. Inductor keeps transferring energy to output capacitor, but there is no load to consume energy.

In practice, output voltage may become very large when load is disconnected. To avoid exceeding device ratings, could (a) connect minimum load to output or (b) reduce D to zero.

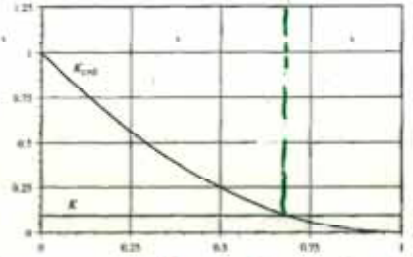
5.1 (c)

Show all Mathcad equations and plot statements



DCM one D for each $\frac{V_o}{V_g}$

e.g. $\frac{V_o}{V_g}$ (DCM Buck Boost is LINEAR

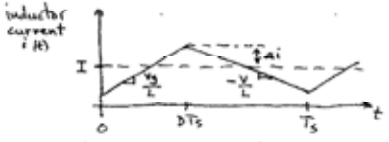


$K < K_c$ DCM Solution

$K > K_c$ CCM Solution

Problem 5.1 Buck-boost in DCM

a) $I > \Delta i \Rightarrow$ CCM, $I < \Delta i \Rightarrow$ DCM



from CCM solution: $I = \frac{-V}{D'R} = \frac{D V_g}{D'^2 R}$

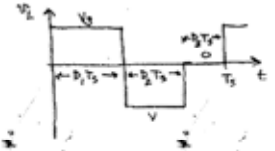
$$\Delta i = \frac{D T_s V_g}{2L}$$

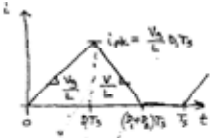
so converter operates in DCM when

$$\frac{D V_g}{D'^2 R} < \frac{D T_s V_g}{2L} \Rightarrow \frac{2L}{RT_s} < (D')^2$$

or, $K < K_{crit}(D)$ where $K = \frac{2L}{RT_s}$, $K_{crit} = (D')^2$

b) Inductor waveforms in DCM:





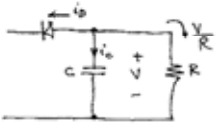
inductor volt-second balance

$$\langle v_L \rangle = 0 = D_1 V_g + D_2 V + D_3 \cdot 0 = D_1 V_g + D_2 V$$

$$\Rightarrow V = -\frac{D_1}{D_2} V_g$$ problem - don't know D_2

(ok to use small ripple approximation here since $|\Delta v| \ll |V|$)

capacitor charge balance



node equation:

$$i_D + i_c + \frac{V}{R} = 0$$

charge balance:

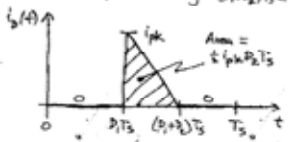
$$\langle i_c \rangle = 0$$

$$\Rightarrow \langle i_D \rangle = -\frac{V}{R}$$ dc load current is supplied by dc component of diode current

so sketch diode current and find its average value:

$$i_D(t) = \begin{cases} 0 & \text{during } 0 < t < D_1 T_s \\ i(t) & \text{during } D_1 T_s < t < (D_1+D_2) T_s \\ 0 & \text{during } (D_1+D_2) T_s < t < T_s \end{cases}$$

can't use small ripple approximation here: $\langle i \rangle \gg I$!



$$\langle i_D \rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t)\, dt$$

$$= \frac{1}{T_s} \left(\frac{1}{2} i_{pk} D_2 T_s \right)$$

$$= \frac{1}{2} D_2 i_{pk} = \frac{V_g D_1 D_2 T_s}{2L}$$

so $\frac{-V}{R} = \frac{V_g D_1 D_2 T_s}{2L} = \frac{D_1}{D_2}\frac{V_g}{R}$

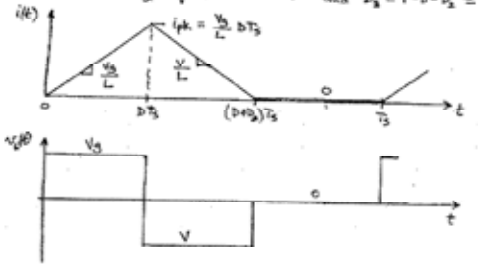
$\Rightarrow D_2^2 = \frac{2L}{RT_s} = K \Rightarrow D_2 = \sqrt{K}$ (take positive root since D_2 cannot be negative)

and hence $V = -V_g \frac{D_1}{\sqrt{K}}$

c) see next page

d) For $D = 0.3$, $K_{crit} = (1-0.3)^2 = 0.49 \Rightarrow K < K_{crit} \Rightarrow$ DCM

$K = 0.1 \Rightarrow D_2 = \sqrt{0.1} = 0.32$ and $D_3 = 1 - D - D_2 = 0.38$

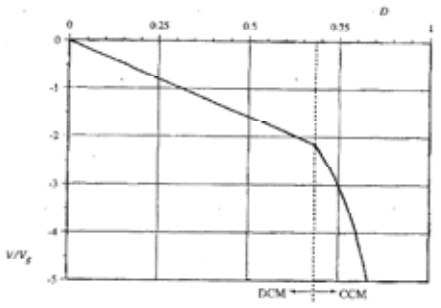


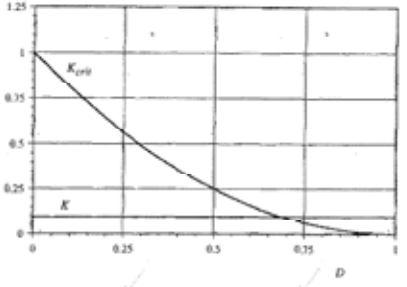
e) At no load, $R \to \infty$ so $K = \frac{2L}{RT_s} \to 0$. DCM: $\frac{V}{V_g} = -\frac{D}{\sqrt{K}} \to -\infty$

In ideal case, $V \to -\infty$. Inductor keeps transferring energy to output capacitor, but there is no load to consume energy.

In practice, output voltage may become very large when load is disconnected. To avoid exceeding device ratings, could (i) connect minimum load to output; or (ii) reduce D to zero.

5.1 (e)


D
0
0.25
0.5
0.75
1
0
-1
-2
-3
-4
-5
V/V_g
DCM
CCM


1.25
1
0.75
0.5
0.25
0
K_crit
K
0
0.25
0.5
0.75
1
D

More stable Ch 7/8/9 2nd semester

Introduction to Discontinuous Conduction Mode (DCM)

diode only one way — 3rd current

- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers having single-quadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:
  - M becomes load-dependent
  - Output impedance is increased
  - Dynamics are altered
  - Control of output voltage may be lost when load is removed

if diodes used $i \to 0$ then 3rd current now current

Why? → open load always DCM

Good! → GOOD for stability - Ch 7/8/9

More Personalities!

Pspice simulations

Introduction to Discontinuous Conduction Mode (DCM)

- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having single-quadrant switches. May also occur in converters having two-quadrant switches.
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- Properties of converters change radically when DCM is entered:
  - M becomes load-dependent
  - Output impedance is increased
  - Dynamics are altered
  - Control of output voltage may be lost when load is removed

Spice Labs

5.2. Analysis of the conversion ratio *M(D,K)*

Analysis techniques for the discontinuous conduction mode:

1. Inductor volt-second balance

$$\langle v_L \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t)\, dt = 0$$

2. Capacitor charge balance

$$\langle i_C \rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t)\, dt = 0$$

} Our small ripple elements

3. Small ripple approximation sometimes applies:

$v(t) \approx V$ because $\Delta v << V$ ← @ V_{IN}, V_{out} even with $\Delta i > I$

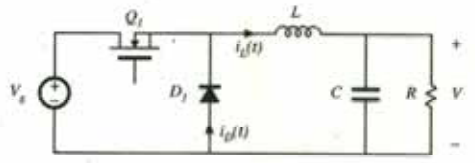
$i(t) \approx I$ is a poor approximation when $\Delta i > I$

Converter steady-state equations obtained via charge balance on each capacitor and volt-second balance on each inductor. Use care in applying small ripple approximation.

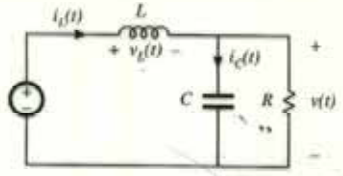
Three Unknowns: D_1, D_2, D_3

Example: Analysis of DCM buck converter $M(D,K)$

Fig 5.9 p 118

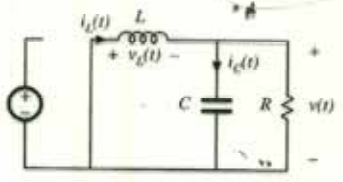


subinterval 1



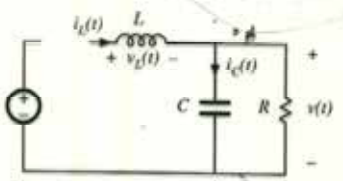
D_1

subinterval 2



D_2

subinterval 3

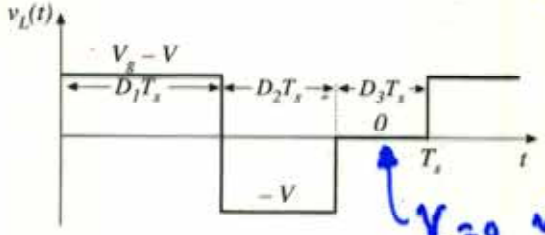


D_3

New Circuit for D_3 diode opens for i reverse

Inductor volt-second balance

Fig 5.8 p 225



Key to understanding

$v_L = 0$ when $i_L = 0$

Volt-second balance:

$$\langle v_L(t) \rangle = D_1(V_g - V) + D_2(-V) + D_3(0) = 0$$

Usually D_1 set by designer

Solve for V:

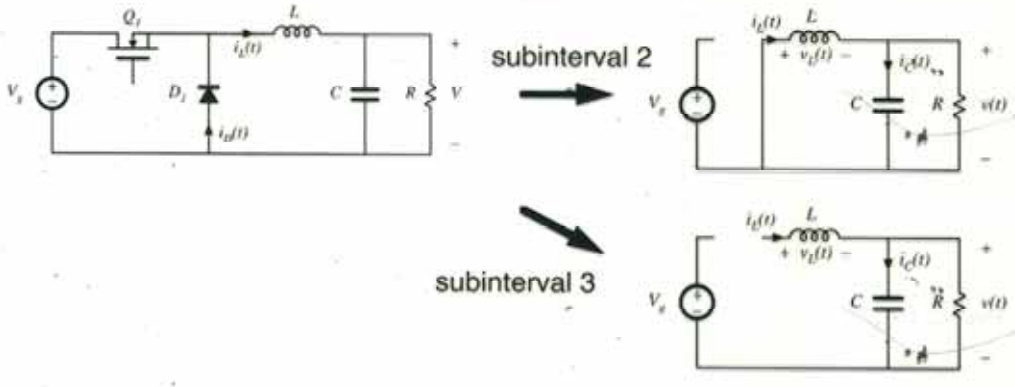
$$V = V_g \frac{D_1}{D_1 + D_2}$$

note that D_2 is unknown

$\frac{V_0}{V_g}$ (CCM Buck) is linear D

Example: Analysis of DCM buck converter *M(D,K)*

$\frac{V_0}{V_g}$ (DCM Buck) is NON linear D



Capacitor charge balance

node equation:

$$i_L(t) = i_C(t) + V / R$$

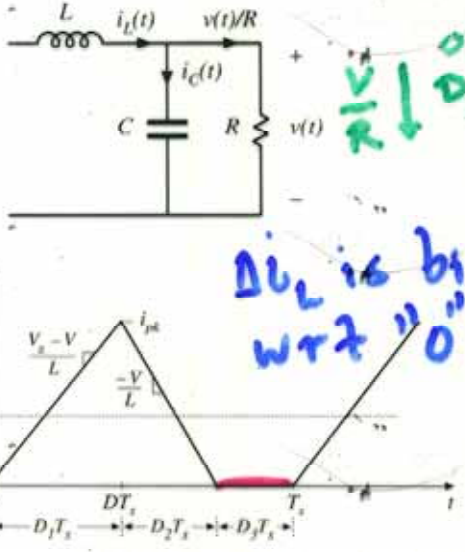
capacitor charge balance:

$$\langle i_C \rangle = 0$$

hence

$$\langle i_L \rangle = V / R$$

must compute dc component of inductor current and equate to load current (for this buck converter example)



Inductor current waveform

peak current:

$$i_L(D_1T_s) = i_{pk} = \frac{V_g - V}{L} D_1 T_s$$

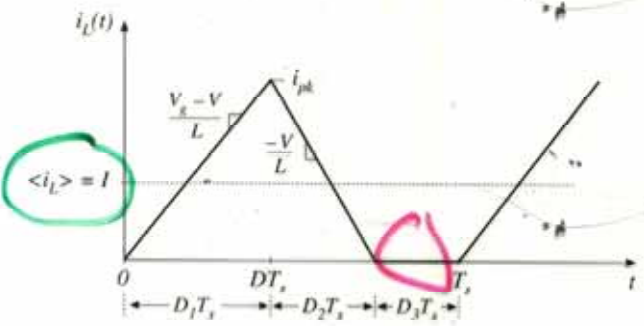
average current:

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_L(t)\, dt = \frac{1}{2} i_{pk} (D_1 + D_2) T_s$$

$$\langle i_L \rangle = (V_g - V) \frac{D_1 T_s}{2L} (D_1 + D_2)$$



equate dc component to dc load current:

$$\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2) (V_g - V)$$

Key!

Solution for V

Two equations and two unknowns (V and D_2):

$$V = V_g \frac{D_1}{D_1 + D_2}$$ (from inductor volt-second balance)

$$\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2) (V_g - V)$$ (from capacitor charge balance)

Eliminate D_2, solve for V:

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + 4K / D_1^2}}$$

where $K = 2L / RT_s$

valid for $K < K_{crit}$

for one $\frac{V}{V_g}$

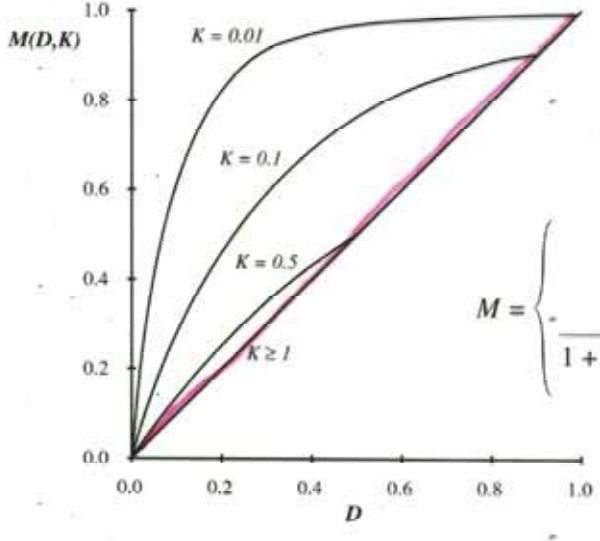
one D_1

possible

$\frac{V_o}{V_g}$ (DCM) > $\frac{V_o}{V_g}$ (CCM)

NON-LINEAR LINEAR

Buck converter $M(D,K)$



$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1+\sqrt{1+4K/D^2}} & \text{for } K < K_{crit} \end{cases}$$

For Buck only the one D matches $\frac{V_o}{V_g}$

But $\frac{V_o}{V_g}$ changes from CCM to DCM

DCM Review

When $\Pi i(AC) \geq I(DC)$

$f_1(D, K)$ $\quad$ $f_2(D, R)$

Define: $K \equiv \frac{2L}{RT_{SW}} = \frac{2L f_{SW}}{R}$

Then each converter has a critical $K \equiv K_c$(critical)

text → D' for buck

Today → $D(D)^2$ for boost

Pbm 5.1 → $(D')^2$ for buck boost

$K > K_c$ for CCM → $R < R_c$

$K < K_c$ for DCM → $R > R_c$

Summary of DCM characteristics

Table 5.2 p124

Unique to topology

Table 5.2. Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	*DCM* $M(D,K)$	*DCM* $D_2(D,K)$	*CCM* $M(D)$
Buck	$(1-D)$	$\frac{2}{1+\sqrt{1+4K/D^2}}$	$\frac{K}{D}M(D,K)$	D
Boost	$D(1-D)^2$	$\frac{1+\sqrt{1+4D^2/K}}{2}$	$\frac{K}{D}M(D,K)$	$\frac{1}{1-D}$
Buck-boost	$(1-D)^2$	$-\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\frac{D}{1-D}$

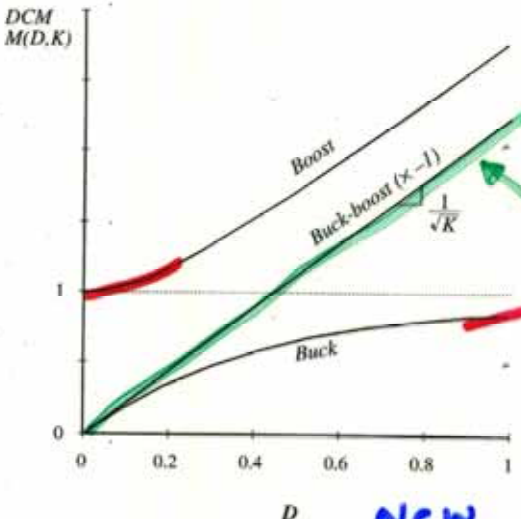
HW 5.1

with $K = 2L/RT_s$ *DCM occurs for* $K < K_{crit}$

K Methodology

Summary of DCM characteristics

Fig 5.20 p125



- DCM buck and boost characteristics are asymptotic to $M = 1$ and to the DCM buck-boost characteristic
- DCM buck-boost characteristic is linear
- CCM and DCM characteristics intersect at mode boundary. Actual M follows characteristic having larger magnitude
- DCM boost characteristic is nearly linear

slope = ?

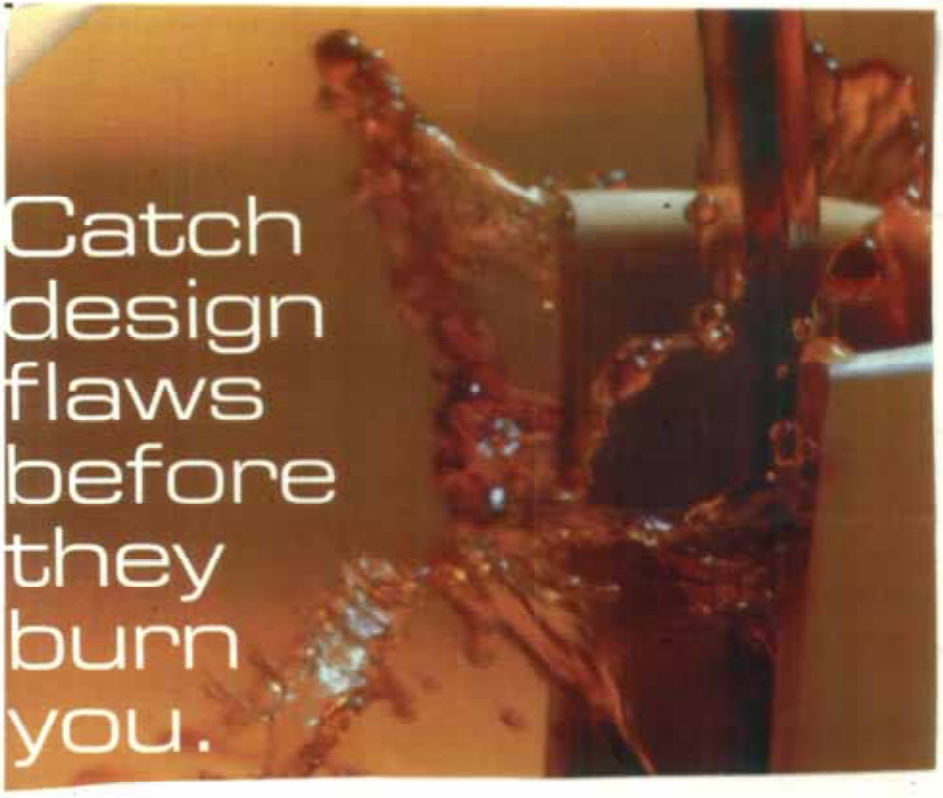
New M(D) Shape

Summary of key points

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on-state current or off-state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.

Summary of key points

4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.
5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.


Catch
design
flaws
before
they
burn
you.

"I guess we didn't really think about the prospect of her burning up on re-entry."

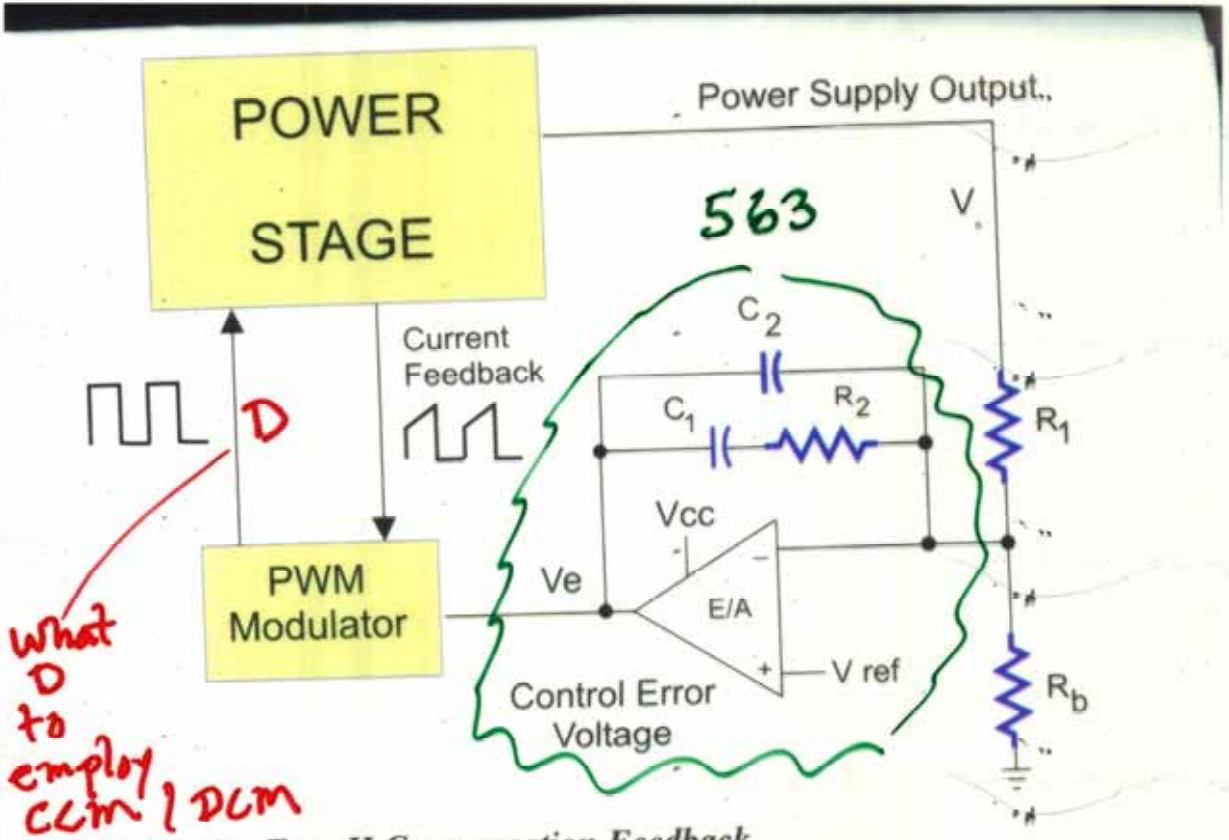


Figure 1a: Type II Compensation Feedback