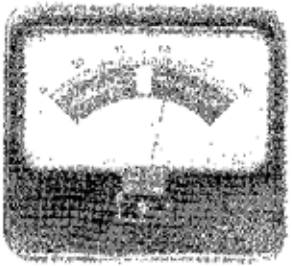
ECE 562

Week 7 Lecture 1

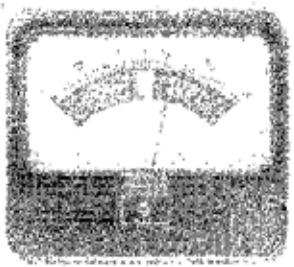
Fall 2008

Week 7 Lecture 1 Summary

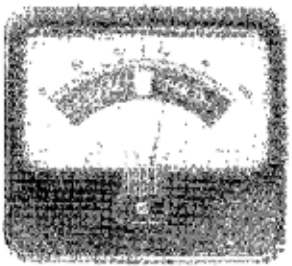
- Section notes
  - Slides 3-5 – In-class talk criteria
  - Slides 6-13 – Homework review
  - Slides 14-19 – Packaging and cooling
  - Slide 20 – Thermal – class participation
  - Slides 21-34 – Heat transfer
  - Slides 35-36 – P-N junction cooling
  - Slides 37-51 – Power diodes
  - Slides 52-66 – Diode characteristics
  - Slides 67-81 – Bipolar junction transistors



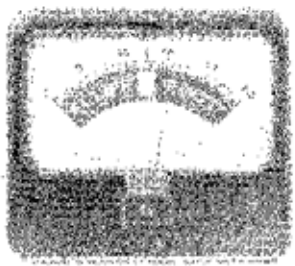
PERFORMANCE



CLARITY



RISK



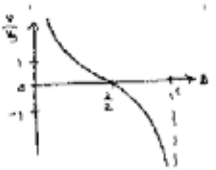
VOICE STYLE

"We've all dozed off during a PowerPoint, Bentham, but today was over the top."

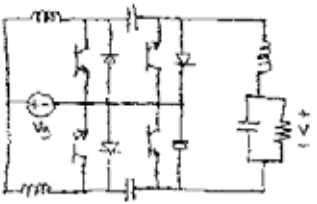
"This is a story about a man and a desk and a flow chart."

Problem 4.5 Push-pull Ćuk amplifier

$$\frac{V}{V_g} = \frac{D'}{D} - \frac{D}{D'} = \frac{1-2D}{DD'}$$



Requires current-bidirectional two-quadrant switches



Prob. 4.5

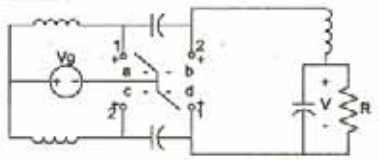
How many?

L

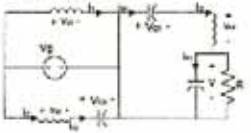
C

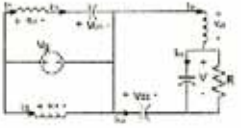
$\Rightarrow \langle v_c \rangle$

$\langle i_o \rangle$



First the equations:





$v_{L1}(t) \approx V_g$; $v_{L2}(t) \approx V_g - V_{c2}$;
$v_{L3}(t) \approx -V_{c2} - V$
$i_{c1}(t) \approx I_1$; $i_{c2}(t) \approx I_2$; $i_{c3}(t) \approx I_3 - V/R$

$v_{L1}(t) \approx V_g - V_{c1}$; $v_{L2}(t) \approx V_g$;
$v_{L3}(t) \approx V_{c1} - V$
$i_{c1}(t) \approx I_1$; $i_{c2}(t) \approx -I_2$;
$i_{c3}(t) \approx I_3 - V/R$

Thus:

3

$\langle v_{L1} \rangle = V_g D + (V_g - V_{c1})D' = 0$
$\langle v_{L2} \rangle = (V_g - V_{c2})D + (V_g)D' = 0$
$\langle v_{L3} \rangle = (-V_{c1} - V)D + (V_{c2} - V)D' = 0$

$V_{c1} = V_g/D'$
$V_{c2} = V_g/D$
$V = Vg[D'/D] - [D/D']$

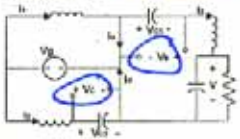
3

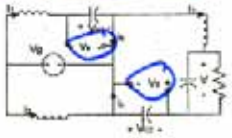
$\langle i_{c1} \rangle = I_1 D + I_1 D' = 0$
$\langle i_{c2} \rangle = I_2 D + (-I_2)D' = 0$
$\langle i_{c3} \rangle = (I_3 - V/R)D + (I_3 - V/R)D' = 0$

$I_1 = -VD'/RD'$
$I_2 = VD'/RD$
$I_3 = V/R$

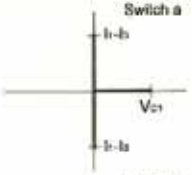
From these equations we know tha V_{c1} and V_{c2} are always positive, V is positive for $D < 0.5$ and negative for $D > 0.5$, I_1 is positive for $D > 0.5$ and negative for $D < 0.5$, and I_2 and I_3 are positive for $D < 0.5$ and negative for $D > 0.5$.

Now we need the open circuit voltages and the closed circuit currents for each switch.

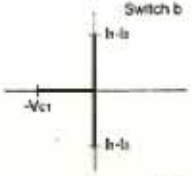




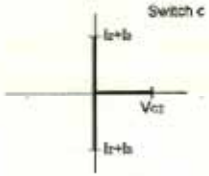
switch a: $I_a = I_1 - I_3$ conducts (closed)
$V_a = V_{c1}$ blocks (open)



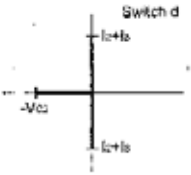
switch b: $I_b = I_1 - I_3$ conducts (closed)
$V_b = -V_{c2}$ blocks (open)



switch c: $I_c = I_2 + I_3$ conducts (closed)
$V_c = V_{c2}$ blocks (open)

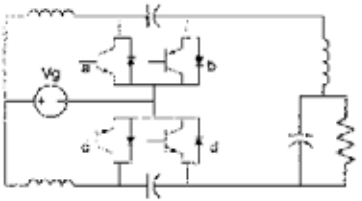


switch d: $I_d = I_2 + I_3$ conducts (closed)
$V_d = -V_{dc}$ blocks (open)



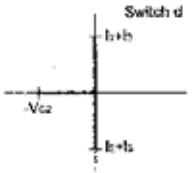
So we need 4 parallel RF diodes combinations. Two of them are reversed (Switches b and d).

The Final picture:



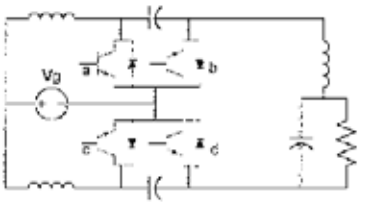
Note: Again the switches could be replaced by the MOSFET but the explanation from Problem 4.4 above can be a deterant for using the MOSFET's.

switch d: $I_d = I_2 + I_3$ conducts (closed)
$V_d = -V_{c2}$ blocks (open)



So we need 4 parallel BJT diodes combinations. Two of them are reversed (Switches b and d).

The Final picture:



Note: Again the switches could be replaced by the MOSFET but the explanation from Problem 4.4 above can be a deterant for using the MOSFET's.

4.3.4. Efficiency vs. switching frequency

$f_{sw}\uparrow$ η ?

Add up all of the energies lost during the switching transitions of one switching period:

diode Q_{rr}

$$W_{tot} = W_{sn} + W_{off} + W_D + W_C + W_L + \ldots$$

DC

stored energy

Average switching power loss is

$$P_{sw} = W_{tot} f_{sw}$$

Plus gate drive loss

$C_g V_g^2 f$

Big for $f \geq 100$ MHz

Total converter loss can be expressed as

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot} f_{sw}$$

where

P_{fixed} = fixed losses (independent of load and f_{sw})
P_{cond} = conduction losses

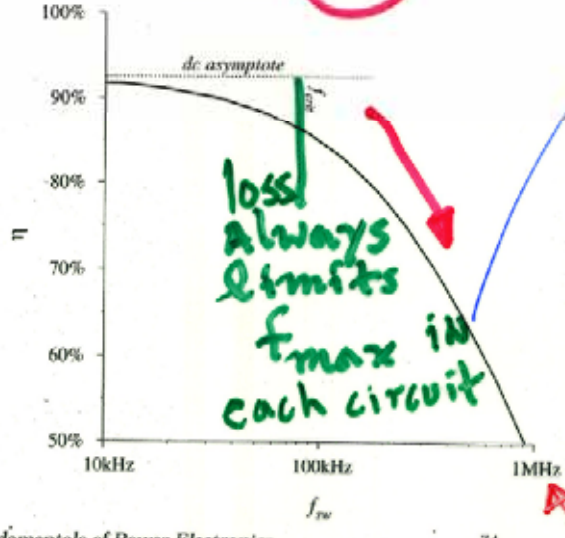
Downsize fow 1

Fig 4.55 pg 101

Efficiency vs. switching frequency

EE564 solves this problem ZVS, ZCS!

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot} f_{sw}$$



loss always limits f_{max} in each circuit

Switching losses are equal to the other converter losses at the critical frequency

$$f_{crit} = \frac{P_{cond} + P_{fixed}}{W_{tot}}$$

This can be taken as a rough upper limit on the switching frequency of a practical converter. For $f_{sw} > f_{crit}$, the efficiency decreases rapidly with frequency.

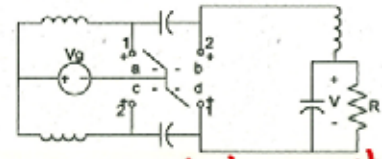
2004 moved to 5 MHz

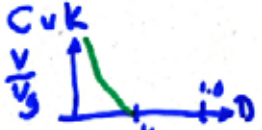
Pick: V_g, V_{out}, ? $\pm R_{out} \pm$?, Ripple

Push-pull

Cuk

Prob. 4.5

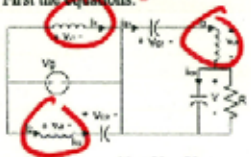


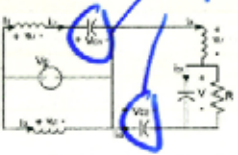


3 inductor currents

3 Caps

First the equations:





$v_{L1}(t) \approx V_g$; $v_{L2}(t) \approx V_g - V_{c2}$;
$v_{L3}(t) \approx -V_{c1} - V$
$i_{c1}(t) \approx I_3$; $i_{c2}(t) \approx I_2$; $i_{c3}(t) \approx I_3 - V/R$

$v_{L1}(t) \approx V_g - V_{c1}$; $v_{L2}(t) \approx V_g$;
$v_{L3}(t) \approx V_{c2} - V$
$i_{c1}(t) \approx I_1$; $i_{c2}(t) \approx -I_3$;
$i_{c3}(t) \approx I_3 - V/R$

Thus:

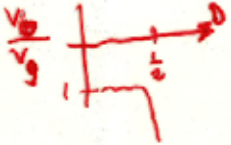
$\langle v_{L1} \rangle = V_g D + (V_g - V_{c1})D' = 0$
$\langle v_{L2} \rangle = (V_g - V_{c2})D + (V_g)D' = 0$
$\langle v_{L3} \rangle = (-V_{c1} - V)D + (V_{c2} - V)D' = 0$
$\langle i_{c1} \rangle = I_3 D + I_1 D' = 0$
$\langle i_{c2} \rangle = I_2 D + (-I_3)D' = 0$
$\langle i_{c3} \rangle = (I_3 - V/R)D + (I_3 - V/R)D' = 0$

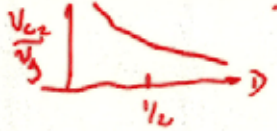
Key

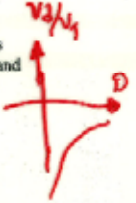
$V_{c1} = V_g/D'$
$V_{c2} = V_g/D$
$V = Vg([D'/D] - [D/D'])$
$I_1 = -VD/RD'$
$I_2 = VD'/RD$
$I_3 = V/R$

$\frac{V}{V_g}\left[\frac{D^2 - D'^2}{DD'}\right]$

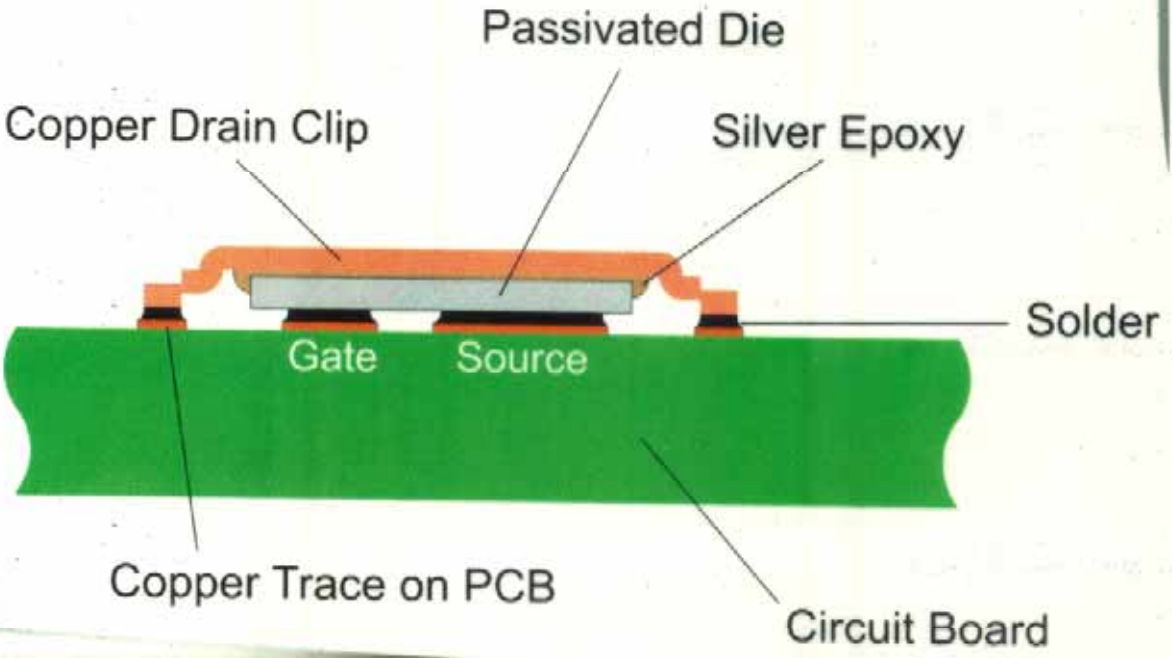
From these equations we know tha V_{c1} and V_{c2} are always positive, V is positive for $D < 0.5$ and negative for $D > 0.5$, I_3 is positive for $D > 0.5$ and negative for $D < 0.5$, and I_2 and I_3 are positive for $D < 0.5$ and negative for $D > 0.5$.








TO247
TO220
D PAK
DirectFET™
Power
Package
Evolution


Passivated Die
Copper Drain Clip
Silver Epoxy
Solder
Gate
Source
Copper Trace on PCB
Circuit Board

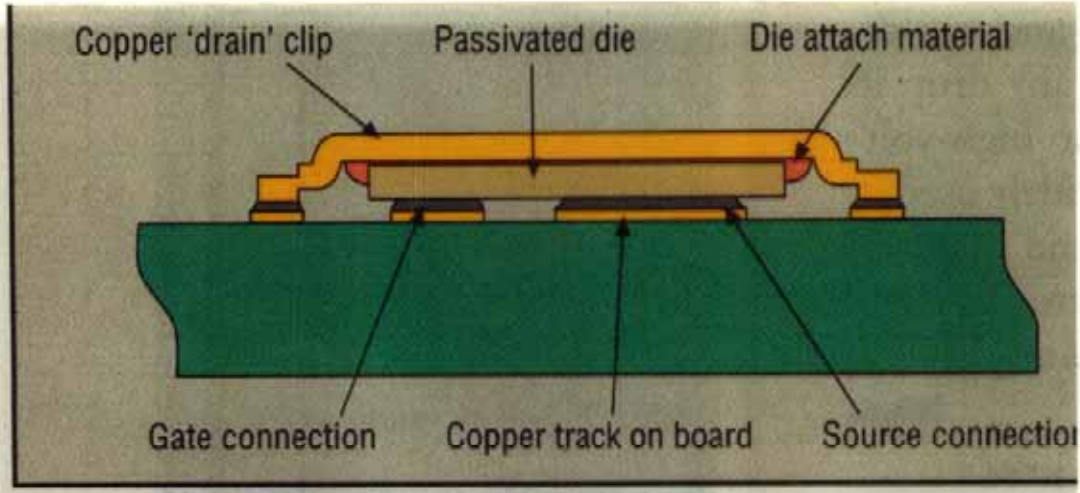


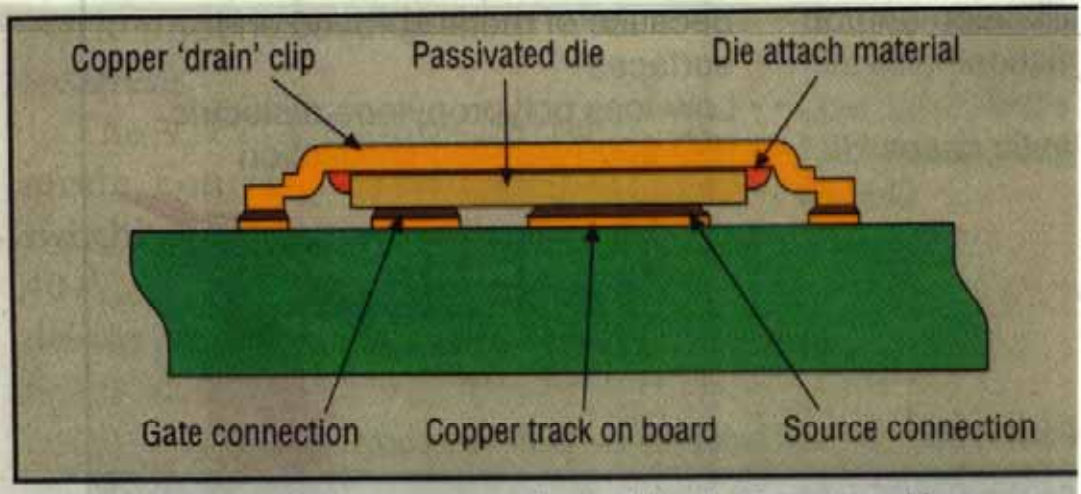
Fig. 1. *DirectFET packaging cross section.*

$i_{sd} \approx 100\,A \Rightarrow P_{loss\ FET} \approx 30\,W$

multi-phase buck

$R_{DS(ON)} = 3m\Omega$

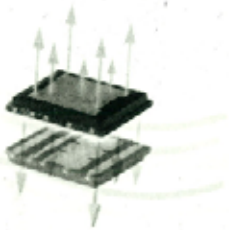
$P(\text{gate drive}) \approx 10\%\, P_{out}$ for RF FETs



Because it allows heat to escape through both the top and bottom sides of the device, IR's DirectFET package cools the die more efficientl than previous surface-mount packages, which transfer almost all of their heat into the pc board.

High Thermal Efficiency Package!
SO-8 6*5mm

Double-Sided-Cooling MOSFETs With Up to 48 % Lower On-Resistance



Industry's Lowest On-Resistance for Point-of-Load, OR-ing and Secondary Side DC/DC Applications

- 1.4 mΩ max for 20-V device; 2.6 mΩ max for 40-V device
- $r_{DS(on)} \times Q_g$ up to 12 % lower than competition

Dual Thermal Paths

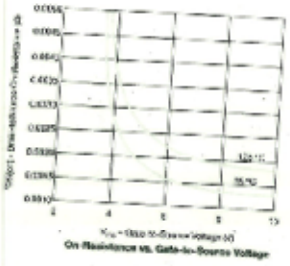
- Top (1 °C/W) and bottom (1 °C/W) cooling provides dual heat dissipation paths for forced air applications
- Double the SO-8 current density (>60 A) in same footprint for space and cost savings

Leadframe-Based Surface-Mount Packaging

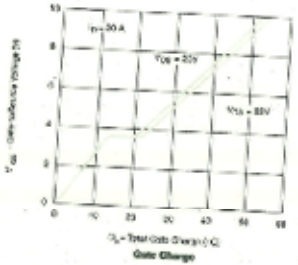
- Easy handling enables high assembly yield
- Plastic encapsulation provides good die protection and reliability
- Fixed footprint and pad layout independent of die size across range of family

Pb **RoHS** COMPLIANT

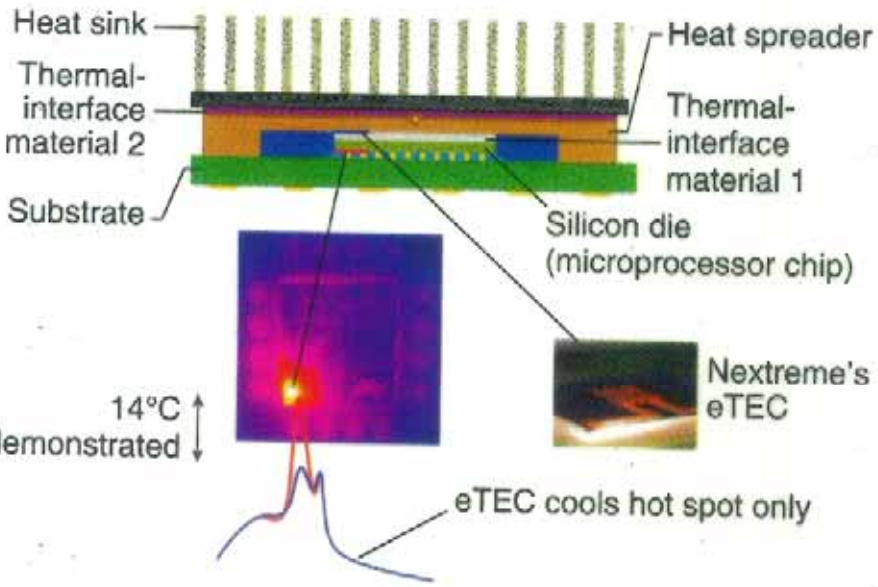
Multi-Sourcing Available



On-Resistance vs. Gate-to-Source Voltage



Gate Charge



Nextreme's thin-film thermoelectric cooler, eTEC, cools a hot spot on a semiconductor chip. This particular implementation is for a silicon microprocessor. (*Courtesy of Nextreme*)

Class participation grade

Detail

Thermal conductivity

Thermal exchange coefficient

Thermal Resistance

Thermal Diffusivity

1 Various Expressions and How interrelated

2 Various Units

3 Associated heat flow equations

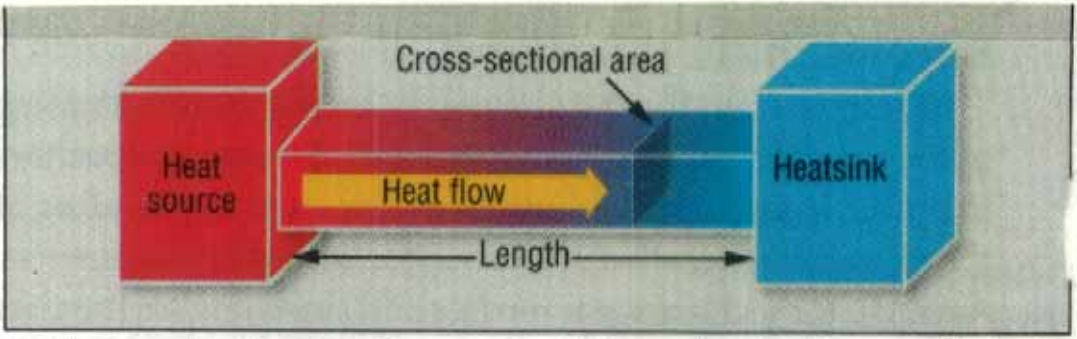


Fig. 1. *In conduction, heat is transferred from a hot body to a cold body via a solid medium.*

σ_{Th} units $\frac{W}{m \cdot {}^{o}K}$

Material	Thermal conductivity (W/mK)
Diamond	1000 to 2600
Silver	406
Copper	385
Gold	320

future

now

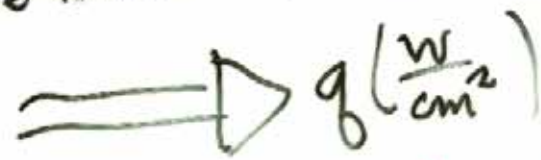
Table 1. *Material thermal conductivities.*

Also use Thermal Resistance Θ $\frac{\Delta(^{o}C)}{W}$

Given that $P_{diss}(W)$ is known

Given Area of part cm^2

We know the heat flux



How to estimate temp rise of part?

Requires heat transfer properties $K_{Thermal}$ of the part or Θ

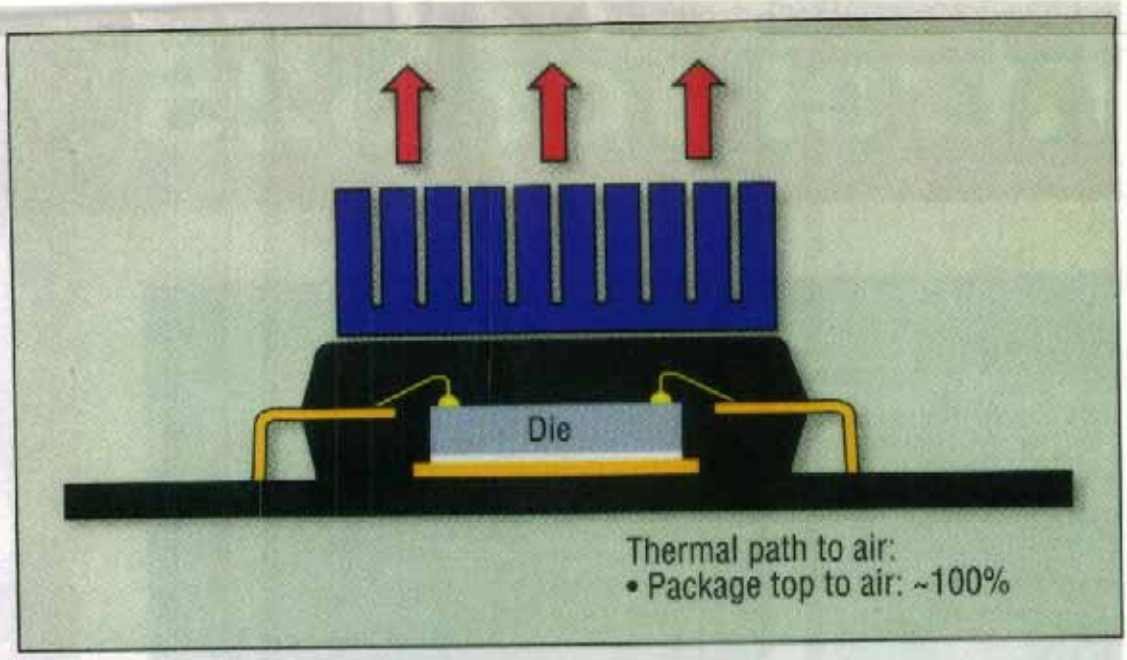


Fig. 7. *For nondigital temperature sensors such as the AD590, a current-output temperature sensor, the value of θ_{JC} indicates the ease of heat flow.*

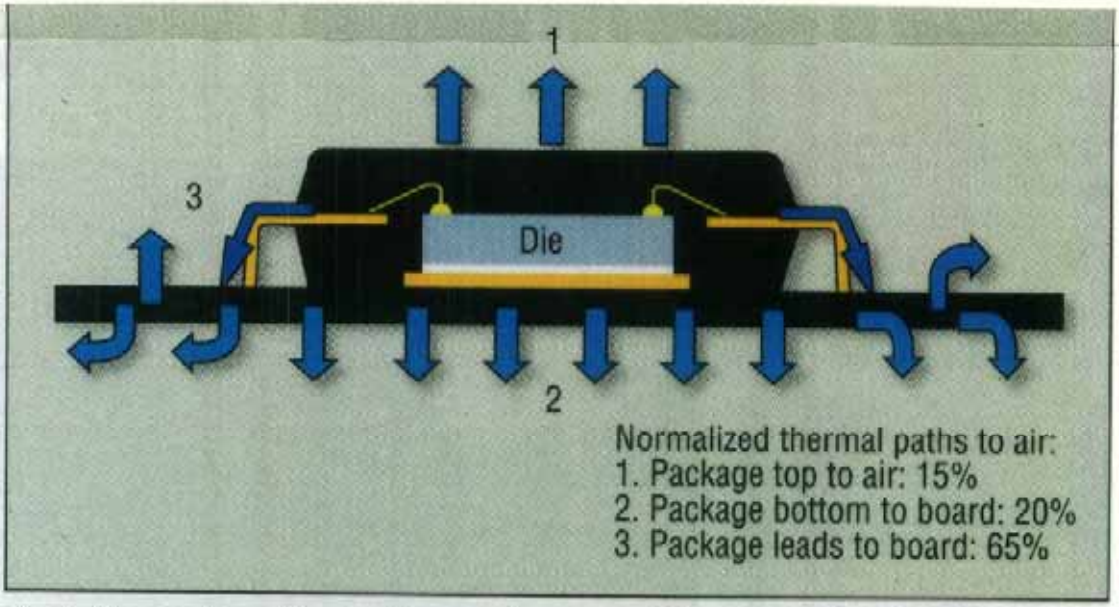


Fig. 6. *The value of θ_{JA} indicates the ease of heat flow for digital temperature sensors through the package.* Θ °C/W thermal resistance

sensor implemented in the pc board in **Fig. 4** is not affected by the heat from the main heat source and is accurately

ΔT ($T_{part} - T_{ambient}$), ΔT (part) = W(part) * Θ

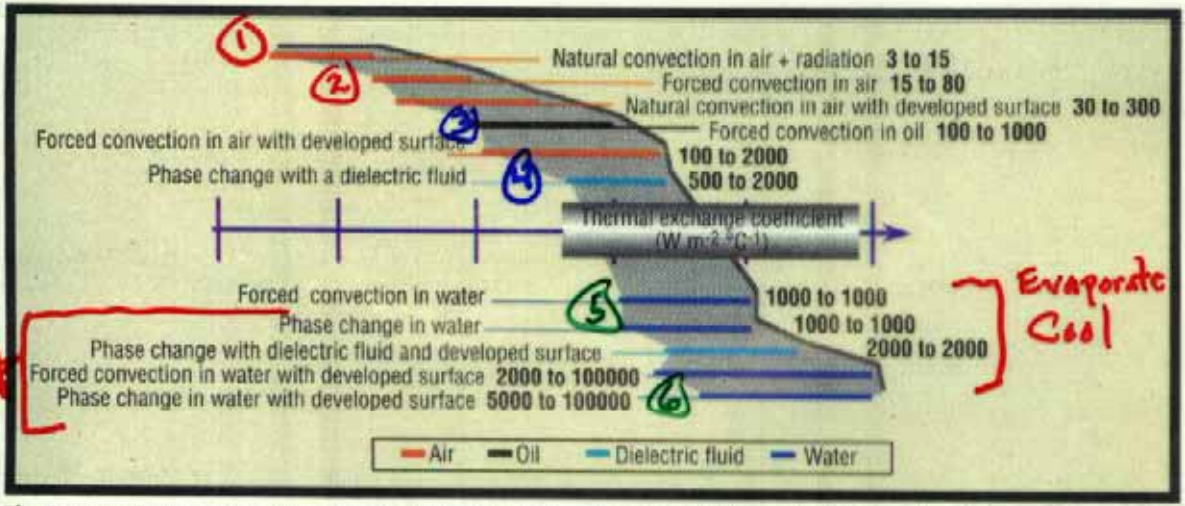


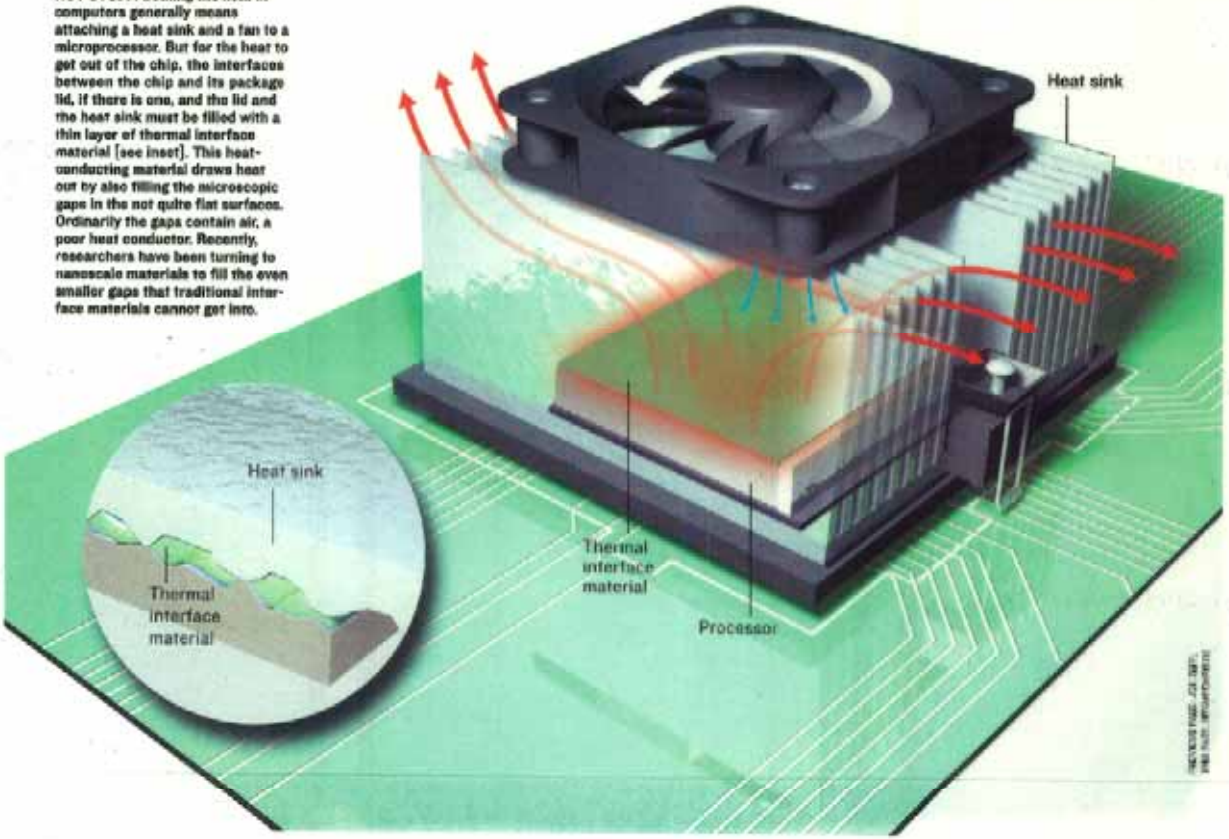
Fig. 1. *Graph depicting heat transfer properties of air, oil, dielectric fluid and water.*

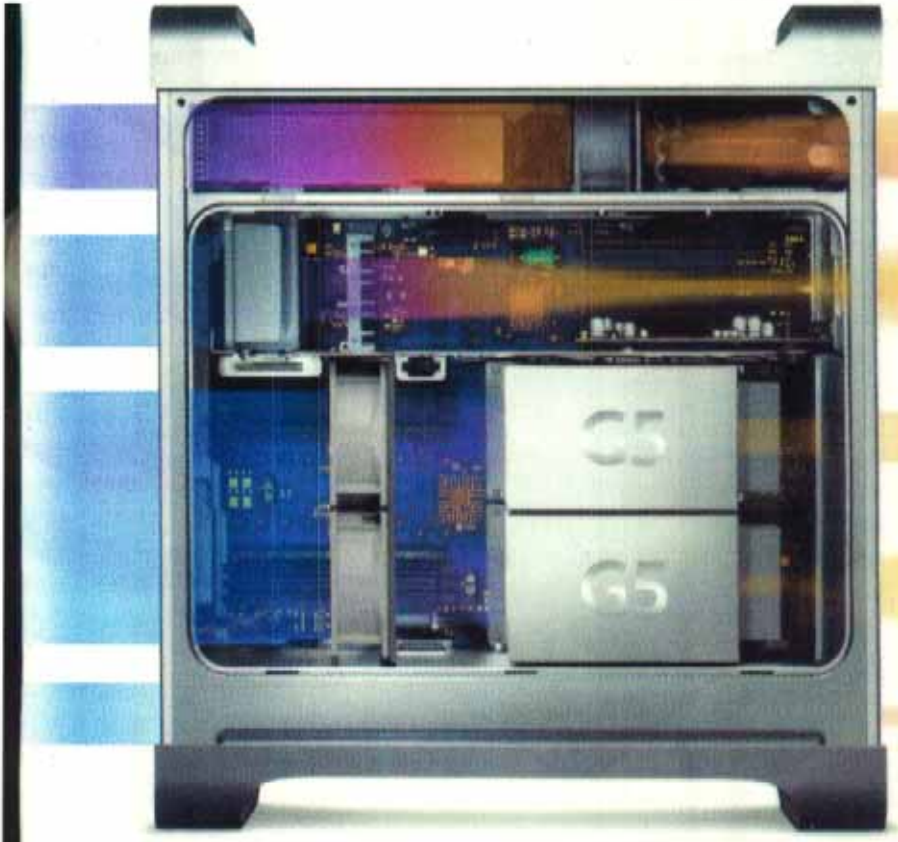
$$\Delta T \text{ in } ^\circ C = \frac{q\left(\frac{W}{cm^2}\right)}{K_{th}\left(\frac{W}{cm^2}\,^\circ C^{-1}\right)}$$

Thermal Exchange Coefficient

$K \uparrow \quad \Delta T \text{ from } T_{ambient} \downarrow$

HOT STUFF: Beating the heat in computers generally means attaching a heat sink and a fan to a microprocessor. But for the heat to get out of the chip, the interfaces between the chip and its package lid, if there is one, and the lid and the heat sink must be filled with a thin layer of thermal interface material [see inset]. This heat-conducting material draws heat out by also filling the microscopic gaps in the not quite flat surfaces. Ordinarily the gaps contain air, a poor heat conductor. Recently, researchers have been turning to nanoscale materials to fill the even smaller gaps that traditional interface materials cannot get into.





WIND TUNNEL: The Apple Power Mac G5 uses nine fans in four individually controlled zones [above, cool air in blue, hot in red] to keep the computer cool enough to operate. Twenty-one temperature sensors provide feedback to control the fans.

Photo 1. *Brazed cold plate used in a bolt-in design and a brazed cold plate for a press-pack semiconductor assembly.*

Problem ΔT Variations
cause expansion / contraction

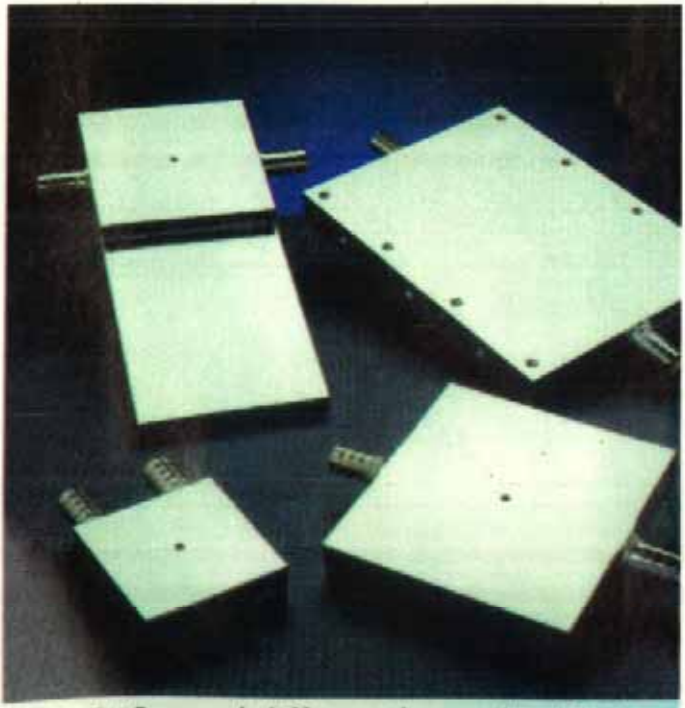


Photo 2. *Several different brazed cold plate designs.*

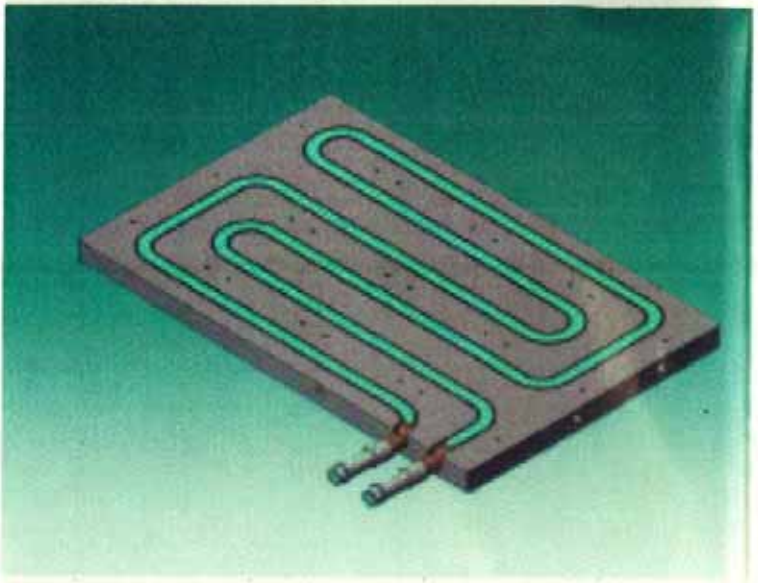


Fig. 2. *Typical copper tube embedded in aluminum plate heatsink design.*

Expanded Copper Tube in Aluminum Plate

H_2O Cooling causes
LARGE $\alpha_T \Delta T$ stress
α_T is thermal expansion coeff

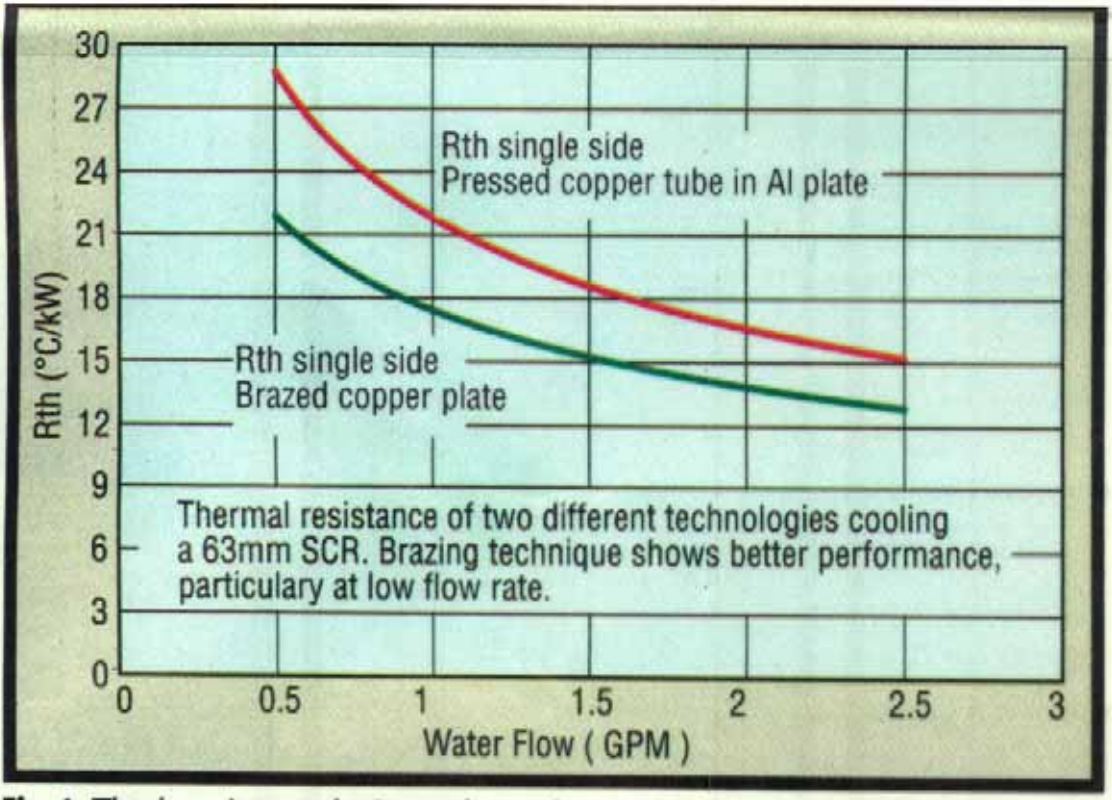


Fig. 4. *The brazing technique shows better performance than the pressed copper tube in aluminum plate technique, as you can see in*

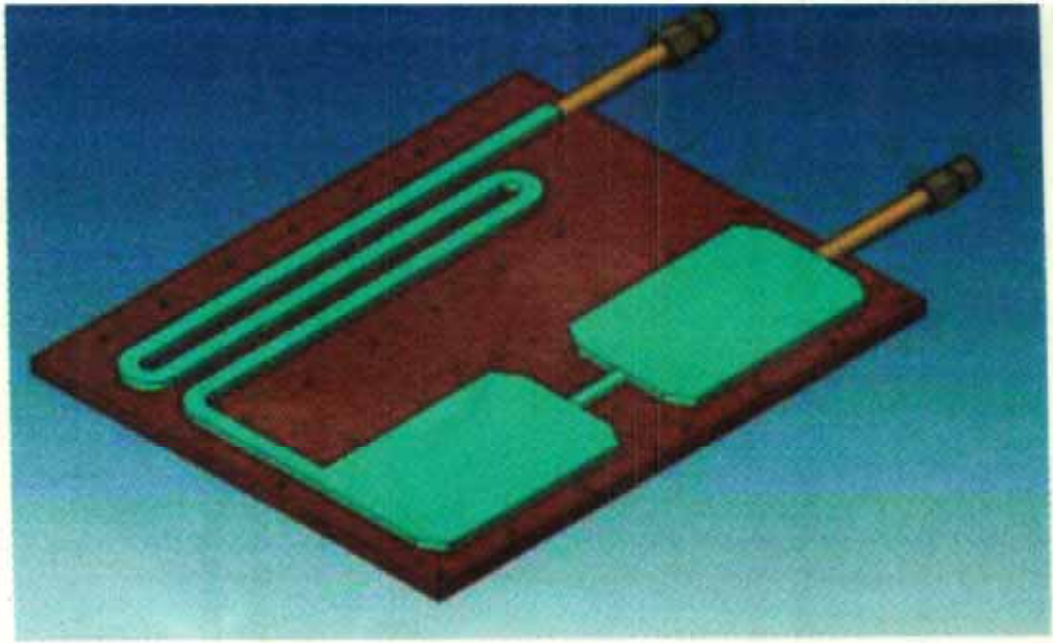
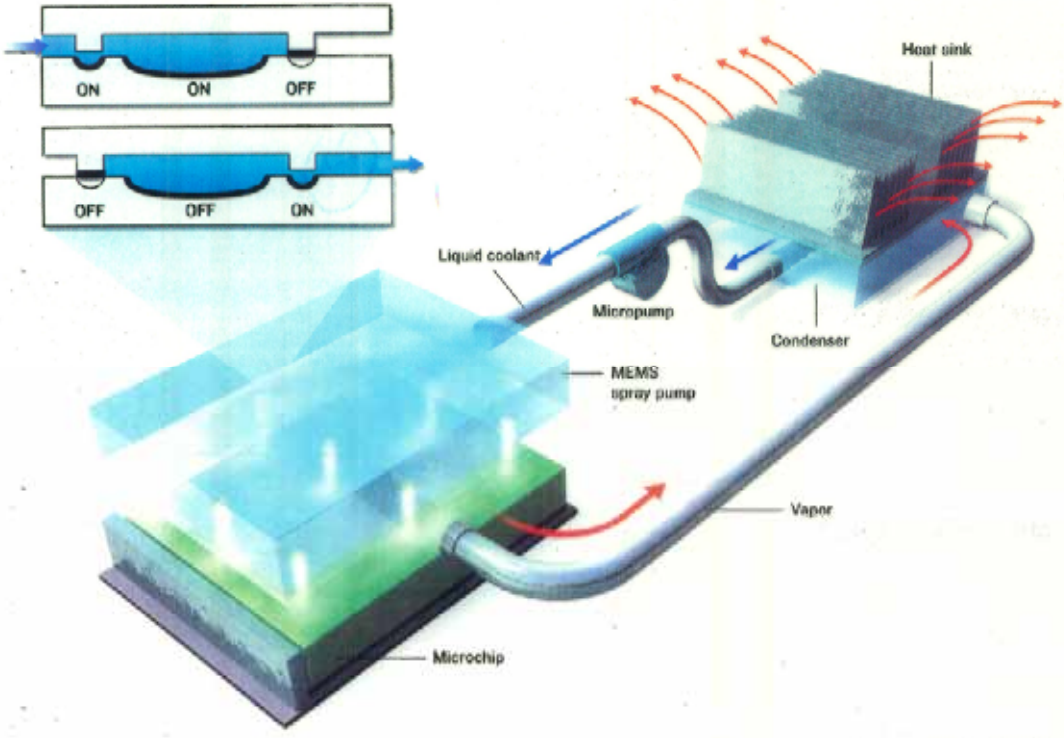
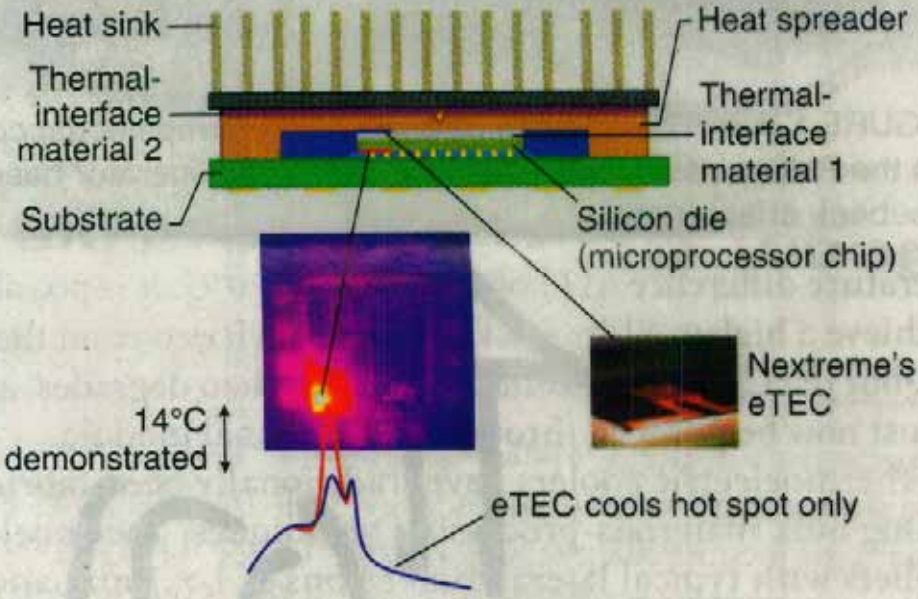


Fig. 3. *Brazed cold plate heatsink design; liquid path geometry detailed.*

cold plate technique is similar to that of bolted cold plate designs, with the



CHIP-SCALE SQUIRT GUN: A device being developed at Carnegie Mellon University cools a hot chip by spraying a dielectric fluid onto it through a MEMS spray pump (bottom left). The fluid evaporates, carrying away the chip's heat. The vapor flows to a heat sink and condenser (top right), which expels the heat and turns the vapor back into a liquid. A micropump then pumps the liquid back to the nozzles.



Nextreme's thin-film thermoelectric cooler, eTEC, cools a hot spot on a semiconductor chip. This particular implementation is for a silicon microprocessor. (*Courtesy of Nextreme*)

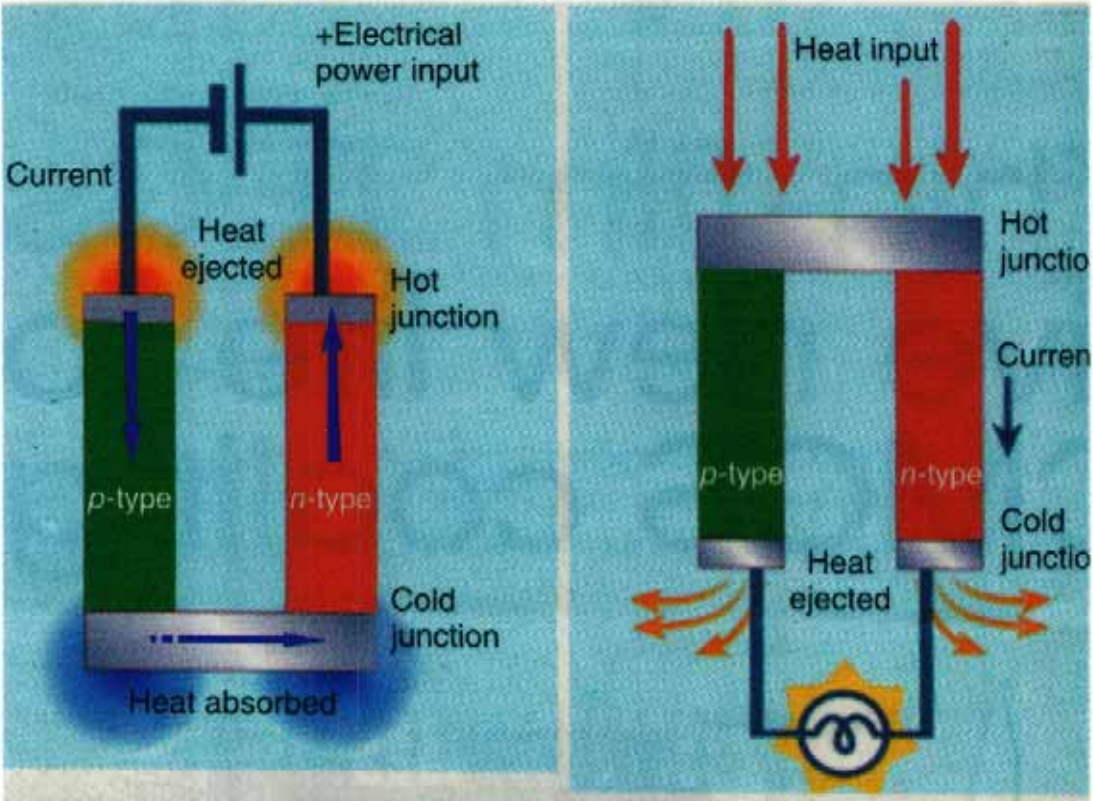


FIGURE 1. A *p-n* couple can be used as a thermoelectric couple based on the Peltier effect (left) or a thermoelectric generator based on the Seebeck effect (right)

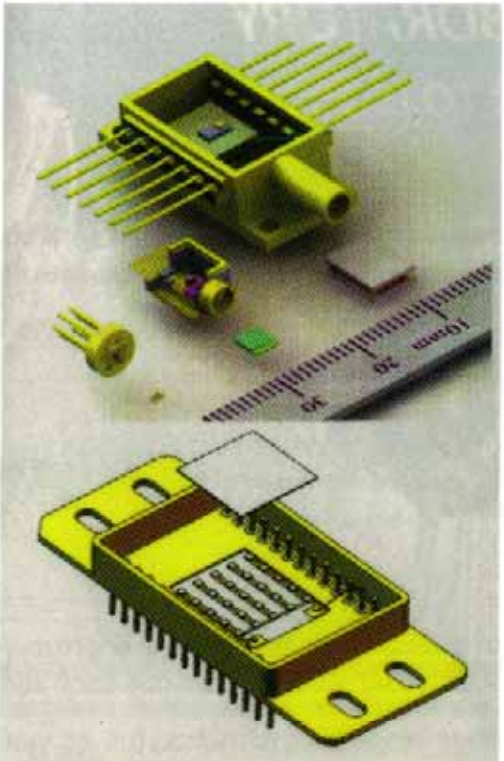
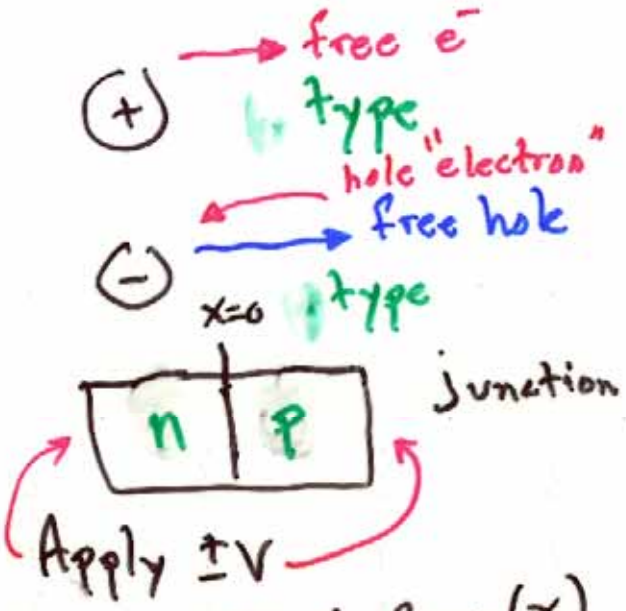


FIGURE 2. A thin-film TEC can cool many types of optoelectronic devices (top). Implemented in a CMOS optical sensor, it takes the form of an array of individual TEC *p-n* couples (bottom). The *p-n* couples are electrically in series and thermally in parallel

Semiconductor Charges

Fixed immobile at lattice sites

Mobile Free Carriers



Reverse Bias

$x=0$

depletion region $\propto$ d(V) increases with V (reverse bias)

$$\nabla \cdot E = \rho_{net} = \frac{dE}{dx}$$

$$E = -\rho_{net}(x)$$

$$V \propto -\rho_{max}(x^2)$$

V (breakdown) limits V_{max}

Doping levels ↑ V_{max} ↓

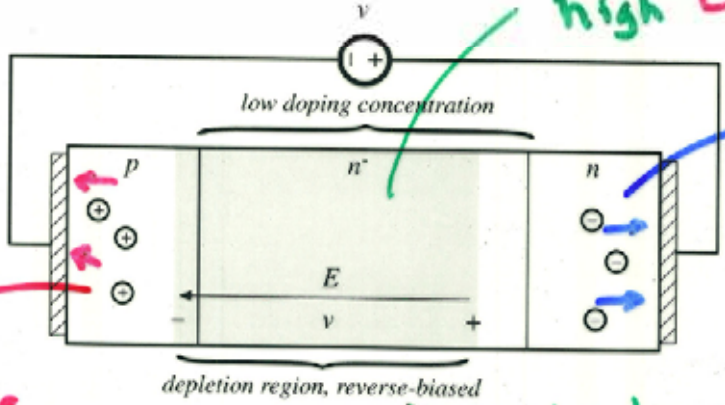
want V_{off} (max) ↑ vs R_{ON} ↓ V_{ON} ↓ want min

4.2.1. Power diodes

PIN structure to increase V (breakdown)

A power diode, under reverse-biased conditions:

intrinsic doping high E (breakdown)



e⁻ dominate go to ⊕ plate

holes dominate go to ⊖ plate

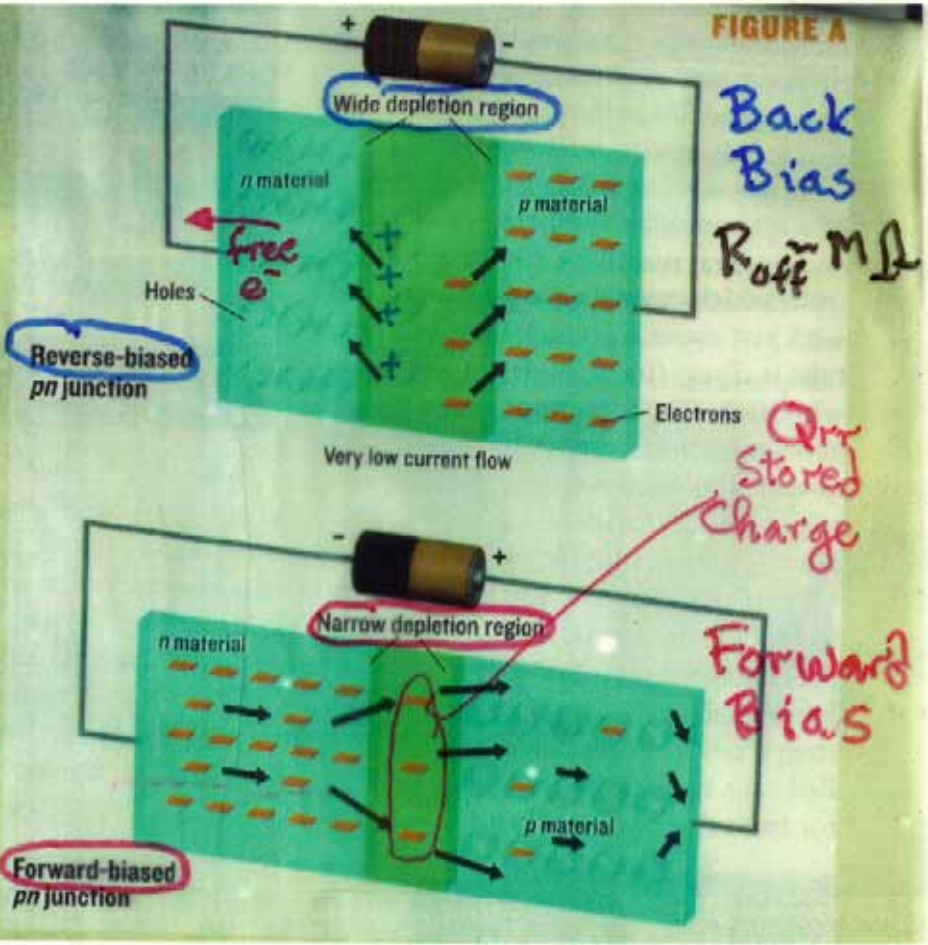
region barren of carriers

lously
g one
The
ıs, a
e it is.
urrent
ansis-
k of
ck

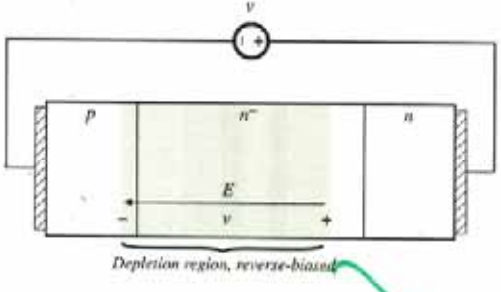
small
ıum-
ipolar

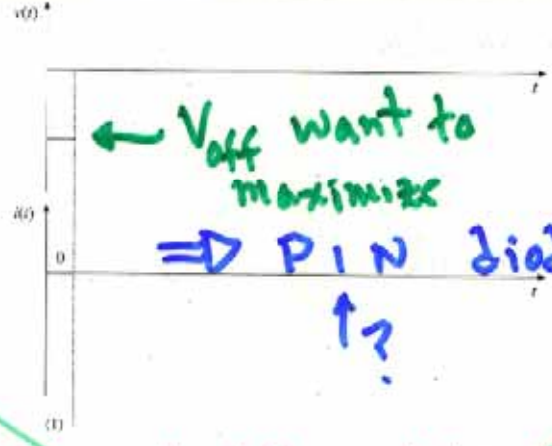
arying
r, and
o the
ation
ce,
nd the

age
o the
se-



Diode in OFF state: reversed-biased, blocking voltage





← V_{off} want to maximize

⇒ PIN diode

↑?

- Diode is reverse-biased
- No stored minority charge: $q = 0$
- Depletion region blocks applied reverse voltage; charge is stored in capacitance of depletion region

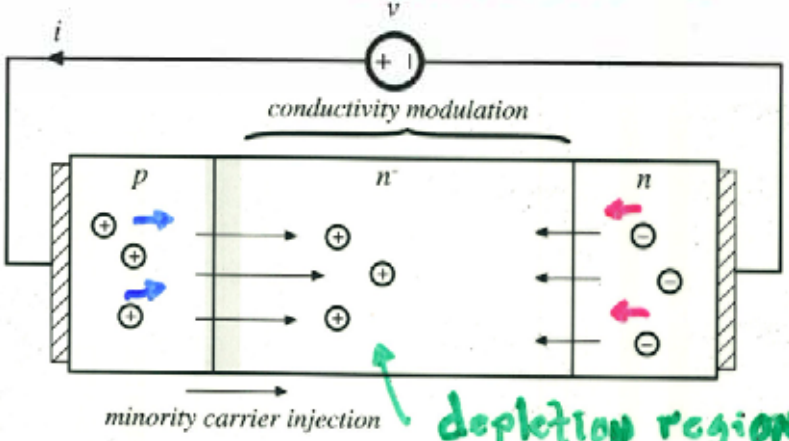
depletion region size EXPANDS with reverse bias

Tradeoffs with Doping Levels

Forward-biased power diode

Want R_{ON}, V_{ON} low } vs high V_{BK}

Arr low

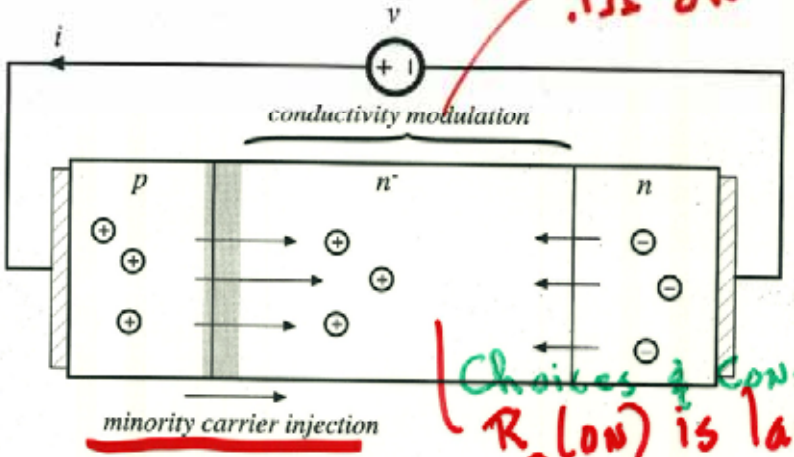


depletion region size SHRINKS with forward bias

i = ?

PIN Diode

Forward-biased power diode



Want MΩ off .1Ω on

hard to pick |N|

Choices & Consequences!

R_D(on) is larger for PIN

But ? is higher structure

Charge-controlled behavior of the diode

The diode equation:

$$q(t) = Q_0\left(e^{\lambda v(t)} - 1\right)$$

Charge control equation:

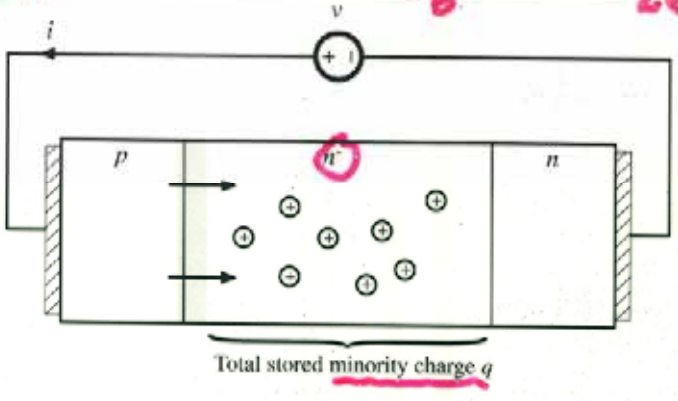
$$\frac{dq(t)}{dt} = i(t) - \frac{q(t)}{\tau_L}$$

With:

λ= 1/(26 mV) at 300 K

τ_L = minority carrier lifetime

(above equations don't include current that charges depletion region capacitance)



In equilibrium: $dq/dt = 0$, and hence

$$i(t) = \frac{q(t)}{\tau_L} = \frac{Q_0}{\tau_L}\left(e^{\lambda v(t)} - 1\right) = I_0\left(e^{\lambda v(t)} - 1\right)$$

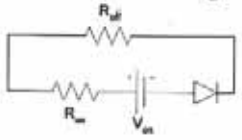
exponential

ON: R_{ON} / V_{ON} Model

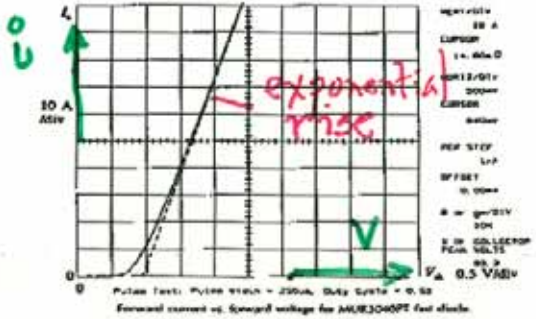
DC Parameters from I-V curve tracer

Static models of diodes involve the following:

R_{ON} ↓ as doping ↑



For HW #4 from the MUR3040PT diode data book for practice obtain all three values: R_{on} = 0.015, R_{off} = 40 MΩ, and V_{on} = 0.94 V.



Forward current vs. forward voltage for MUR3040PT fast diode.

Static characteristics do not tell the full story of any device. Like people the dynamic characteristics may reveal new and unexpected behavior. For example, the V_{on} for the diode above does have a brief voltage overshoot when driven by a constant current source to turn it on. This needs to be accounted for in any dynamic model of diode operation as the dynamic I-V is unique.

$R_{ON} = \frac{\Delta V}{\Delta I}$ typically 10 mΩ

$V_{ON} = V_{th} - I_1 R_{ON}$ typically 1-2 V

Paralleling diodes

Attempts to parallel diodes, and share the current so that $i_1 = i_2 = i/2$, generally don't work.

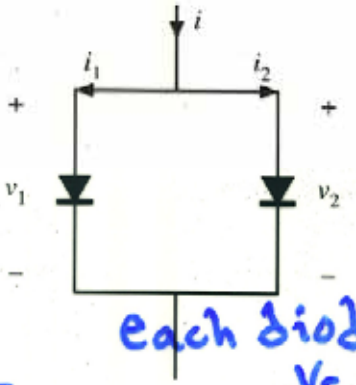
Reason: thermal instability caused by temperature dependence of the diode equation.

Increased temperature leads to increased current, or reduced voltage.

One diode will hog the current.

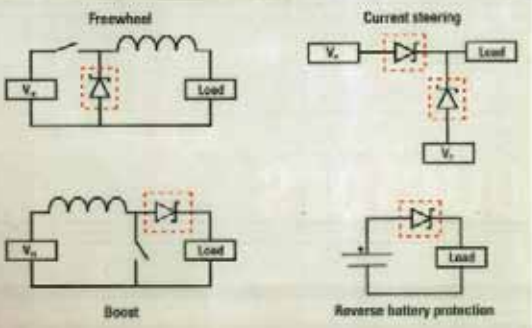
To get the diodes to share the current, heroic measures are required:

- Select matched devices
- Package on common thermal substrate
- Build external circuitry that forces the currents to balance



each diode
$i \sim e^{v_F}$

Diode and Circuit Determine diode "Choices"



Part Number	$I_{F(AV)}$	V_{RRM}	V_F max @25°C	I_R max @25°C	T_J Range
IR0530CSPTR	0.5A	30V	0.33V	50µA	-55 to 150°C
IR05H40CSPTR	0.5A	40V	0.42V	10µA	-55 to 150°C
IR130CSPTR	1.0A	30V	0.33V	100µA	-55 to 150°C
IR140CSPTR	1.0A	40V	0.38V	80µA	-55 to 150°C
IR1H40CSPTR	1.0A	40V	0.42V	10µA	-55 to 150°C

Characteristics of several commercial power rectifier diodes

Part number	*Rated max voltage*	*Rated avg current*	V_F *(typical)*	t_r *(max)*
Fast recovery rectifiers				
1N3913	400V	30A	1.1V	400ns
SD453N25S20PC	2500V	400A	2.2V	2*μs*
Ultra-fast recovery rectifiers				
MUR815	150V	8A	0.975V	35ns
MUR1560	600V	15A	1.2V	60ns
RHRU100120	1200V	100A	2.6V	60ns
Schottky rectifiers				
MBR6030L	30V	60A	0.48V	
444CNQ045	45V	440A	0.69V	
30CPQ150	150V	30A	1.19V	


High Voltage
Diodes
1 kV to 300 kV
Fast Recovery down to 35nS
Average Forward Current up to 10 Amps
HVCA diodes are ideal for use in high voltage power supplies and multipliers found in medical equipment and instrumentation. They are also well-suited for aerospace, military, automotive, down hole and high temperature applications and X-ray equipment used for medical, dental, industrial and security purposes.
HVCA
P.O. Box 848, Farmington, NJ 07727
(732) 938-4499 ■ (732) 938-4451 FAX
e-mail: info@hvca.com ■ www.hvca.com

Types of power diodes

Standard recovery $\tau = 100\mu s$

Reverse recovery time not specified, intended for 50/60Hz

Fast recovery and ultra-fast recovery $\tau \sim \leq 10\mu s$

Reverse recovery time and recovered charge specified

Intended for converter applications

Schottky diode $\tau \sim 10\ ns$

A majority carrier device

Essentially no recovered charge

Model with equilibrium i-v characteristic, in parallel with depletion region capacitance

Restricted to low voltage (few devices can block 100V or more)

As t_{rr} goes so goes E_{loss} (Joules)

Types of power diodes

$T_{cycle}/2 = 8\text{–}10\,ms$

Standard recovery Mains Electronics

- Reverse recovery time not specified, intended for 50/60Hz

must be $t_r < ms$

Fast recovery and ultra-fast recovery $f_{sw} < 200kHz$

- Reverse recovery time and recovered charge specified
- Intended for converter applications

$T/2 = 2.5\mu s$ $t_r < \mu s$

Schottky diode any i_{rr} ? 0

- A majority carrier device
- Essentially no recovered charge
- Model with equilibrium i-v characteristic, in parallel with depletion region capacitance
- Restricted to low voltage (few devices can block 100V or more)

$f_{sw} \to MHz$ $T/2 \to 500ns$ $t_r = 10ns$ (100)

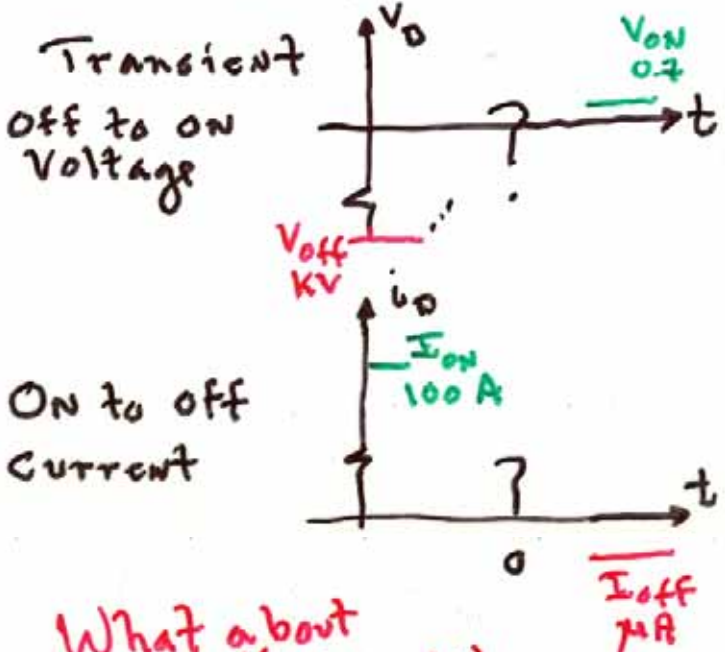
Charge-control in the diode: Discussion

- The familiar *i–v* curve of the diode is an equilibrium relationship that can be violated during transient conditions
- During the turn-on and turn-off switching transients, the current deviates substantially from the equilibrium *i–v* curve, because of change in the stored charge and change in the charge within the reverse-bias depletion region
- Under forward-biased conditions, the stored minority charge causes "conductivity modulation" of the resistance of the lightly-doped n^- region, reducing the device on-resistance

PIN Diode Dynamics

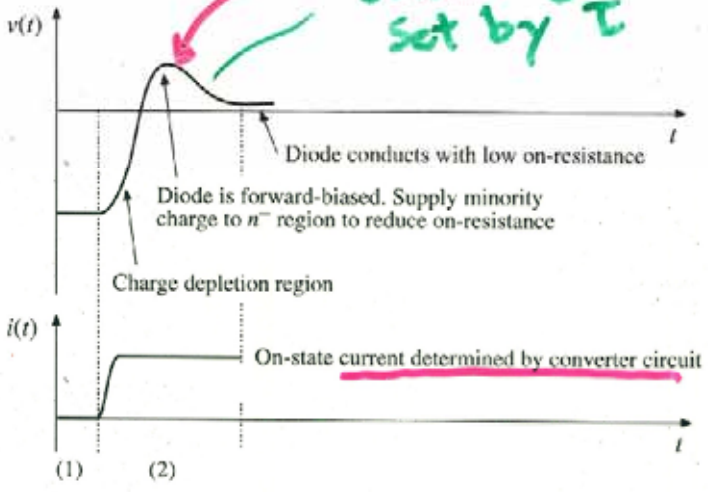
$V_{ON} \geq 0.7\ V$

DC $I_{off} \sim \mu A$



What about
ON - off
off - ON
} $V_D(t)$
$i_D(t)$

Turn-on transient

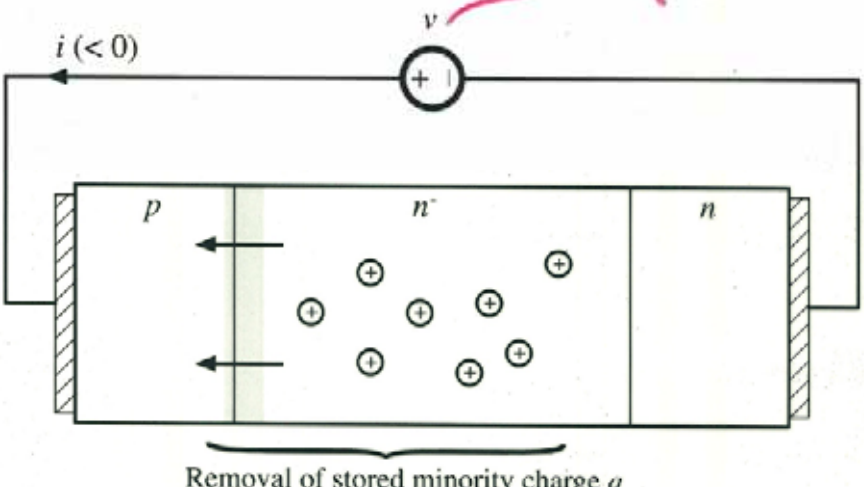


The current $i(t)$ is determined by the converter circuit. This current supplies:

- charge to increase voltage across depletion region
- charge needed to support the on-state current
- charge to reduce on-resistance of n^- region

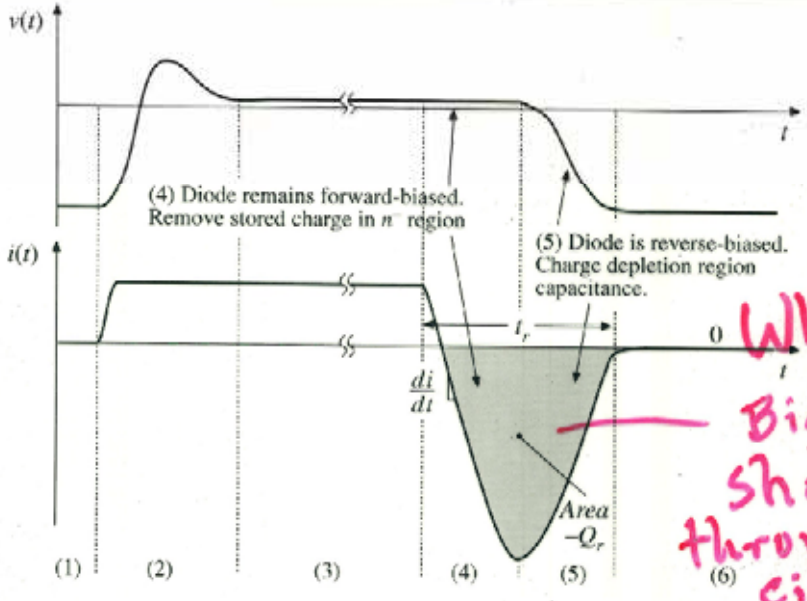
Turn-off transient

flip polarity



Q_{rr}

Diode turn-off transient
continued

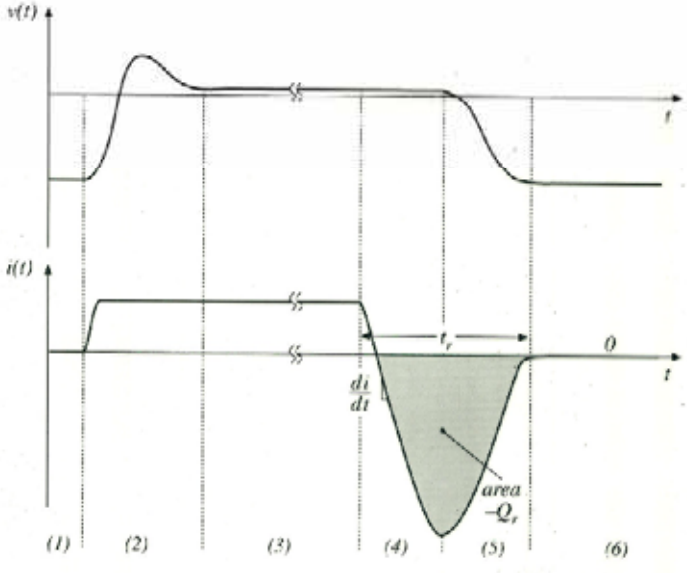


Whoa!

Big Shoot through in circuit

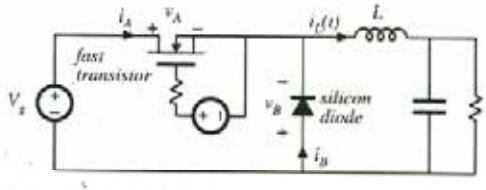
All together

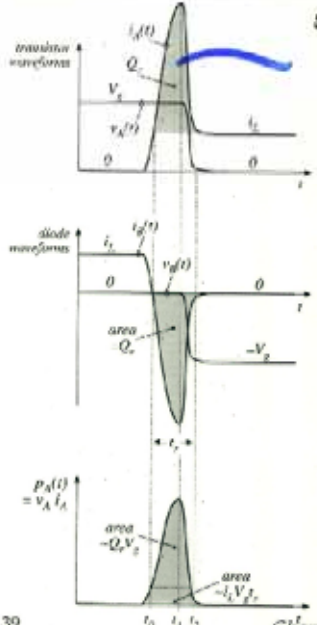
Typical diode switching waveforms



Diode Q_r increases T_R loss off-on

The diode switching transients induce switching loss in the transistor





see Section 4.3.2

brief shoot through for I_{DS}

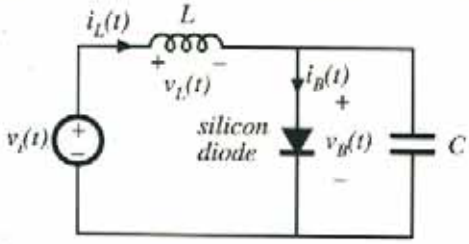
Peak I_D during V_{off}

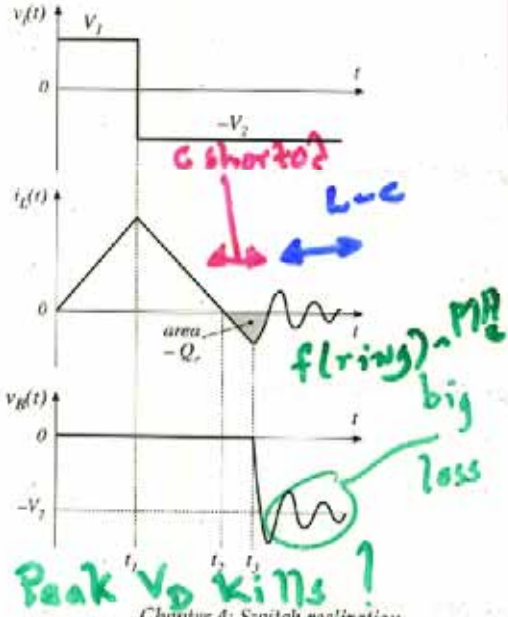
- Diode recovered stored charge Q_r flows through transistor during transistor turn-on transition, inducing switching loss
- Q_r depends on diode on-state forward current, and on the rate-of-change of diode current during diode turn-off transition

V_{peak} for oh no see
I_{peak}

Ringing induced by diode stored charge

see Section 4.3.3





- Diode is forward-biased while $i_L(t) > 0$
- Negative inductor current removes diode stored charge Q_r
- When diode becomes reverse-biased, negative inductor current flows through capacitor C.
- Ringing of L-C network is damped by parasitic losses. Ringing energy is lost.

High Q ring Peaks ≈ 5 steady state

Energy associated with ringing

Recovered charge is $Q_r = -\int_{t_2}^{t_3} i_L(t)\, dt$

Energy stored in inductor during interval $t_2 \le t \le t_3$:

$$W_L = \int_{t_2}^{t_3} v_L(t)\, i_L(t)\, dt$$

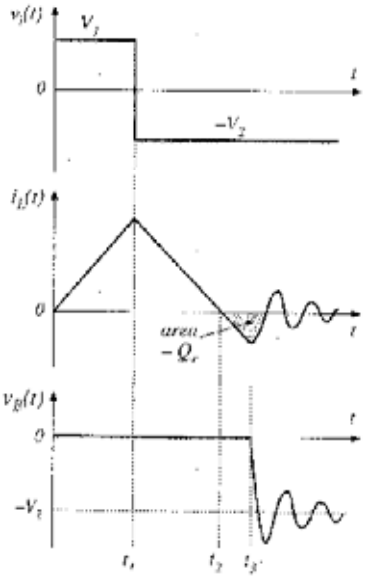
Applied inductor voltage during interval $t_2 \le t \le t_3$:

$$v_L(t) = L\, \frac{di_L(t)}{dt} = -V_2$$

Hence,

$$W_L = \int_{t_2}^{t_3} L\, \frac{di_L(t)}{dt}\, i_L(t)\, dt = \int_{t_2}^{t_3} (-V_2)\, i_L(t)\, dt$$

$$W_L = \tfrac{1}{2} L\, i_L^2(t_3) = V_2\, Q_r$$



Switching loss calculation

Energy lost in transistor:

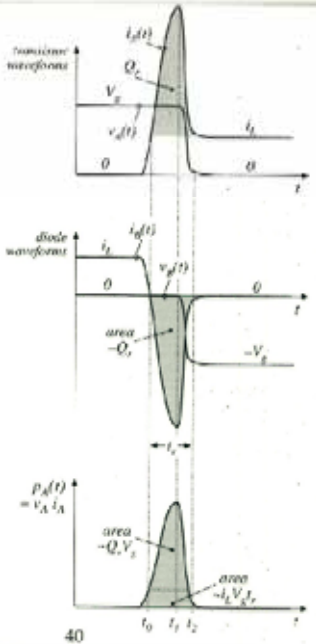
$$W_D = \int_{\substack{\text{switching} \\ \text{transition}}} v_A(t)\, i_A(t)\, dt$$

With abrupt-recovery diode:

$$W_D \approx \int_{\substack{\text{switching} \\ \text{transition}}} V_g\, (i_L - i_B(t))\, dt$$

$$= V_g\, i_L\, t_r + V_g\, Q_r$$

- *Often, this is the largest component of switching loss*



Soft-recovery diode:

$(t_2 - t_1) >> (t_1 - t_0)$

Abrupt-recovery diode:

$(t_2 - t_1) << (t_1 - t_0)$

Table 4.1 p177

Characteristics of several commercial power rectifier diodes

High f Rectifier @ f_{sw}

Part number	Rated max voltage	Rated avg current	V_F (typical)	t_r (max)
Fast recovery rectifiers				
1N3913	400V	30A	1.1V	400ns
SD453N25S20PC	2500V	400A	2.2V	2μs
Ultra-fast recovery rectifiers				
MUR815	150V	8A	0.975V	35ns
MUR1560	600V	15A	1.2V	60ns
RHRU100120	1200V	100A	2.6V	60ns
Schottky rectifiers				
MBR6030L	30V	60A	0.48V	
444CNQ045	45V	440A	0.69V	
30CPQ150	150V	30A	1.19V	

$\Delta t_{rr} =$ ions

High-Reliability Schottky Rectifiers in a Wide Range of Voltage, Current and Package Options

Package		$I_{F(max)}$	V_R
	TO-257	16A	30V to 150V
	D2	16A	30V to 150V
	SMD-0.5	30A	30V to 150V
	TO-254	35A	30V to 150V
	D3	35A	30V to 150V
	SMD-1	120A	30V to 150V

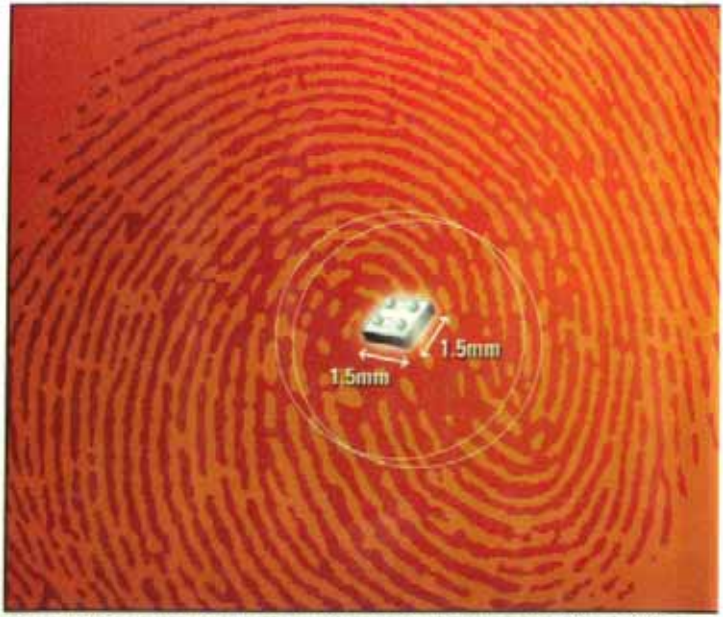
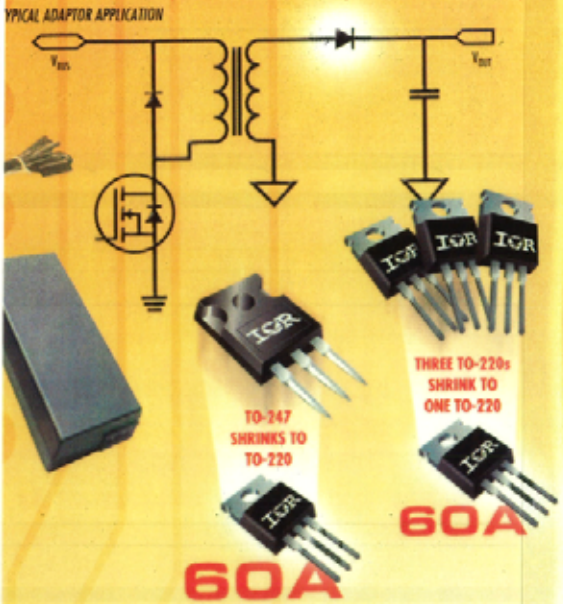


Fig. 4. *With its 1.5-mm x 1.5-mm footprint, International Rectifier's IR140CSP 1-A Schottky diode, shown here superimposed on a fingerprint, is nearly seven times smaller than the first surface-mount, 1-A Schottky introduced in the late 1980s.*

New Schottky Diodes Double Current Densit

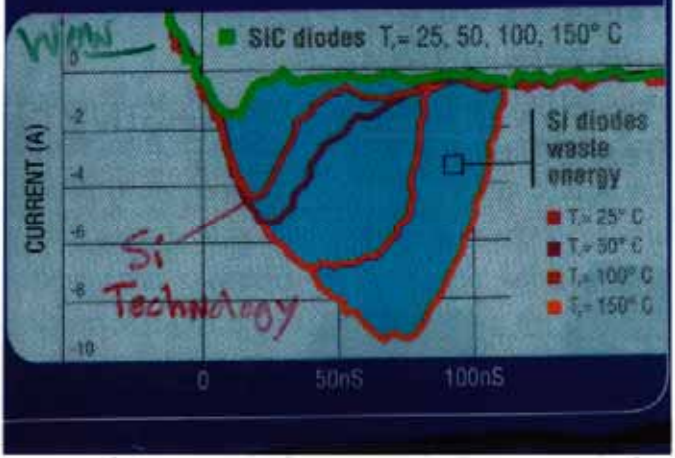


SPECIFICATIONS

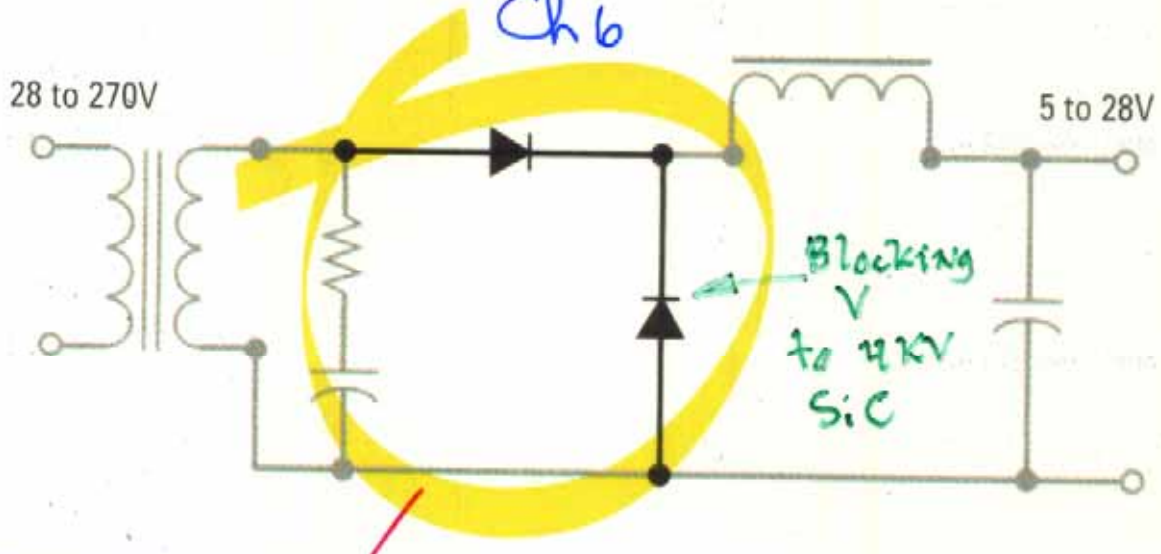
Part Number	I_F Max (A)	V_F @25°C (V)	V_F @125°C (V)	Package Options
10CTQ150/S/-1	10	0.93 @ 5A	0.73 @ 5A	TO-220/D²Pak/TO-262
20CTQ150/S/-1/FP	20	0.83 @ 10A	0.66 @ 10A	TO-220/D²Pak/TO-262/TO-220FP
30CPQ150	30	1.0 @ 15A	0.78 @ 15A	TO-247
40CTQ150/S/-1/FP	40	0.93 @ 20A	0.71 @ 20A	TO-220/D²Pak/TO-262/TO-220FP
60CTQ150	60	0.88 @ 30A	0.72 @ 30A	TO-220
60CPQ150	60	0.83 @ 30A	0.67 @ 30A	TO-247
80CPQ150	80	0.86 @40A	0.71 @ 40A	TO-247

SiC. THE MATERIAL OF CHOICE.

- *ZERO RECOVERY*® Rectifier
- Higher frequency operation
- No high frequency ringing
- Lower switching loss
- Lower noise
- Cooler operating temperature
- Higher power density



Forward Converter Output Filter



Schottky diode enables f_{sw}↑ yet Sw loss ↓

① Smaller L, C ② Less heatsinks fans

Table 1. Monocrystalline SiC polytypes compared to GaAs and silicon.

Properties	4H-SiC	6H-SiC	3C-SiC	GaAs	Si	GaN
Bandgap (eV)	3.26	3.03	2.2	1.43	1.12	3.5
Breakdown electric field [V/cm (at 1kV)]	2.2×10^6	2.4×10^6	2×10^6	3×10^5	2.5×10^5	
Thermal conductivity (W/cm.K)	4.9	4.9	4.9	0.5	1.5	1.3
Saturated electron drift velocity [cm/s]	2.7×10^7	2.0×10^7	2.7×10^7	1.0×10^7	1.0×10^7	2.5×10^7

3-5 x higher $\sigma_{Thermal}$

BV is 10x (BV) Si GaAs

Transistor: Trans Resistor Concept

One reversed pn junction

High V
low i ⇒ High R_{out}

One forward biased pn junction

Low V
High i ⇒ low R_{in}

cb junction reverse biased wide spatially

be junction forward bias thin spatially

Requires two bias voltages

i_c @ MΩ
i_e @ mΩ
} i same ⇒ Trans resistance

diode
Base-emitter on

diode
Collector-Base off

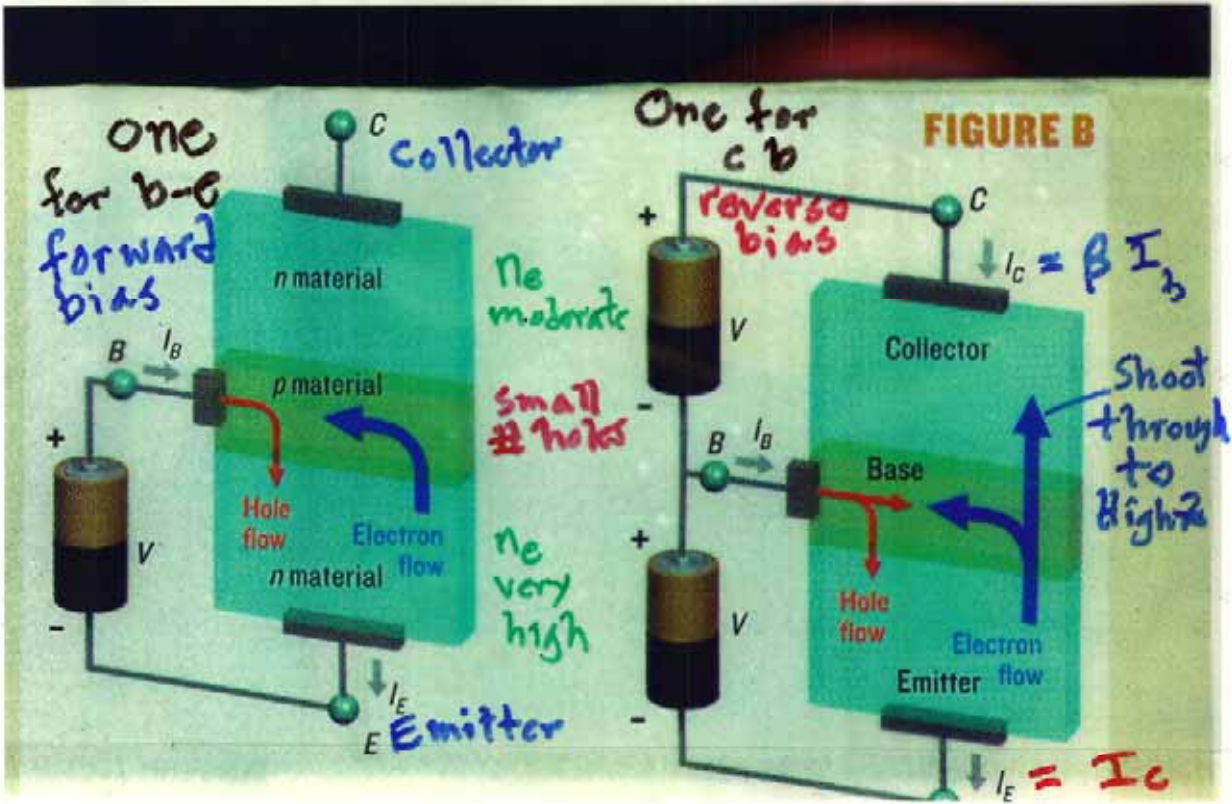
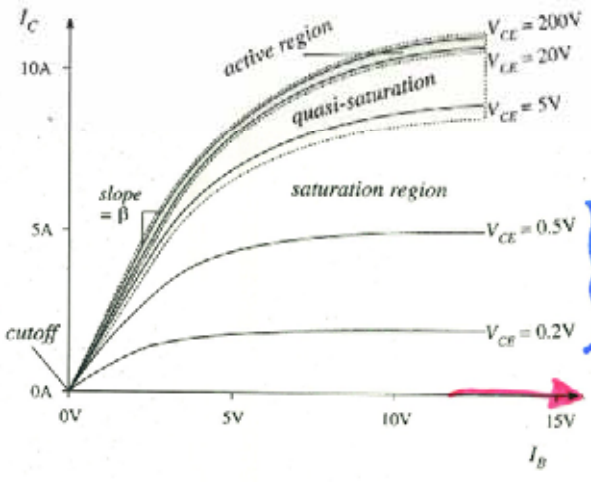


FIGURE B

BJT characteristics

$\beta = \frac{\Delta i_c}{\Delta i_b}$



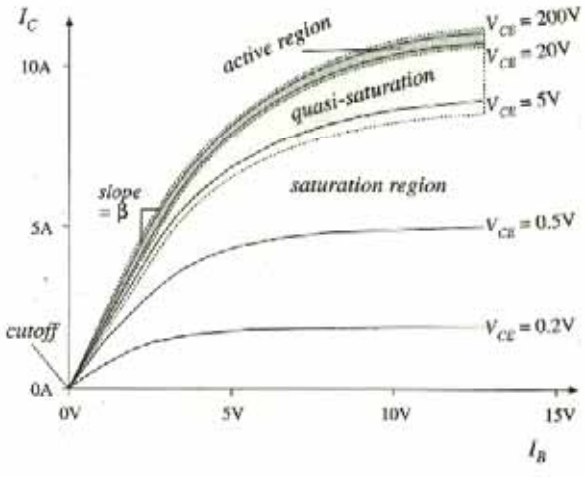
- Off state: $I_B = 0$
- On state: $I_B > I_C/\beta$
- Current gain β decreases rapidly at high current. Device should not be operated at instantaneous currents exceeding the rated value

low V_{CE}

V_{cb}

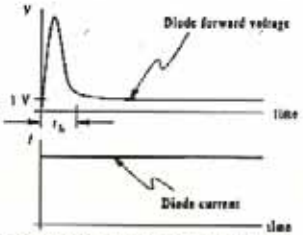
Fig 4.35 p 85

BJT characteristics



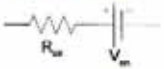
- Off state: $I_B = 0$
- On state: $I_B > I_C / \beta$
- Current gain β decreases rapidly at high current. Device should not be operated at instantaneous currents exceeding the rated value

oh NO Sec!

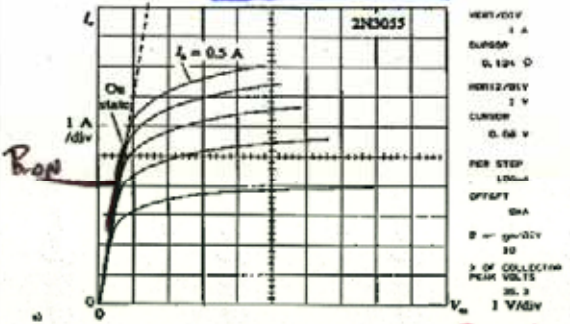


Forward recovery characteristic of a diode.

A static npn bipolar transistor model should involve the following two values:



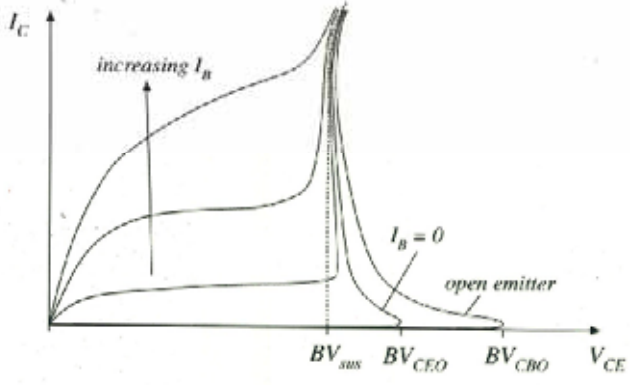
For HW #4 from the measured transistor characteristics below for practice obtain: R_{on} = 134 mΩ and V_{on} = 0.08 V.



$V_{ON} \approx V - IR_{ON}$ @ 3A $V_{ON} = .1V$

Breakdown voltages

Avalanch Effect ≈ 1ns



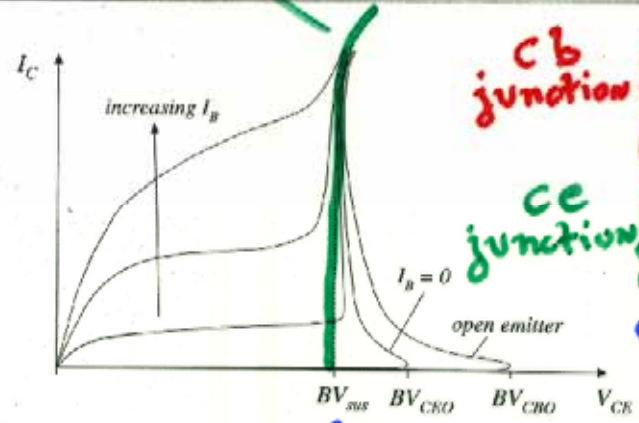
BV_{CBO}: avalanche breakdown voltage of base-collector junction, with the emitter open-circuited

BV_{CEO}: collector-emitter breakdown voltage with zero base current

BV_{sus}: breakdown voltage observed with positive base current

In most applications, the off-state transistor voltage must not exceed BV_{CEO}.

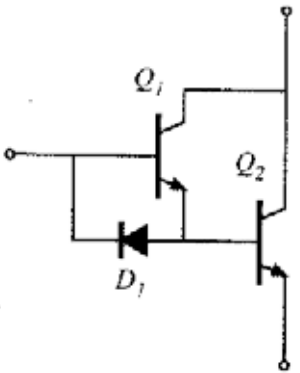
Breakdown voltages:



- BV_{CBO}: avalanche breakdown voltage of base-collector junction, with the emitter open-circuited
- BV_{CEO}: collector-emitter breakdown voltage with zero base current
- BV_{sus}: breakdown voltage observed with positive base current

In most applications, the off-state transistor voltage must not exceed BV_{CEO}.

Darlington-connected BJT

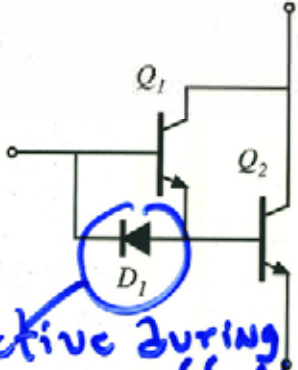


- Increased current gain, for high-voltage applications
- In a monolithic Darlington device, transistors Q_1 and Q_2 are integrated on the same silicon wafer
- Diode D_1 speeds up the turn-off process, by allowing the base driver to actively remove the stored charge of both Q_1 and Q_2 during the turn-off transition

Fig 4.36 p 86

Darlington-connected BJT

$\beta_{eff} = \beta_1 \beta_2 \Rightarrow$ $I_{B(in)} = I_C / \beta_1 \beta_2$

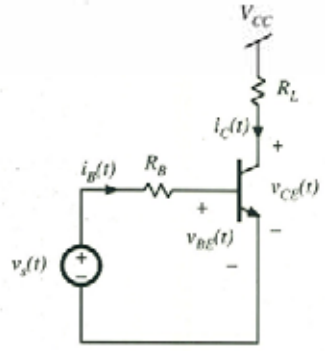


- Increased current gain, for high-voltage applications
- In a monolithic Darlington device, transistors Q_1 and Q_2 are integrated on the same silicon wafer
- Diode D_1 speeds up the turn-off process, by allowing the base driver to actively remove the stored charge of both Q_1 and Q_2 during the turn-off transition

only active during turn-off: $V_{IN}\ominus$

$Q_{rr(1)}$ and $Q_{rr(2)}$

BJT switching times



V drive

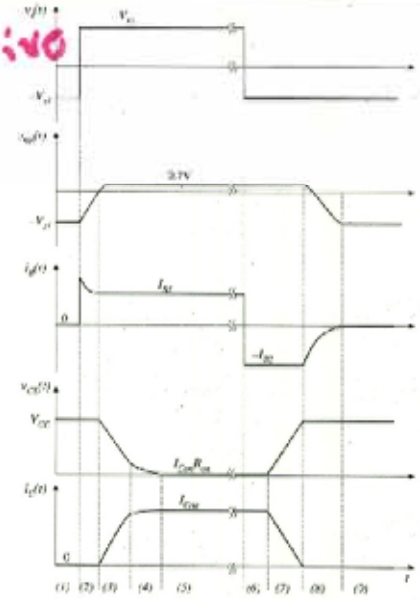


Fig 4.32 p 83

BJT switching times

? delay details? stored collector Q

need I_B to sustain I_{ON}

$\frac{I_{B1}}{C_{IN}}$

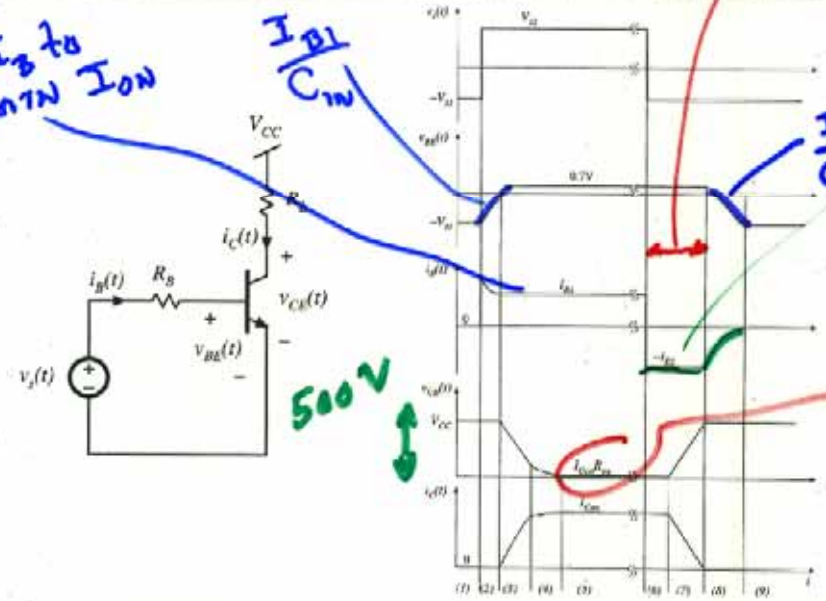
Q_{rr}

$\frac{I_{B2}}{C_{IN}}$

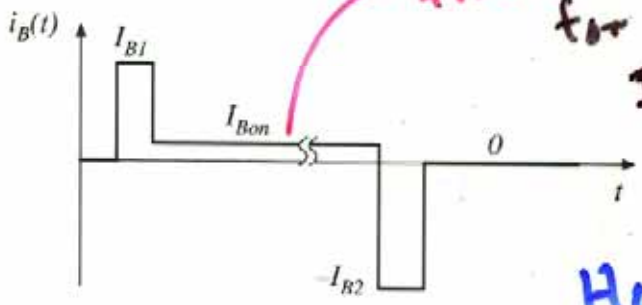
Adv. of Bipolar

(100 A)(.3V) 30W loss when ON

500 V



Ideal base current waveform



need all the time Q is on

for $\beta = 10$ or 100

$I_C = 100A$

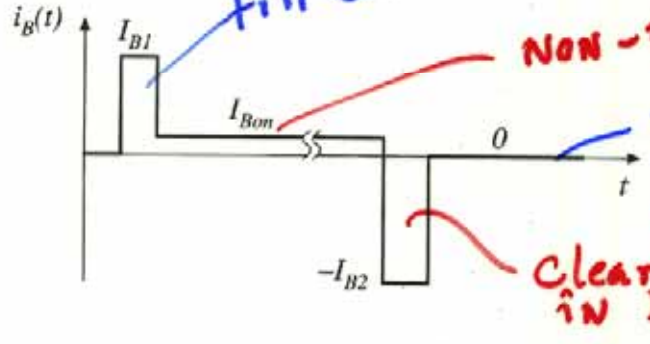
$I_B = ?$

How to reduce $I_{B(ON)}$?

Fig 4.33 p 84

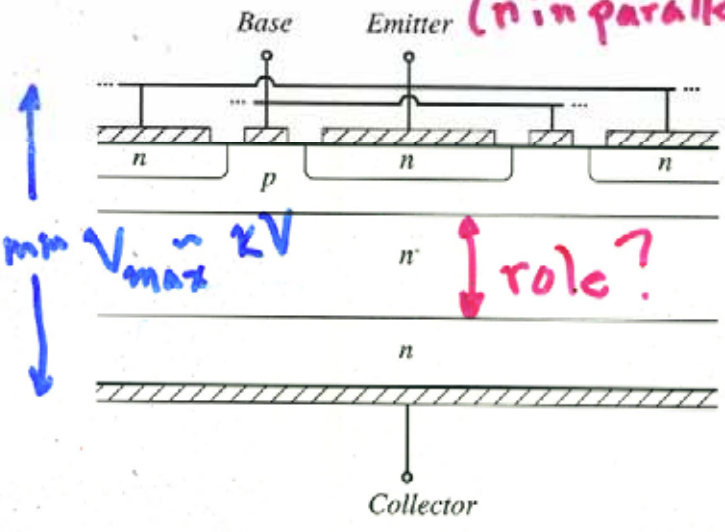
Ideal base current waveform

Base Driver must provide $i_B(t)$



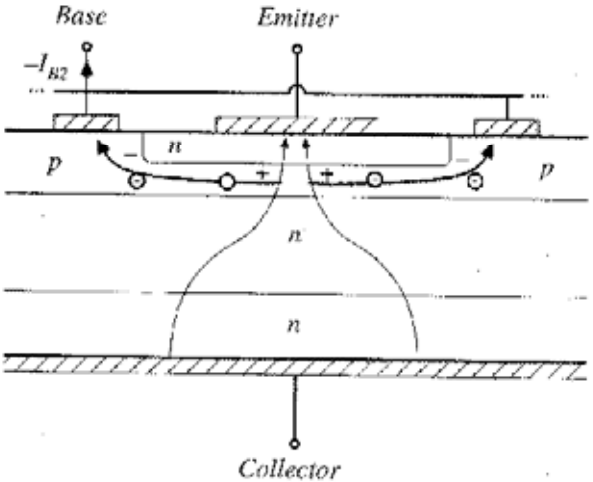
4.2.3. Bipolar Junction Transistor (BJT)

Power BJT in 1000μ layer



- Interdigitated base and emitter contacts
- Vertical current flow
- npn device is shown
- minority carrier device
- on-state: base-emitter and collector-base junctions are both forward-biased
- on-state: substantial minority charge in p and n^- regions, conductivity modulation

Current crowding due to excessive I_{B2}

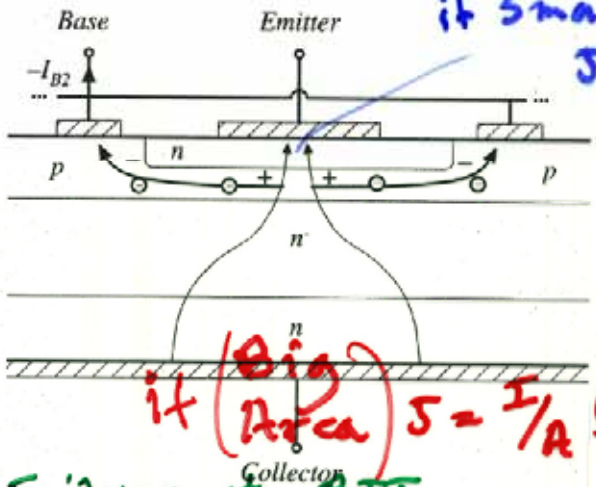


can lead to formation of hot spots and device failure

Fig 4.34

Current crowding due to excessive I_{B2}

I_{const} but $J = I/A$ ↑



if small Area

$J = \frac{I}{A}$ high

can lead to formation of hot spots and device failure

if (Big Area) $J = I/A$ low

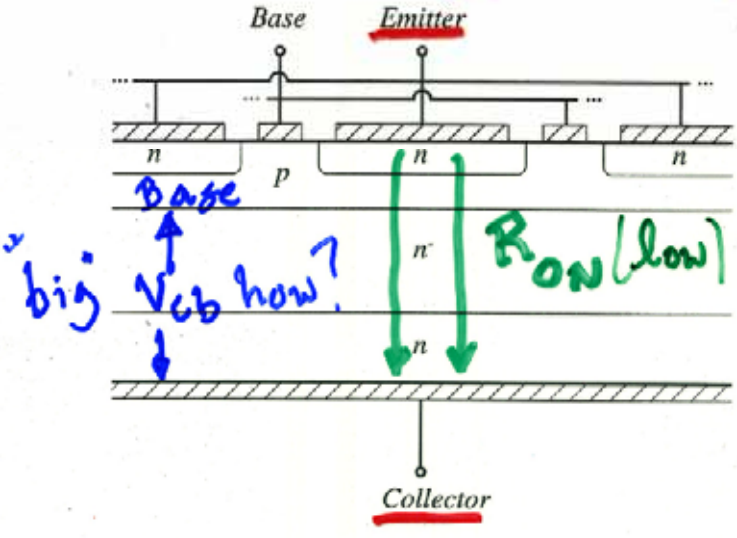
Failure of BJT

Runaway condition via hot spot area

Back in time
For s.s. switches still the lowest R_{ON}, V_{ON}

4.2.3. Bipolar Junction Transistor (BJT)

Figure 4.30 pg 82



- Interdigitated base and emitter contacts
- Vertical current flow
- npn device is shown
- minority carrier device
- on-state: base-emitter and collector-base junctions are both forward-biased
- on-state: substantial minority charge in p and n^- regions, conductivity modulation

$V_{be} = .7$
$V_{bc} = .1$
$\Rightarrow V_{cb}$?