ECE 562

Week 6 Lecture 2

Fall 2008

Week 6 Lecture 2 Summary

- Section notes
  - Slides 3-4 – Device sizes decrease over time
  - Slides 5-15 – MOSFET operation
  - Slides 16-21– MOSFET characteristics
  - Slides 22-31 – MOSFET resistance
  - Slides 32-34 – MOSFET body diodes
  - Slides 35-44 – Reducing switch losses
  - Slides 45-51 – Commercial MOSFETs
  - Slides 52-59 – MOSFET parasitics and other non-ideal behaviors
  - Slides 60-81 – Efficiency and conclusion summary


1980s
1970s
1960s


2007
1990s

To date

Summary of chapter 4

1. How an SPST ideal switch can be realized using semiconductor devices depends on the polarity of the voltage which the devices must block in the off-state, and on the polarity of the current which the devices must conduct in the on-state.
2. Single-quadrant SPST switches can be realized using a single transistor or a single diode, depending on the relative polarities of the off-state voltage and on-state current.
3. Two-quadrant SPST switches can be realized using a transistor and diode, connected in series (bidirectional-voltage) or in anti-parallel (bidirectional-current). Several four-quadrant schemes are also listed here.
4. A "synchronous rectifier" is a MOSFET connected to conduct reverse current, with gate drive control as necessary. This device can be used where a diode would otherwise be required. If a MOSFET with sufficiently low R_{on} is used, reduced conduction loss is obtained.

4.2. A brief survey of power semiconductor devices

- Power diodes
- Power MOSFETs ← Today
- Bipolar Junction Transistors (BJTs)
- Insulated Gate Bipolar Transistors (IGBTs)
- Thyristors (SCR, GTO, MCT)

Next

- On resistance vs. breakdown voltage vs. switching times
- Minority carrier and majority carrier devices

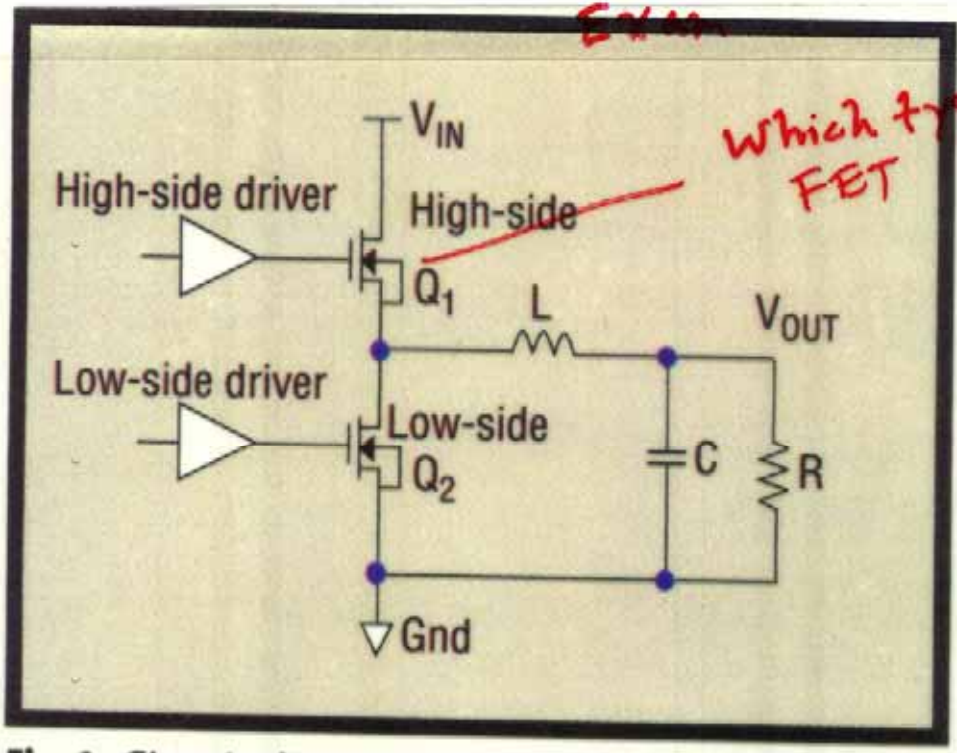
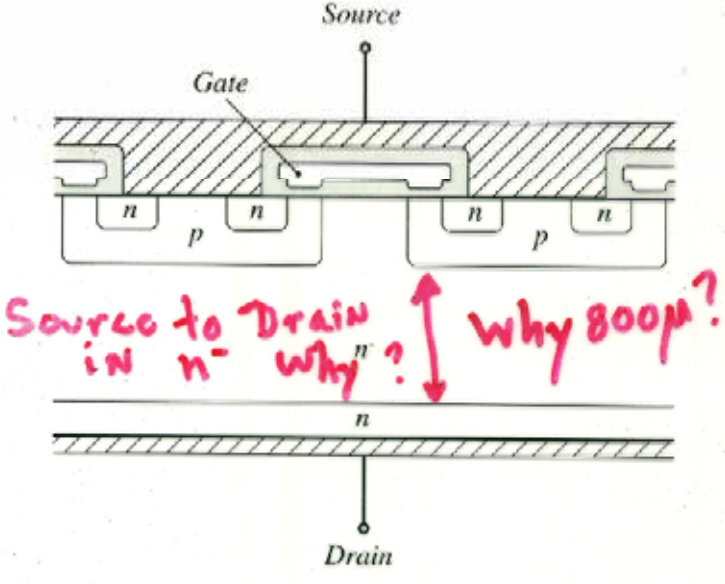


Fig. 1. *Circuit diagram of dc-to-dc synchronous buck converter.*

Optimized W gated Trench

Semiconductor (Structure Doping)

4.2.2. The Power MOSFET

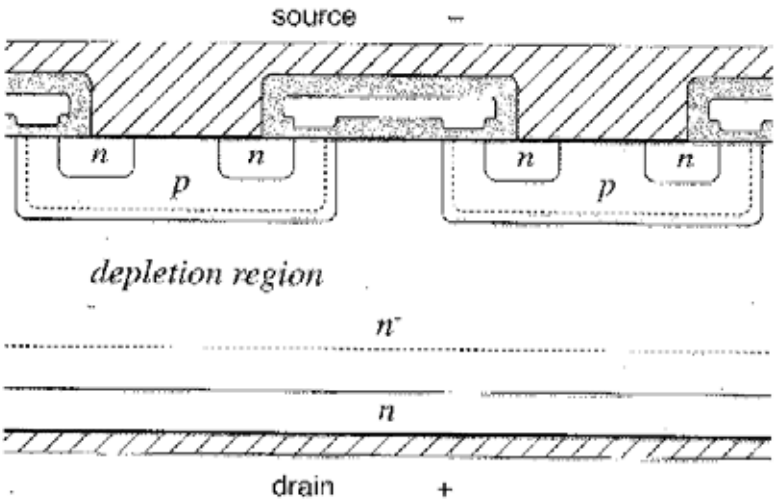


Source to Drain in n⁻ Why ?

Why 800μ?

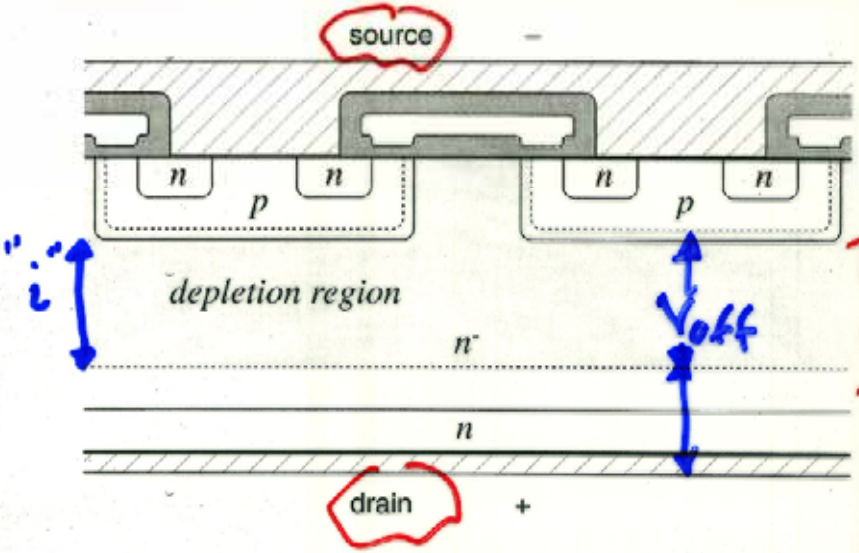
- Gate lengths approaching one micron
- Consists of many small enhancement-mode parallel-connected MOSFET cells, covering the surface of the silicon wafer
- Vertical current flow
- n-channel device is shown

MOSFET: Off state



- p-n^- junction is reverse-biased
- off-state voltage appears across n^- region

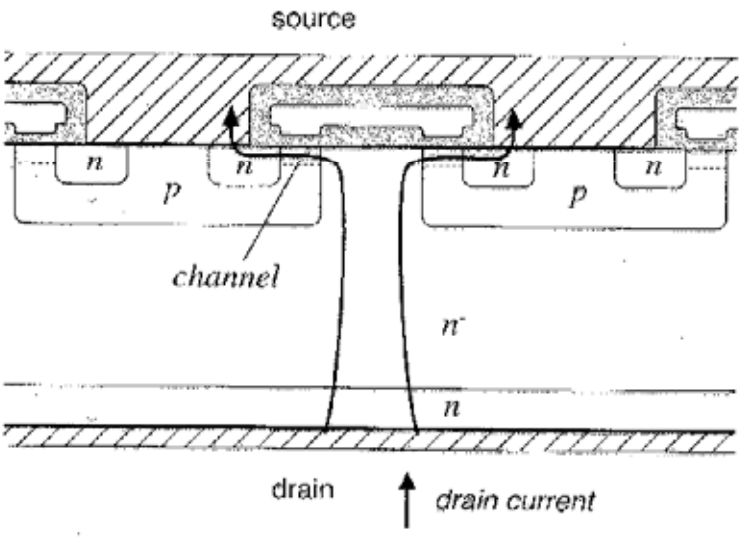
Vertical MOSFET: Off state



- *p-n* junction is reverse-biased
- off-state voltage appears across n region

Trade off!
large V_{off}
High R_{ON}
low doping
1000 in 11
lowers R_{ON}
but not
enough

MOSFET: on state



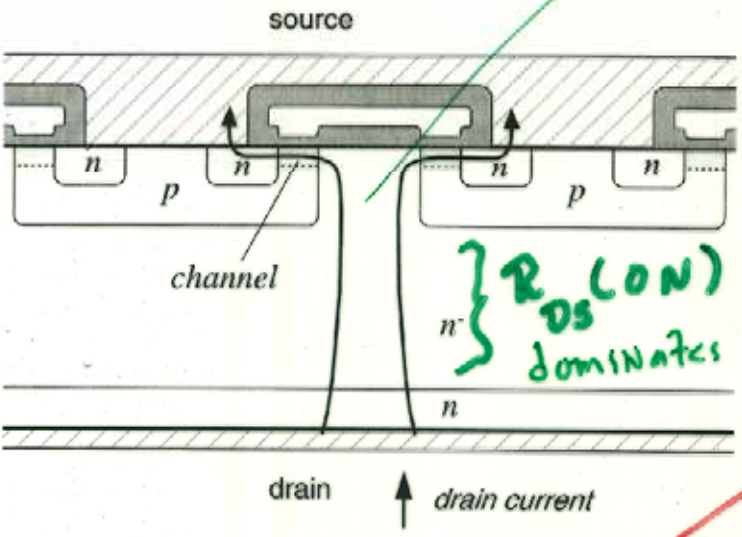
- p-n^- junction is slightly reverse-biased
- positive gate voltage induces conducting channel
- drain current flows through n^- region and conducting channel
- on resistance = total resistances of n^- region, conducting channel, source and drain contacts, etc.

CoolMOS R_{on} 特性 yes

U verticle inversion channel

way to lower R_{ON}

MOSFET: on state



- p-n^- junction is slightly reverse-biased
- positive gate voltage induces conducting channel
- drain current flows through n^- region and conducting channel
- on resistance = total resistances of n^- region, conducting channel, source and drain contacts, etc.

dominates

CAN improve?

20V Direct FET 6620 D↓ sw loss high
Synchronous FET 6620 D↑ I_{in}↑

MOSFET PACKAGING

Part #	$R_{DS(on)}$ mΩ @10V_{GS}	Q_G (nC)	Q_{GD} (nC)	Q_{SW} (nC)	I_D (A)
IRF6620	2.1	28	8.8	12	150*
IRF6623	4.4	11	4	5.2	55*
*T_{case} = 25°C					

High i

Q low for low driver loss

Table. *Typical MOSFET specifications.*

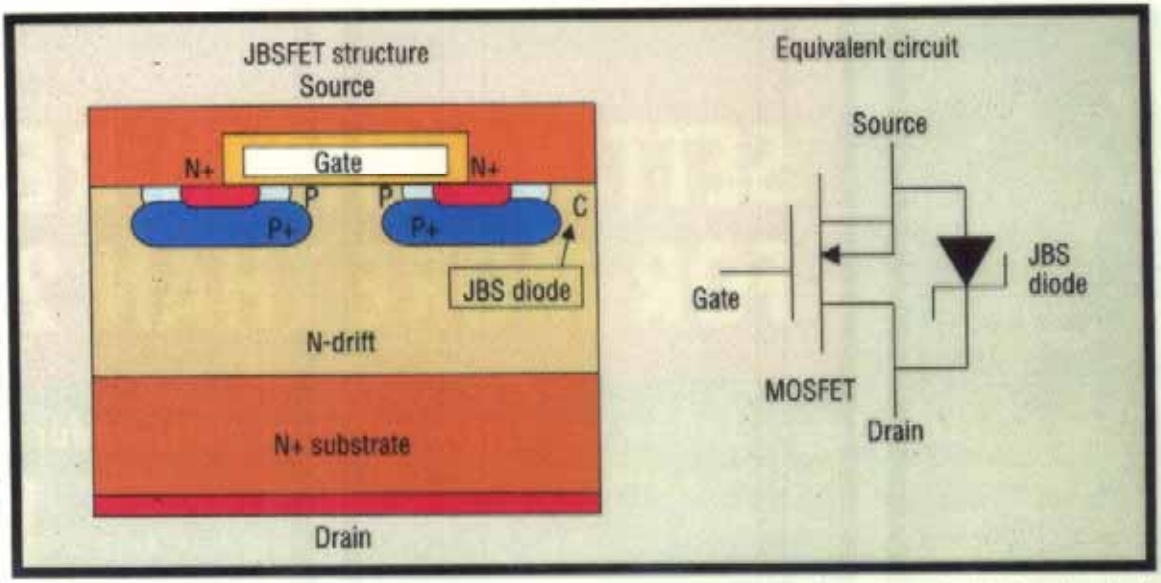


Fig. 5. *JBSFET structure and its equivalent circuit with Junction Barrier controlled Schottky diode.*

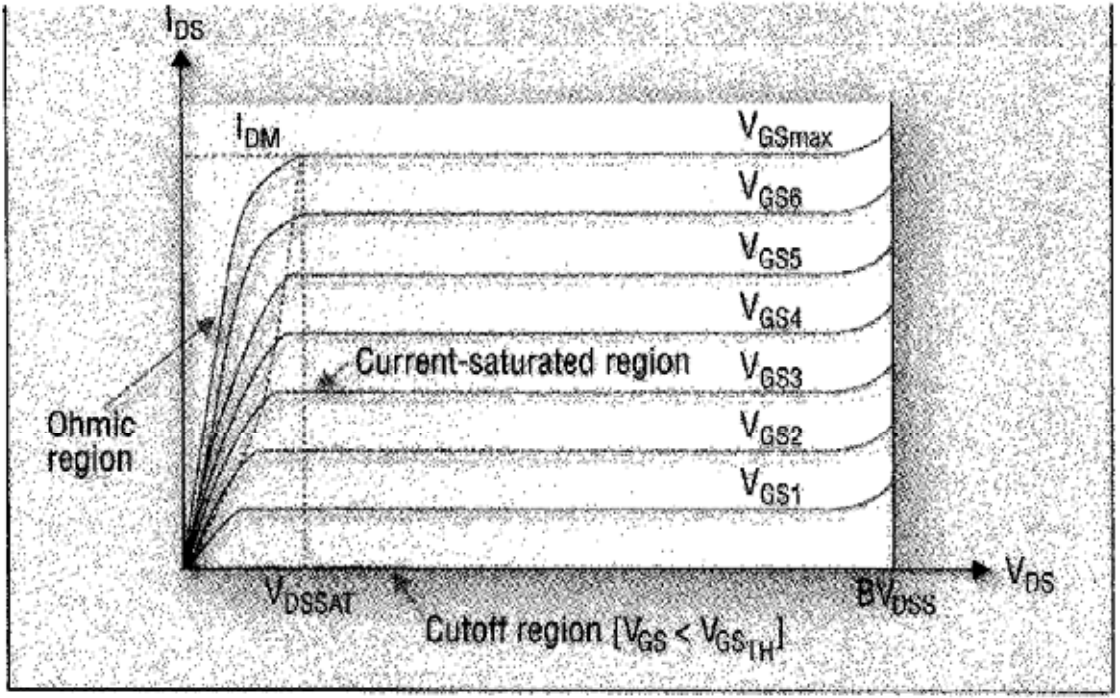
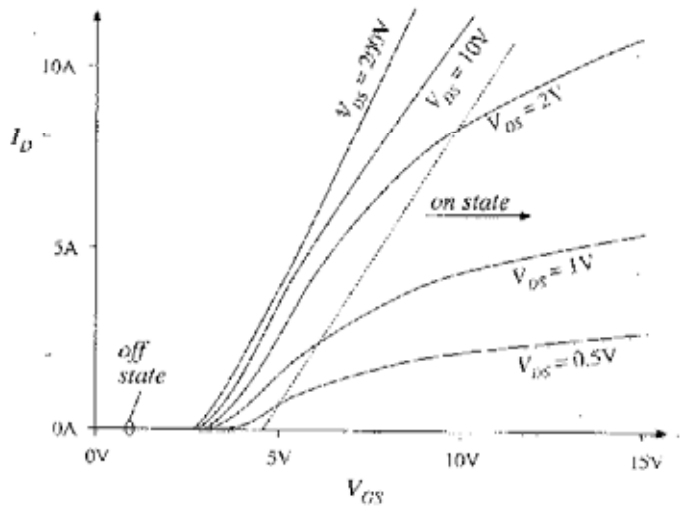


Fig. 1. *As shown in this generalized graph of output characteristics, an n-channel power MOSFET has three possible modes of operation.*

Typical MOSFET characteristics



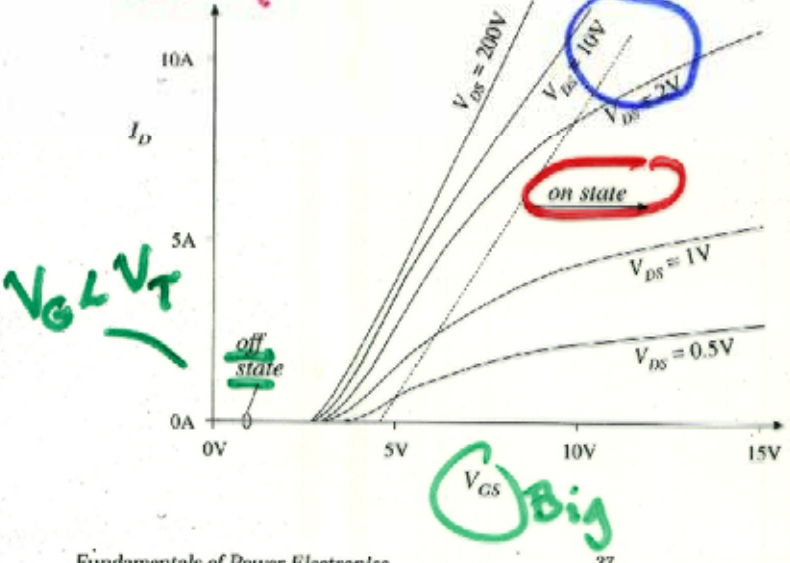
- Off state: $V_{GS} < V_{th}$
- On state: $V_{GS} >> V_{th}$
- MOSFET can conduct peak currents well in excess of average current rating —characteristics are unchanged
- on-resistance has positive temperature coefficient, hence easy to parallel

Fig 4.28 pg 80 C_{IN} to power Fet : 10nF 100nF

Typical MOSFET characteristics

Big gate voltage required

100A possible



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- On state: $V_{GS} >> V_{th}$
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5A

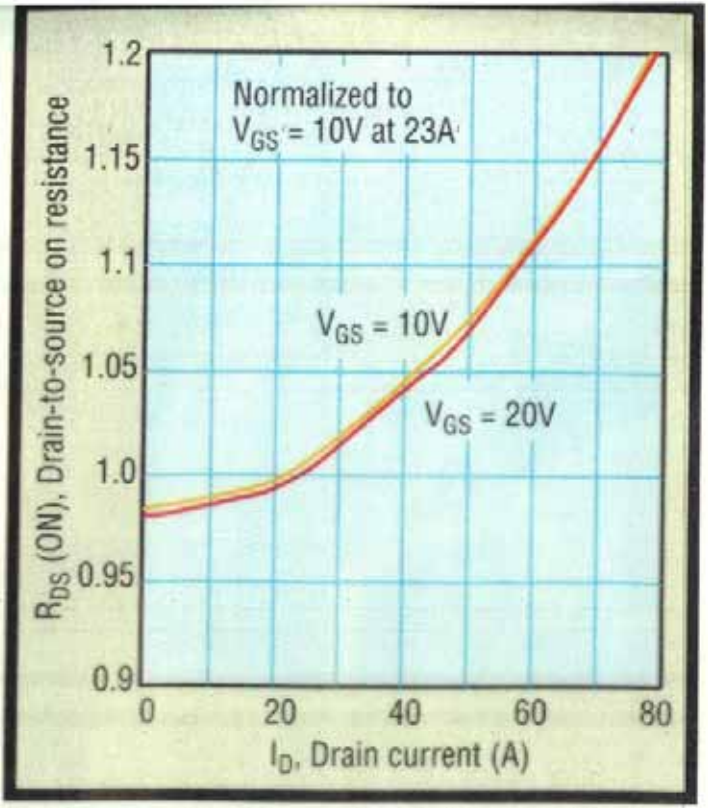

Fig. 3. *Normalized $R_{DS(on)}$ for APT5010B2LL at*

Characteristics of several commercial power MOSFETs

Part number	*Rated max voltage*	*Rated avg current*	R_{on}	Q_g *(typical)*
IRFZ48	60V	50A	0.018Ω	110nC
IRF510	100V	5.6A	0.54Ω	8.3nC
IRF540	100V	28A	0.077Ω	72nC
APT10M25BNR	100V	75A	0.025Ω	171nC
IRF740	400V	10A	0.55Ω	63nC
MTM15N40E	400V	15A	0.3Ω	110nC
APT5025BN	500V	23A	0.25Ω	83nC
APT1001RBNR	1000V	11A	1.0Ω	150nC

Pg 81

Characteristics of several commercial power MOSFETs

Gate charge to switch

R_{ON} > 10mΩ

Part number	*Rated max voltage*	*Rated avg current*	R_{on}	Q_g *(typical)*
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APT1001RBNR	1000V	11A	1.0Ω	150nC

Cool MOS Trench Gate will expand MOS usage to HV off and low R_{ON}

Turn on off

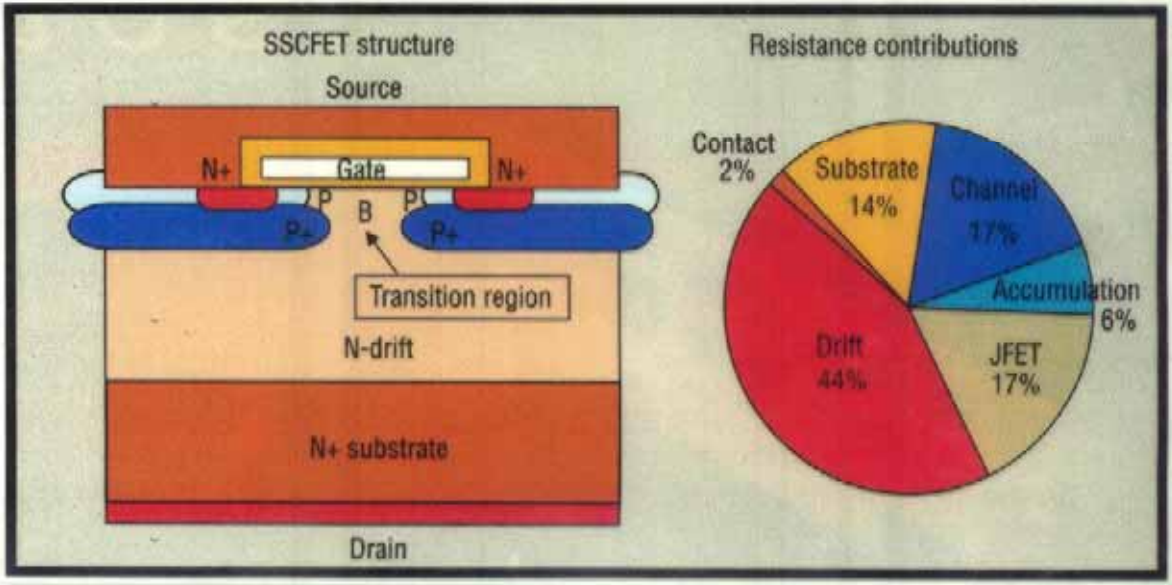


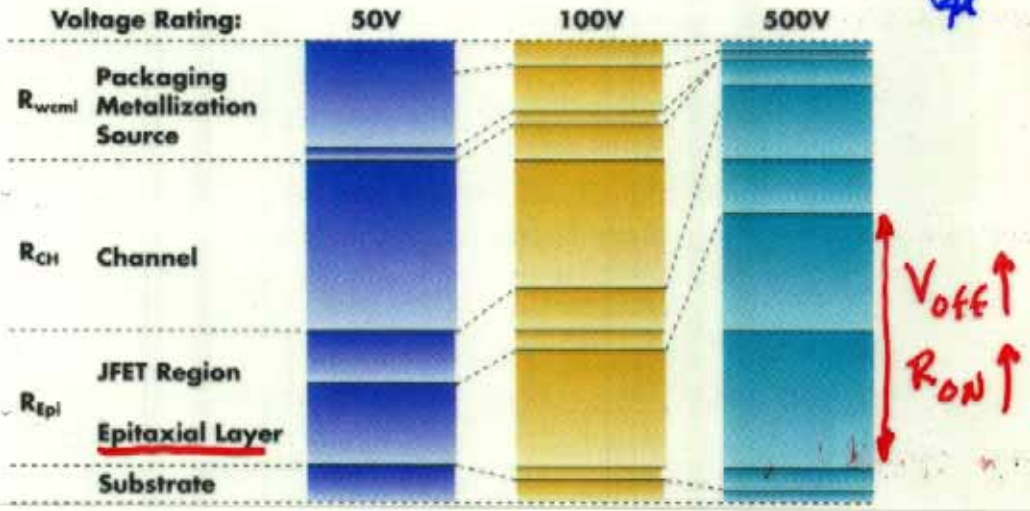
Fig. 4. *SSCFET structure and its internal resistance distribution.*

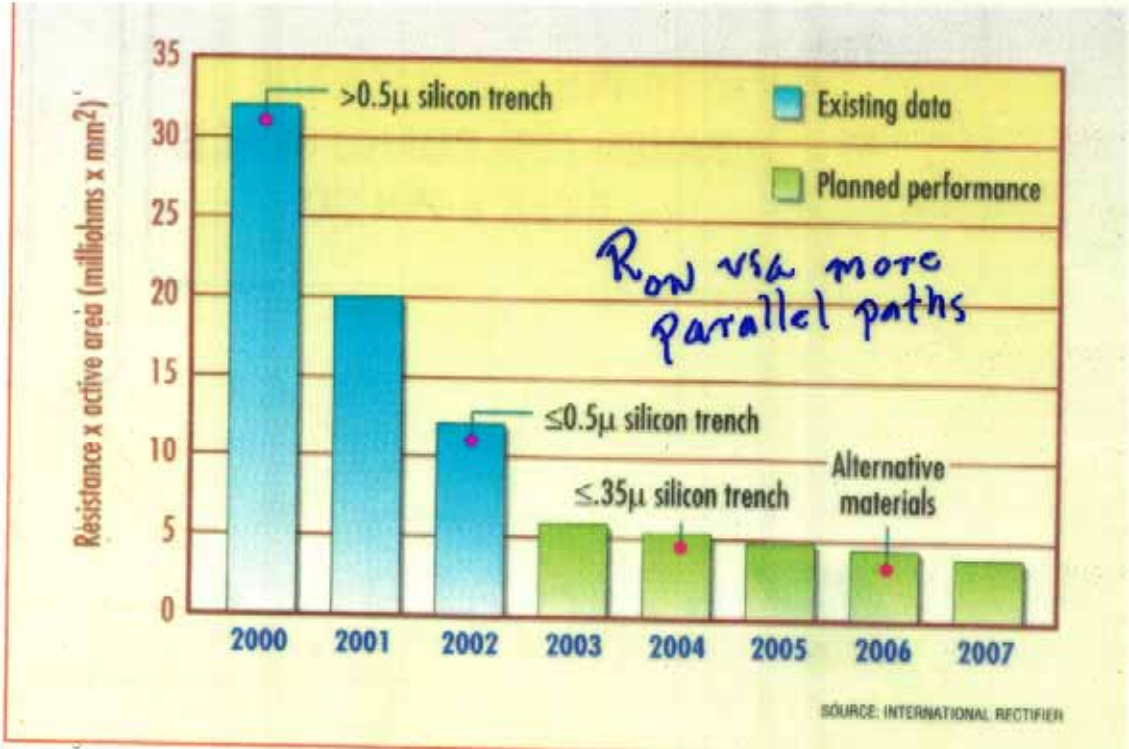
dominates for HV device

ON-STATE RESISTANCE ($R_{DS(on)}$)

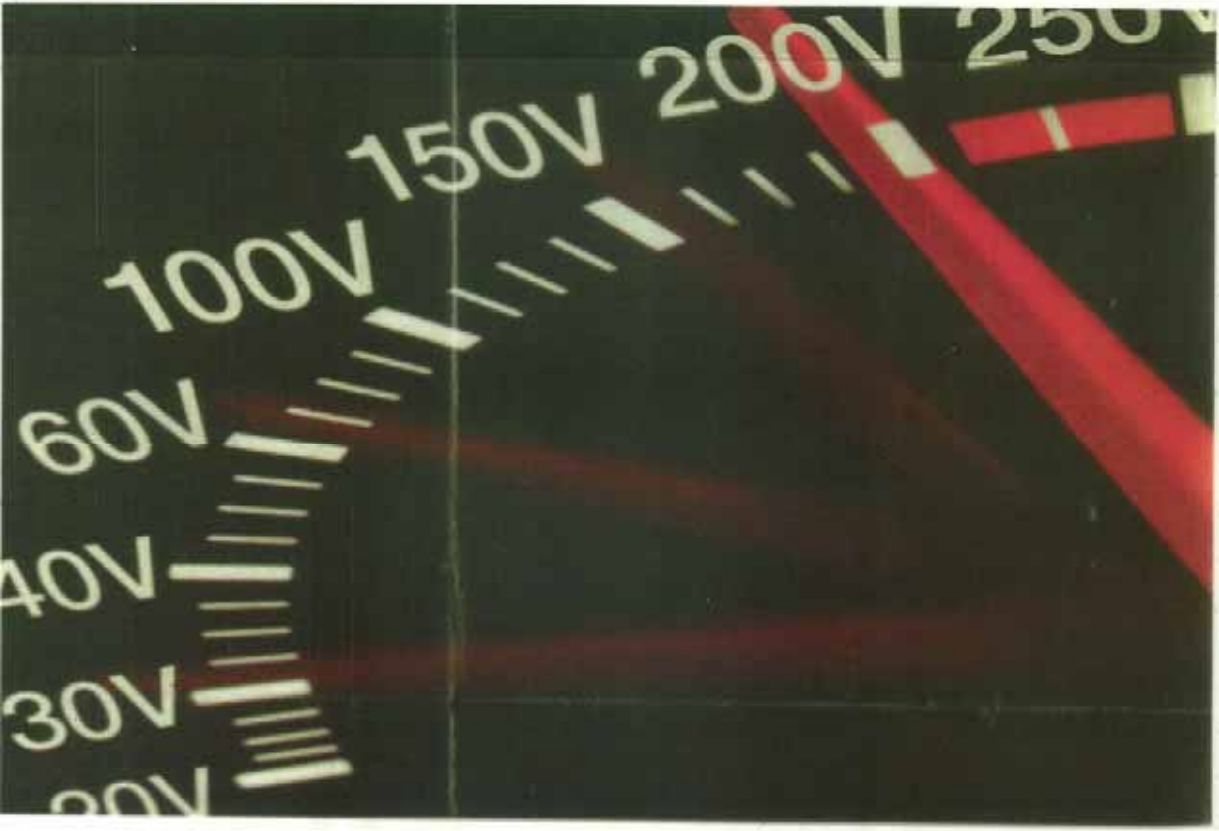
$R_{DS(an)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml}$

Substrate resistivity directly affects on-state resistance. For high voltage devices (500V) the total on-state resistance is dominated by Epi resistivity while for low voltage devices (50V) channel and external contacts and packaging play a more significant role. Substrate resistivity contributes more significantly to lower breakdown voltage devices.





The MOSFET's figure of merit for on-resistance—the product of device resistance R and active die area—improves 30 percent with each new technology generation.


150V
200V
100V
60V
40V
30V

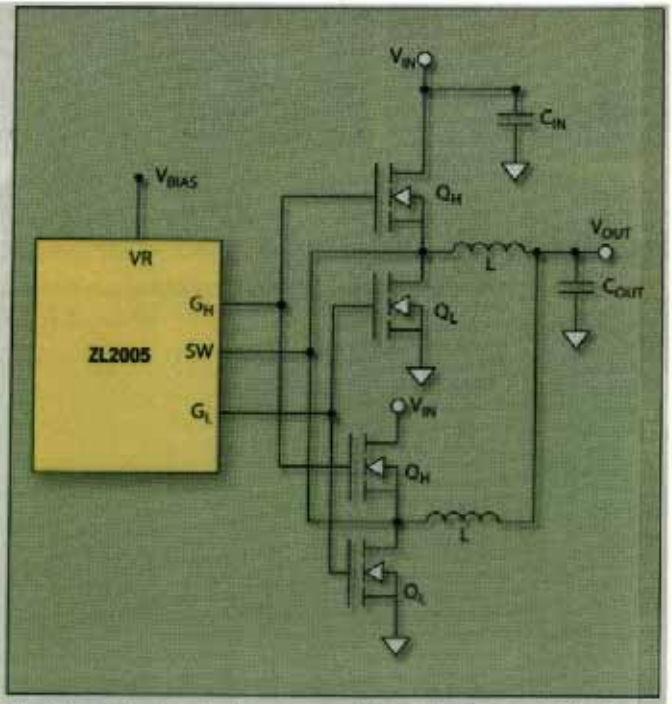


Fig. 1. *A single-phase buck converter with dual inductors and dual MOSFETs on the high and low sides allow the use of standard low-profile components for a design that delivers 40 A.*

single-phase operation. This design will deliver 40 A, which

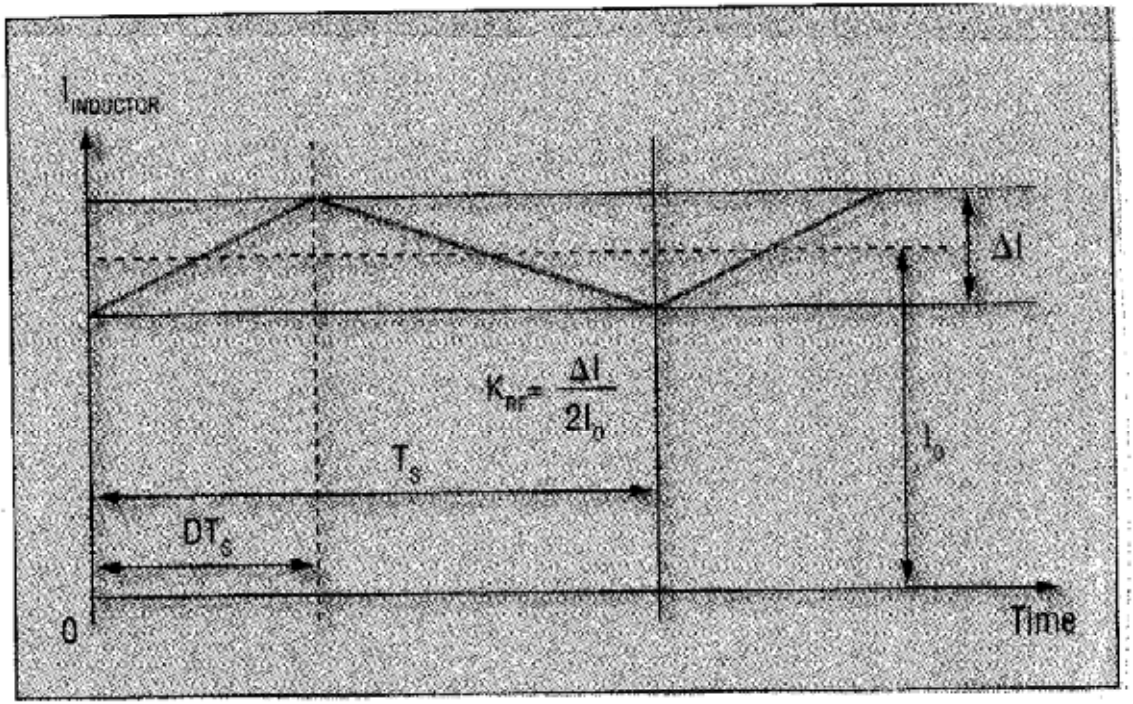


Fig. 3. *The ripple-current factor KRF affects several aspects of the converter and must be established early in the design process. It is typically assigned a value between 0.1 and 0.2* [2].

Pulse-width modulation: a control strategy for power converters, wherein the device is switched on and off with a duty cycle that keeps the average voltage over the switching period equal to the desired voltage value.

Rectifier: a power converter for ac-to-dc conversion, in which the power flows predominantly from the ac to dc side.

Safe operating area: a domain of voltage and current values within which the sustained operation of a device in various modes is safe. The modes include turn-on, turn-off, and on and off states.

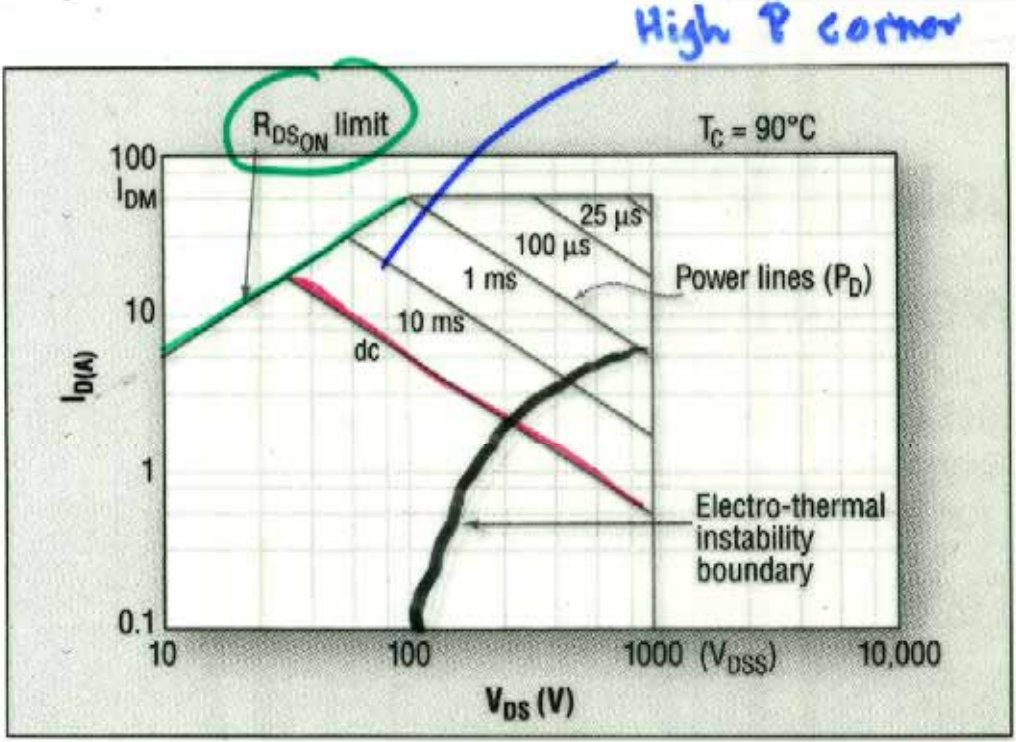


Fig. 2. *Power MOSFETs optimized for switched-mode designs have limited ability to operate in the corner of the FBSOA graph, where electro-thermal instability can occur as shown here for a typical n-channel power MOSFET.*

SOA

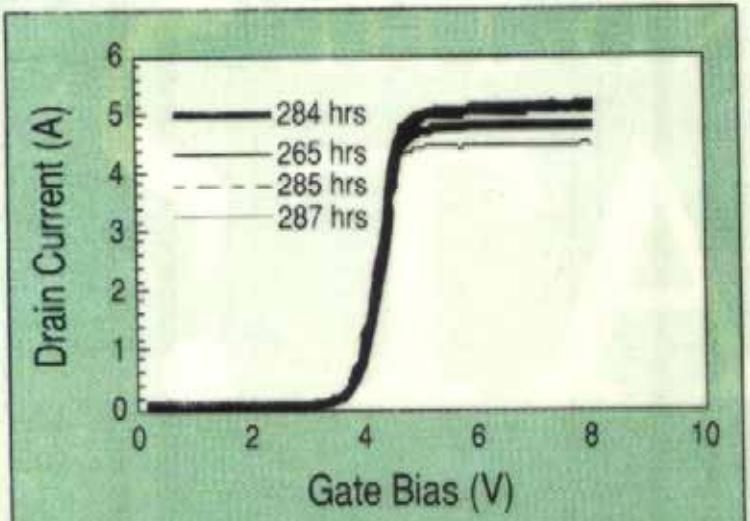


Figure 3. *Degradation of MOSFET transfer curve with time under avalanche stress.*

With (avalanch stress)

R_{ON} ↑

V_{BK} ↓

∴ Reduce SOA

Other stress

$\frac{dV}{dt}$

reverse recovery Q_{rr}

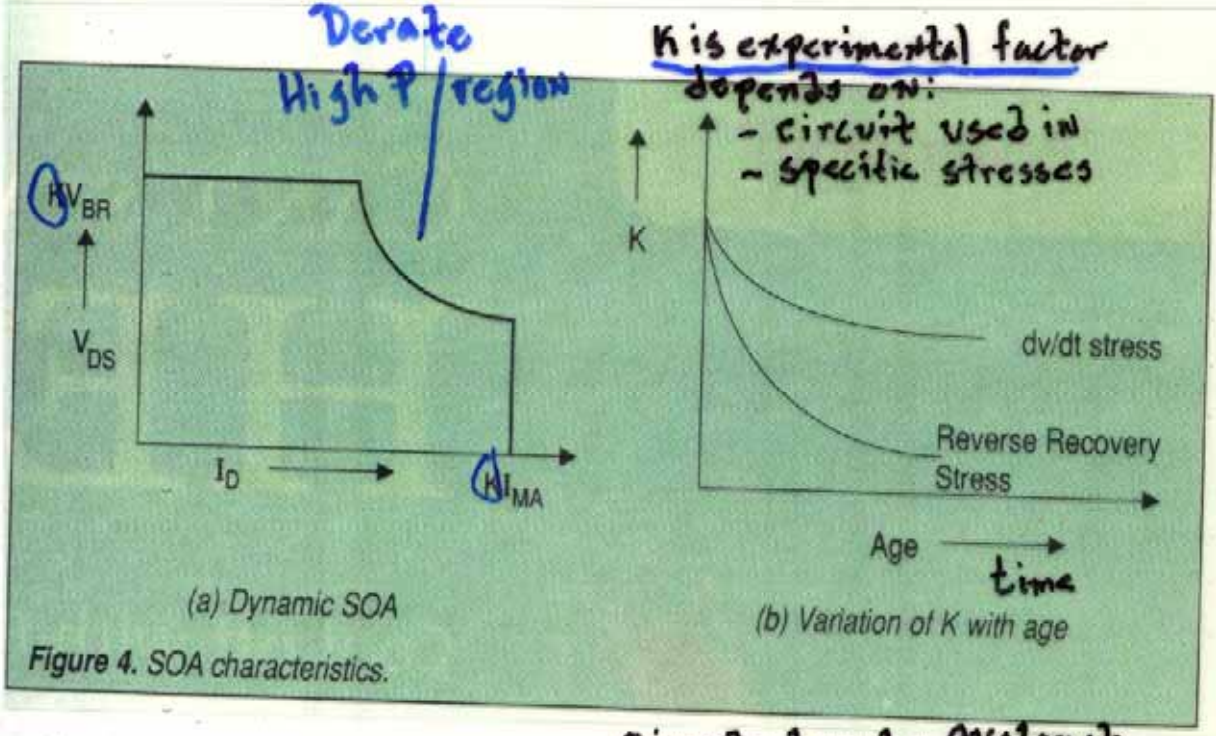


Figure 4. SOA characteristics.

Simple boost: Avalanch stress

Bridge: Qrr from body diode

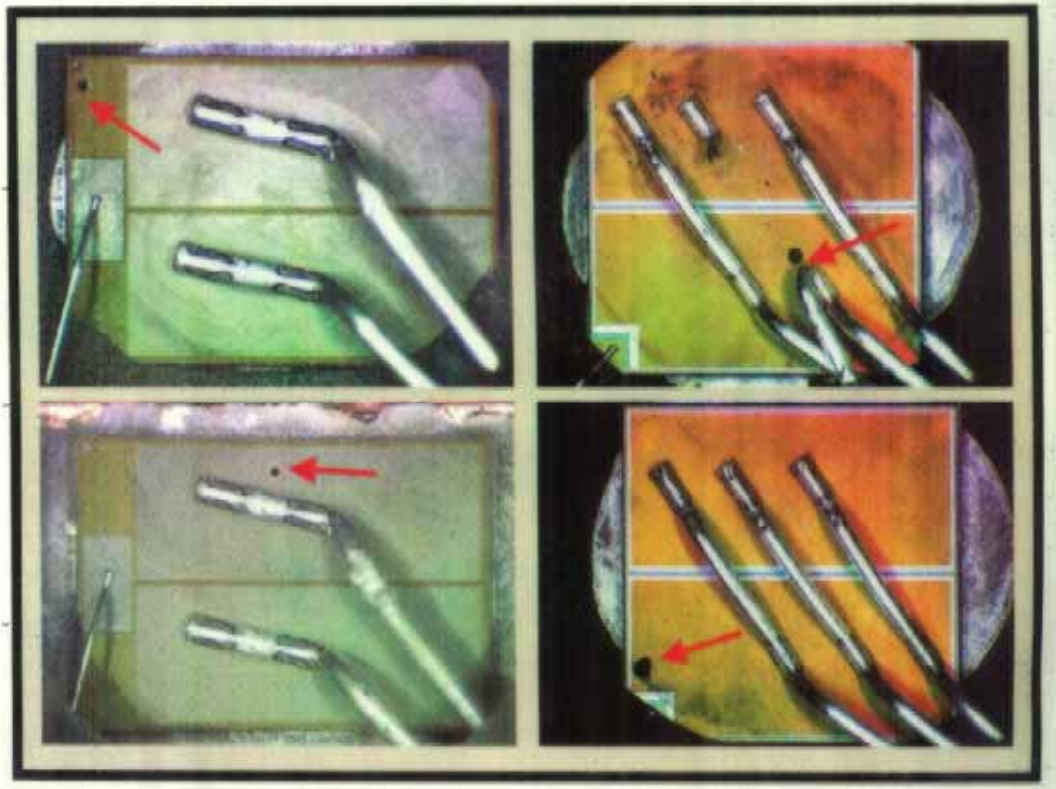
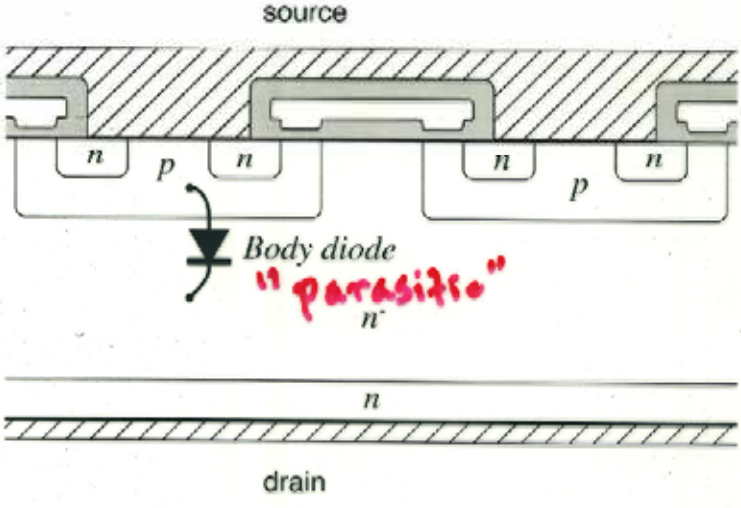


Fig. 3. *Avalanche damage to Planar FETs (left) and Trench FETs (right). The bond-wire has been cut and moved out of the way to expose the damage in the part at upper right.*

MOSFET body diode



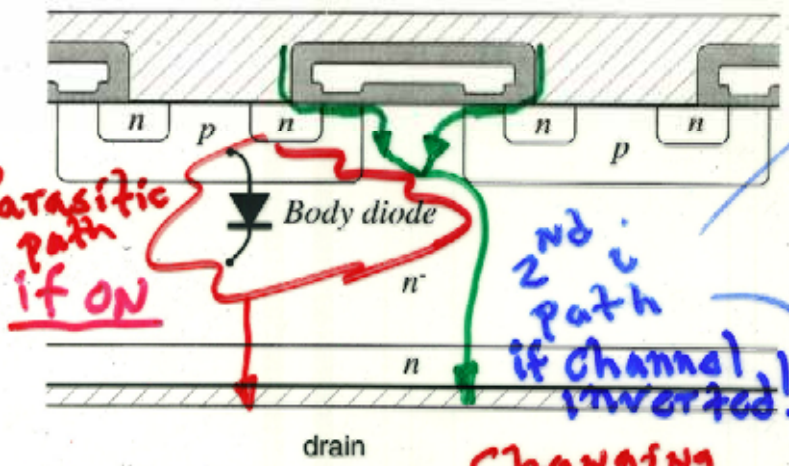
- p-n^- junction forms an effective diode, in parallel with the channel
- negative drain-to-source voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q_r is large

Fig 4.27 c Pg 99

MOSFET body diode

Similiar to L_m of a transformer

You have to know this parasitic well



Parasitic path if ON

2nd path if Channel inverted!

- *p-n* junction forms an effective diode, in parallel with the channel
- negative drain-to-source voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q_r is large

Changing but

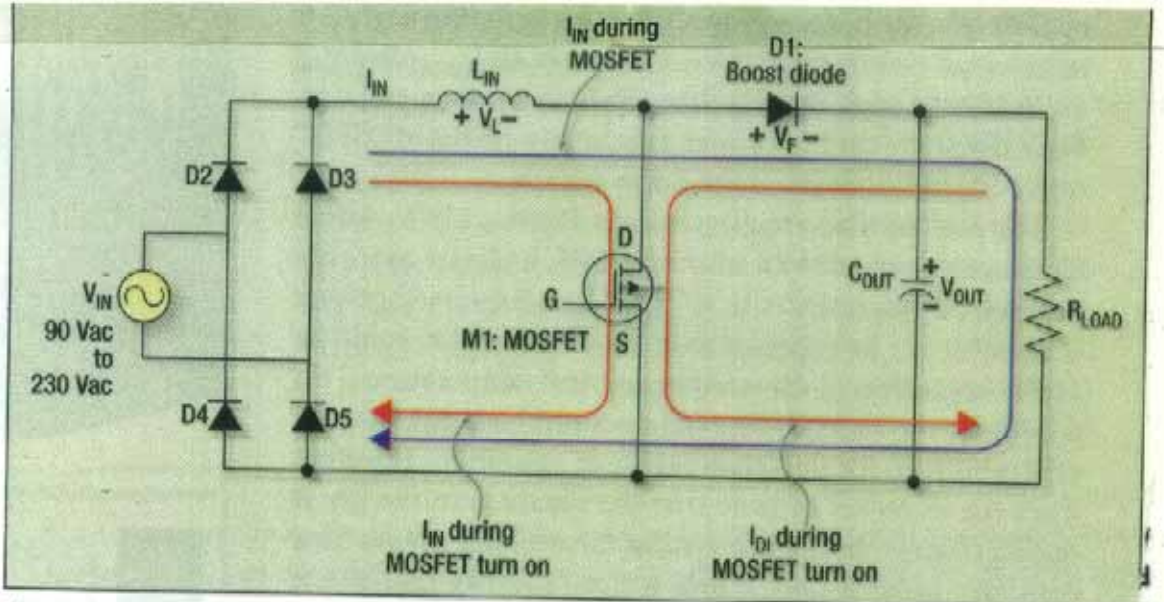


Fig. 1. *In the basic PFC circuit operated in CCM, the reverse-recovery current of the boost diode significantly contributes to the switching losses of the MOSFET.*

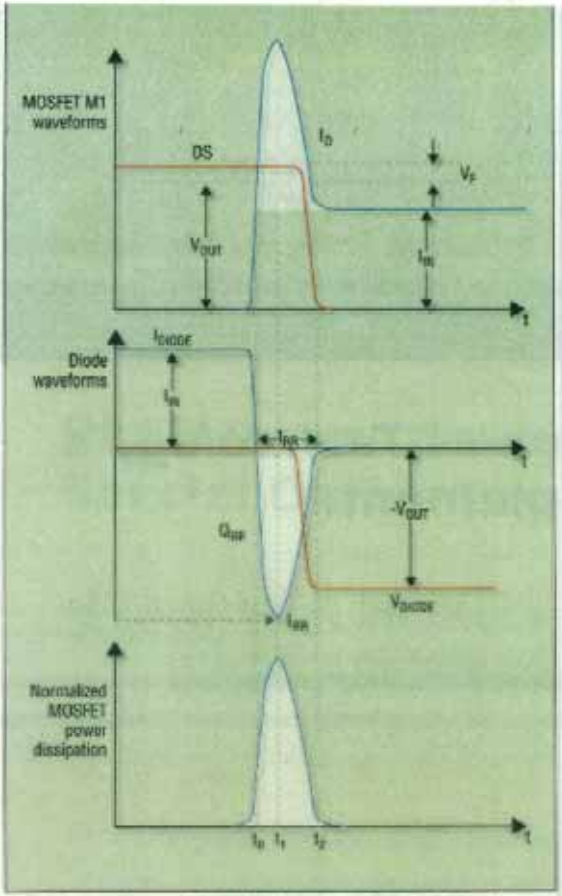
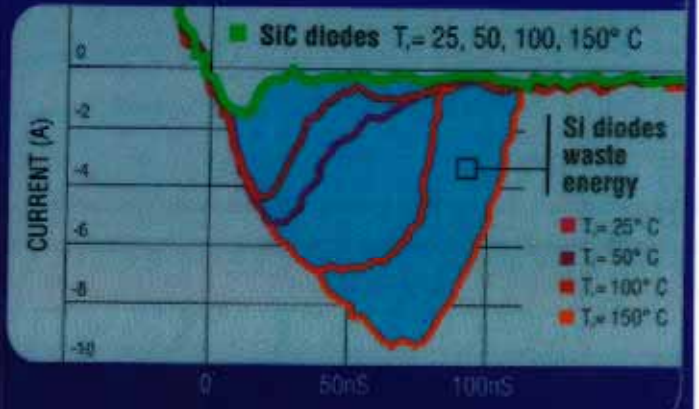
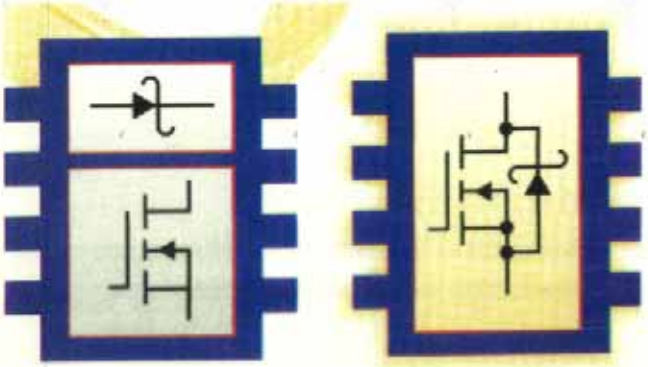


Fig. 2. *The waveforms of a CCM PFC stage reveal how switching losses occur in pulses when non-zero voltages and currents, including reverse-recovery currents from the boost diode, overlap.*

SiC. THE MATERIAL OF CHOICE.

- ZERO RECOVERY® Rectifier
- Higher frequency operation
- No high frequency ringing
- Lower switching loss
- Lower noise
- Cooler operating temperature
- Higher power density

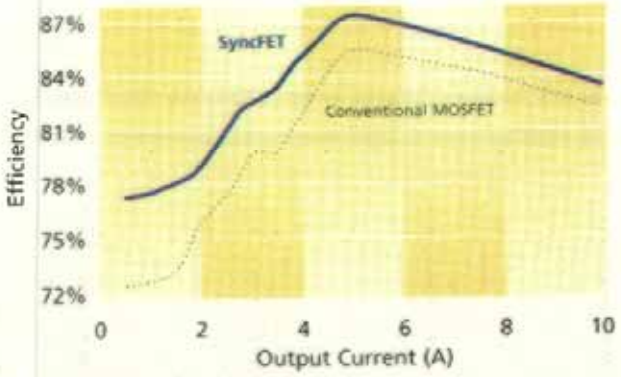


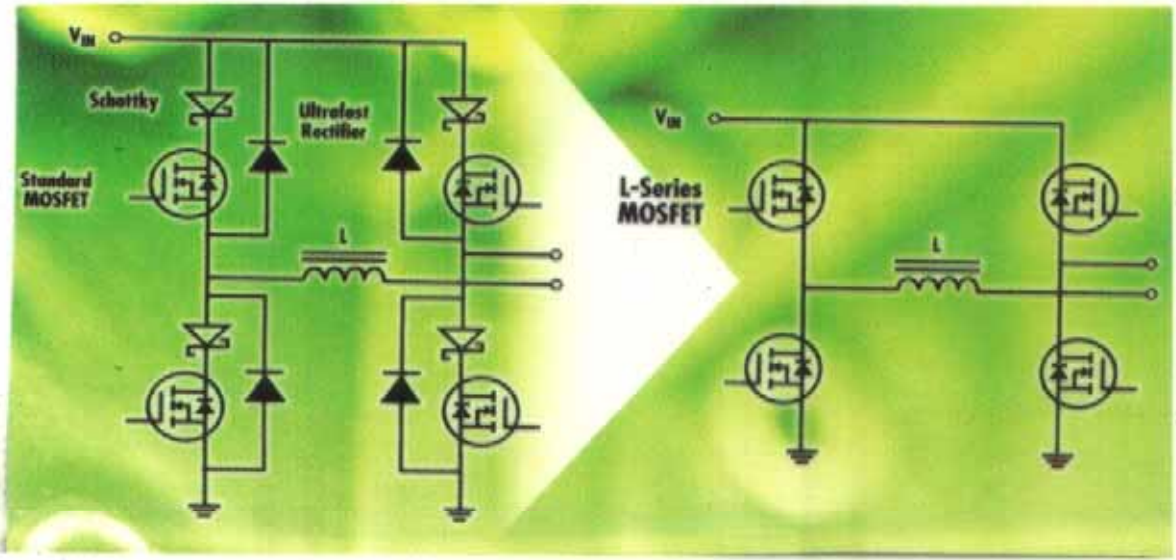


Co-Packaged
MOSFET & Schottky

SyncFET Monolithic
MOSFET & Schottky

Effect of SyncFET on Efficiency




V_{IN}
Schottky
Ultrafast Rectifier
Standard MOSFET
L
V_{IN}
L-Series MOSFET
L

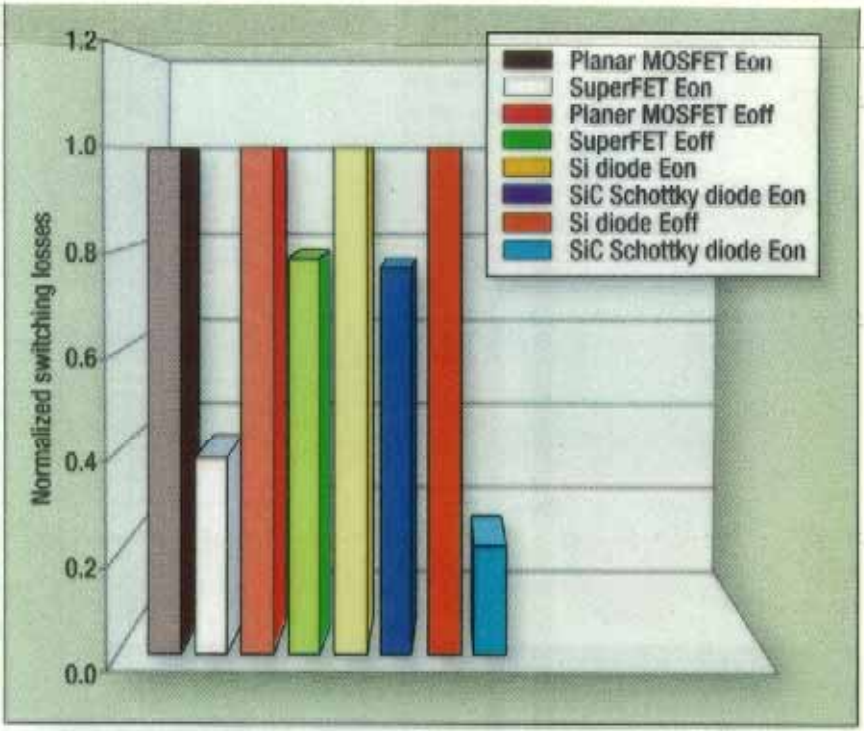


Fig. 5. *The normalized switching losses of the SuperFET/SiC Schottky diode combination and the planar-MOSFET/Si diode combination reveal the substantial gains in efficiency provided by the former configuration.*

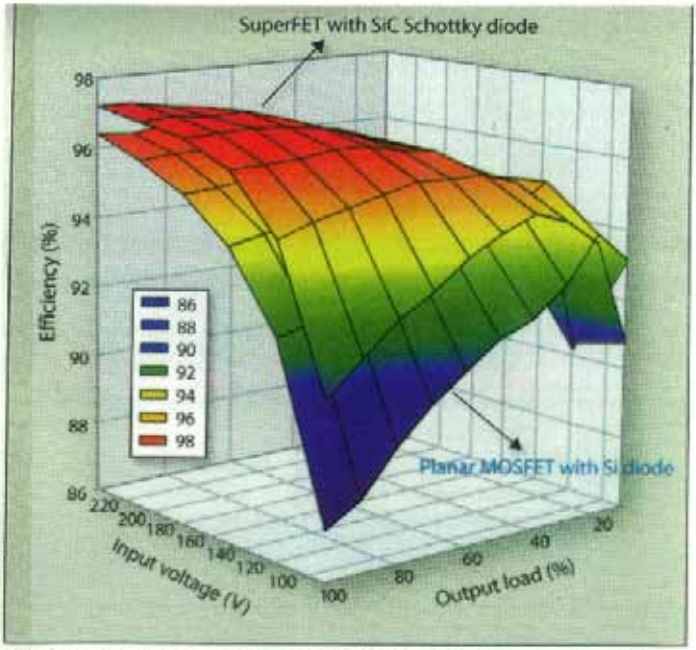
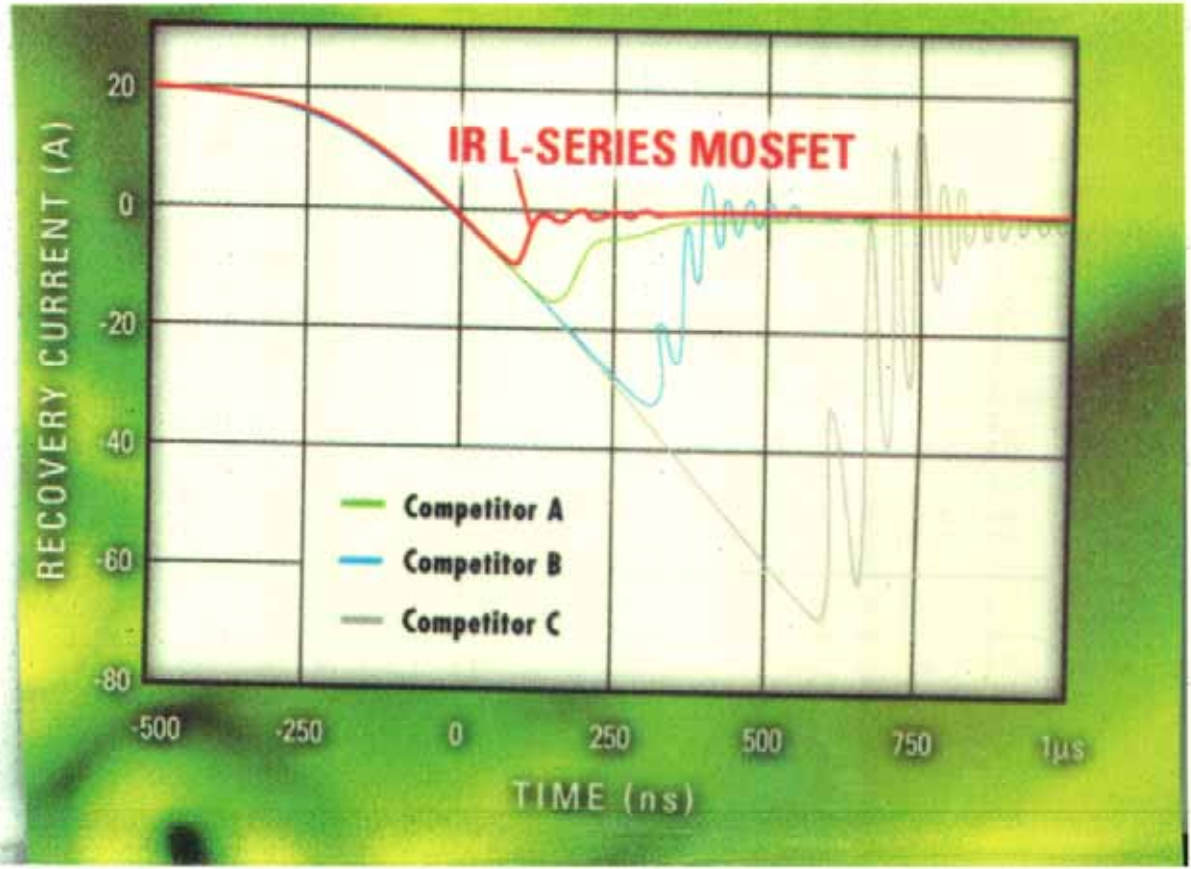


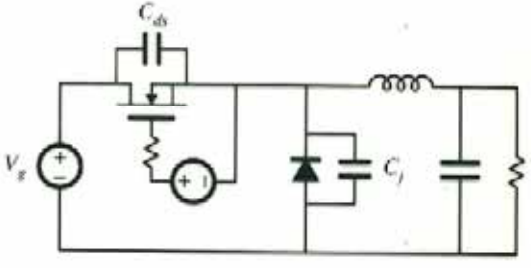
Fig. 6. *The efficiency of the SuperFET/SiC Schottky diode combination vs. the planar MOSFET/Si diode combination in a 400-W CCM PFC design directly translates into lower temperatures, higher power densities and reduced heatsink requirements.*


IR L-SERIES MOSFET
RECOVERY CURRENT (A)
20
0
-20
-40
-60
-80
-500
-250
0
250
500
750
1µs
TIME (ns)
Competitor A
Competitor B
Competitor C

More (Energy Loss) due to $\frac{1}{2}CV^2$

Switching loss caused by semiconductor output capacitances

Buck converter example



Energy lost during MOSFET turn-on transition (assuming linear capacitances):

$$W_C = \tfrac{1}{2}\,(C_{ds} + C_j)\,V_g^2$$

Some other sources of this type of switching loss

Schottky diode

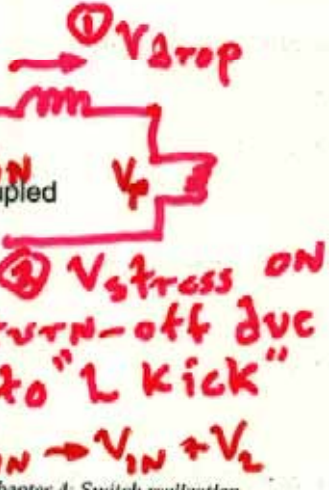
- Essentially no stored charge
- Significant reverse-biased junction capacitance

Transformer leakage inductance

- Effective inductances in series with windings
- A significant loss when windings are not tightly coupled

Interconnection and package inductances

- Diodes
- Transistors
- A significant loss in high current applications



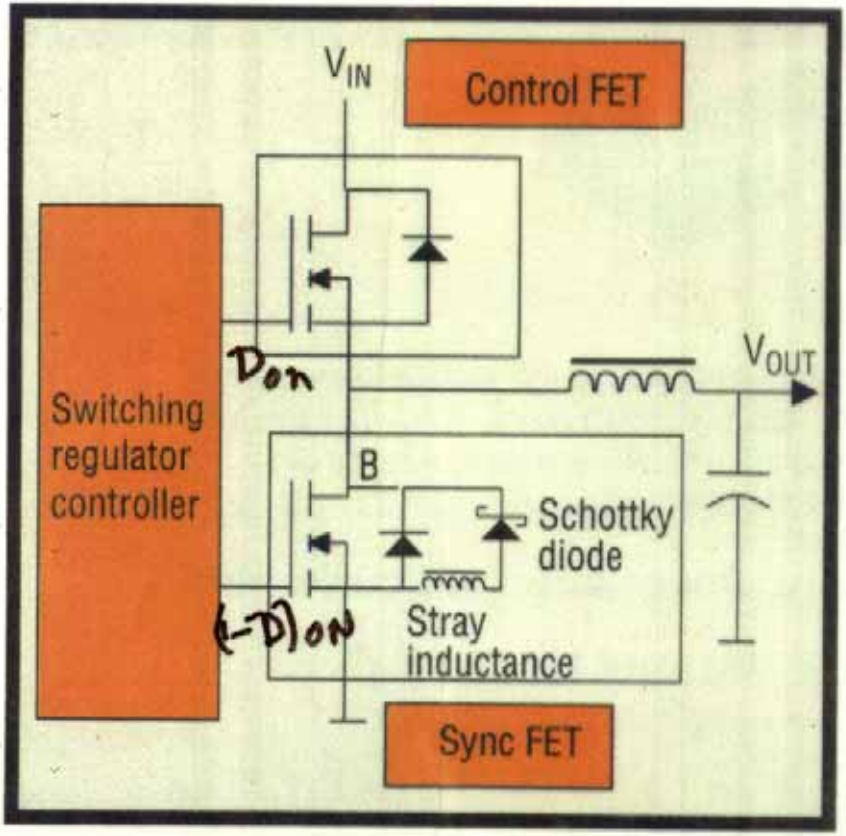


Fig. 1. *Sync-buck dc-dc converter topology.*

Control FET

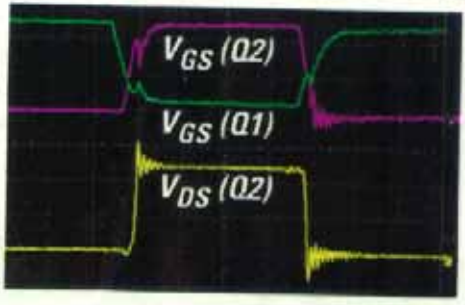
Type	$V_{(BR)DSS}$ [V]	I_D [A]	$R_{DS(on)}$max @10V [mΩ]	Q_g (tot) @10V [nC]	Package
STS12NH3LL	30	12	14*	9.5*	SO-8
STD38NH02L	20	38	13.5	18	DPAK
STB50NH02L	20	50	13.5	18	D²PAK
STD50NH02L	20	50	10	22	DPAK

*Available in Q1 2003. Values refer to 4.5V VGS

Synchronous FET

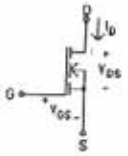
Type	$V_{(BR)DSS}$ [V]	I_D [A]	$R_{DS(on)}$max @10V [mΩ]	Q_g (tot) @10V [nC]	Package
STD90NH02L	20	60	6	47.5	DPAK
STD100NH02L	20	60	4.8	62	DPAK
STB130NH02L	20	90	4.4	69	D²PAK
STS25NH3LL	30	25	3.5	50	SO-8
STD150NH02L	20	150	3.3	69	ClipPAK(1)

(1)same footprint as DPAK

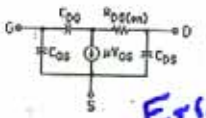


Predictive Gate Drive and Switch Node Waveforms

Texas Instruments introduces a new synchronous buck driver for today's low output voltage, nonisolated high-efficiency power converters. The **UCC27222** employs Predictive Gate Drive™ technology, which is a self-contained feedback system that looks ahead and optimizes the overlap of the two gate drive transitions. Adjusting for changing operating conditions, the Predictive Gate Drive minimizes body diode conduction and reverse recovery losses for up to 4% efficiency gain over adaptive drive technologies and up to 40% improved thermal dissipation for higher reliability.



Symbol



Approximate Equivalent Circuit

Erickson

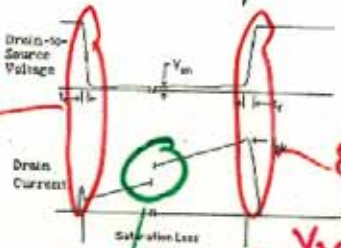
Gate

Gate Drive

Drive Power

$P = f_{sw}[E_{on} + E_{off}]$

neglect as V_G, I_G are low?



E(off to on)

V_{on} rises as I_{on} ramps up

E(on to off)

V_{DS} and I_{on} effects

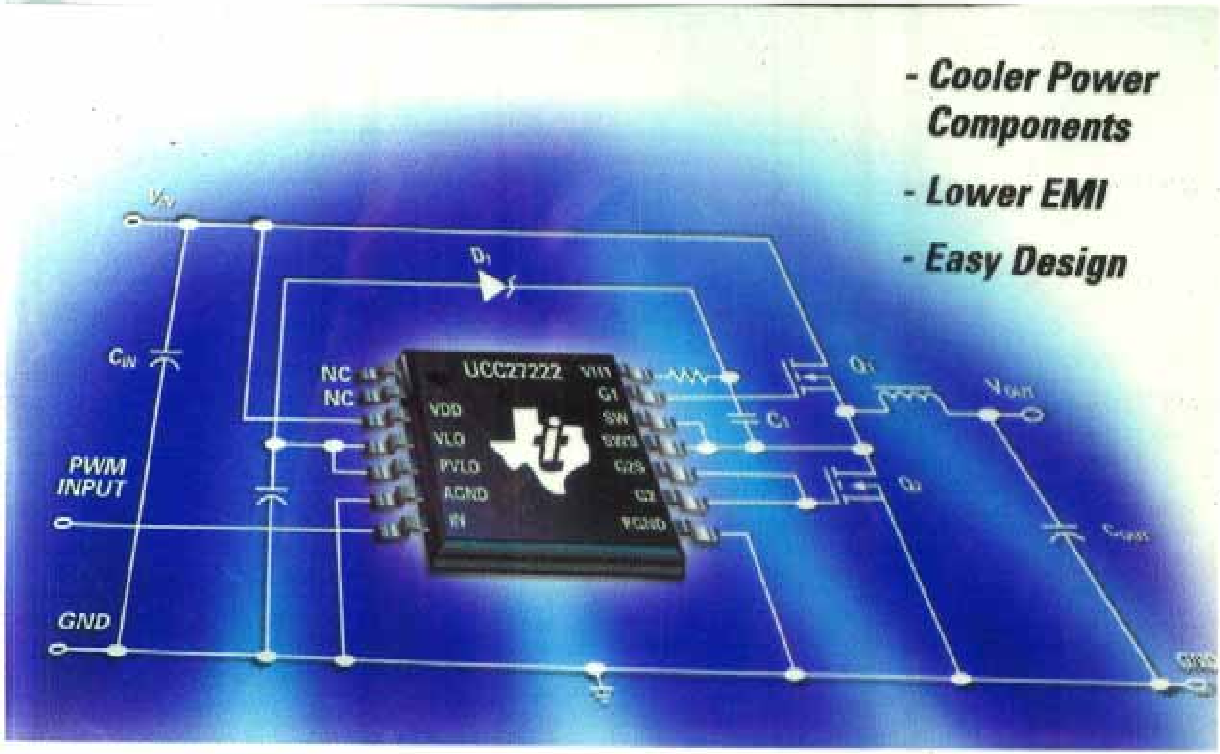
$P(sw\,loss) = f_{sw}[E(_{off}^{on}) + E(_{on}^{off})] + ?$

0

These I_d and V_{ds} waveforms will allow us to calculate switch loss for each switching cycle. The cycle includes two parts as each switch alternates on and off alternatively. We neglect switch driver losses for now.

NOT IN ERICKSON

$\frac{di}{dt}$ limited by $\frac{V}{L}$


- Cooler Power Components
- Lower EMI
- Easy Design
UCC27222
NC
NC
VDD
VLO
PVLO
AGND
IN
G1
SW
G2
PGND
PWM INPUT
GND
D1
Q1
Q2
C1

Typical Power FET

$C_g = 10nF \quad V_g = 10V$

$f_{sw} = MHz$

$P \sim \frac{1}{2} C_g V_g^2 * f_{sw} = 10^{-8}\ 10^{2}\ 10^{6}$

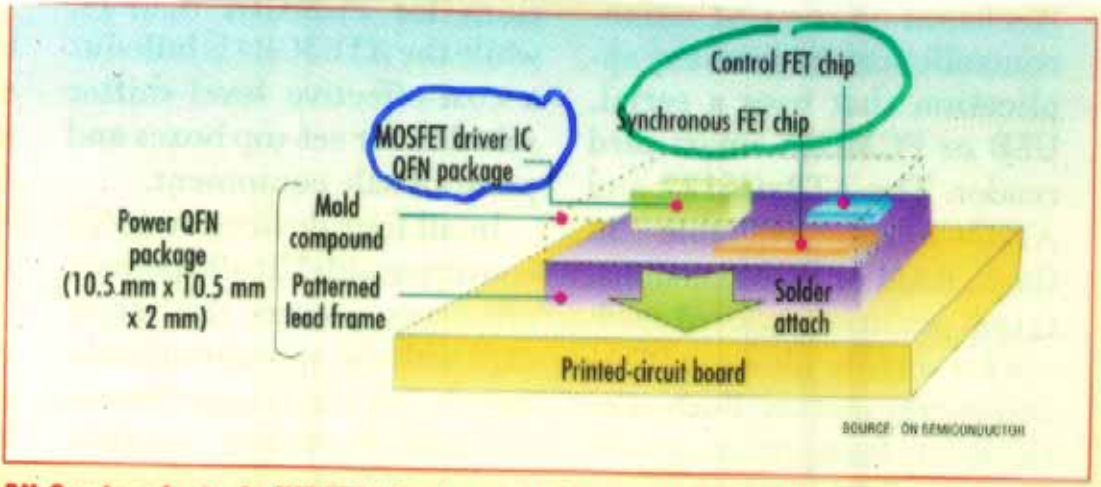
$\frac{1}{2} C_g V_g^2$: energy to switch ON-off, off-ON

$10^{-8}\ 10^{2}\ 10^{6}$: 1W — no big deal

if $C_g \rightarrow 1.0\,\mu F$

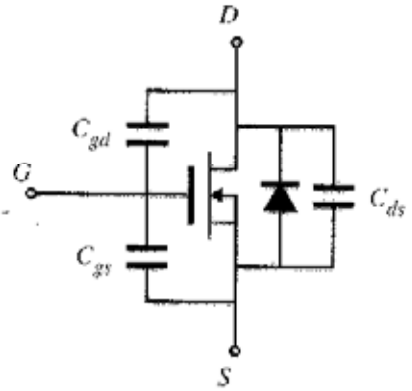
$P \sim C_g V_g^2 f_{sw} = 10^{-6}\ 10^{2}\ 10^{6}$

100W ☹



ON Semiconductor's NIS3001 implements the company's package-within-a-package technology, which typifies the arriving breed of power devices that extends the building-block multichip module approach to dc/dc converters.

A simple MOSFET equivalent circuit



- C_{gs} : large, essentially constant
- C_{gd} : small, highly nonlinear
- C_{ds} : intermediate in value, highly nonlinear
- switching times determined by rate at which gate driver charges/discharges C_{gs} and C_{gd}

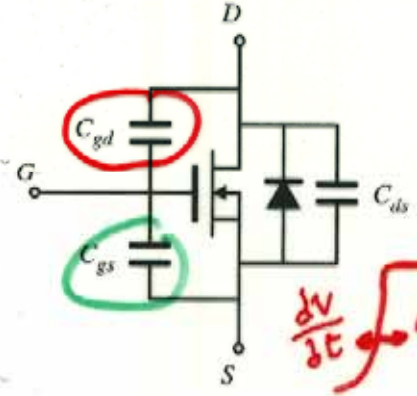
$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \qquad C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$

CV=Q C_{ds}↓ when V_{ds}↑ is good !! for fast off time slower on time ok !!

Fig 4.29 p380

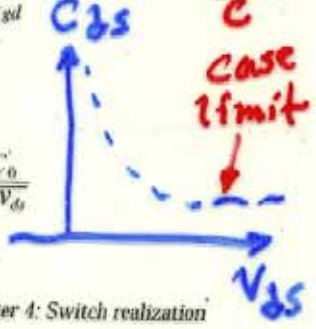
A simple MOSFET equivalent circuit

More free parasitic elements: C Device



- C_{gs} : large, essentially constant 100nF 10nF
- C_{gd} : small, highly nonlinear Miller C
- C_{ds} : intermediate in value, highly nonlinear
- switching times determined by rate at which gate driver charges/ discharges C_{gs} and C_{gd}

$\frac{dv}{dt} \propto \frac{I}{C}$



$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}}$$

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0}{\sqrt{v_{ds}}}$$

MOSFET nonlinear C_{ds}

Approximate dependence of incremental C_{ds} on v_{ds} :

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0}{\sqrt{v_{ds}}}$$

Energy stored in C_{ds} at $v_{ds} = V_{DS}$:

$$W_{Cds} = \int v_{ds}\, i_C\, dt = \int_0^{V_{DS}} v_{ds}\, C_{ds}(v_{ds})\, dv_{ds}$$

$$W_{Cds} = \int_0^{V_{DS}} C_0(v_{ds})\, \sqrt{v_{ds}}\, dv_{ds} = \frac{2}{3}\, C_{ds}(V_{DS})\, V_{DS}^2$$

— same energy loss as linear capacitor having value $\frac{4}{3}\, C_{ds}(V_{DS})$

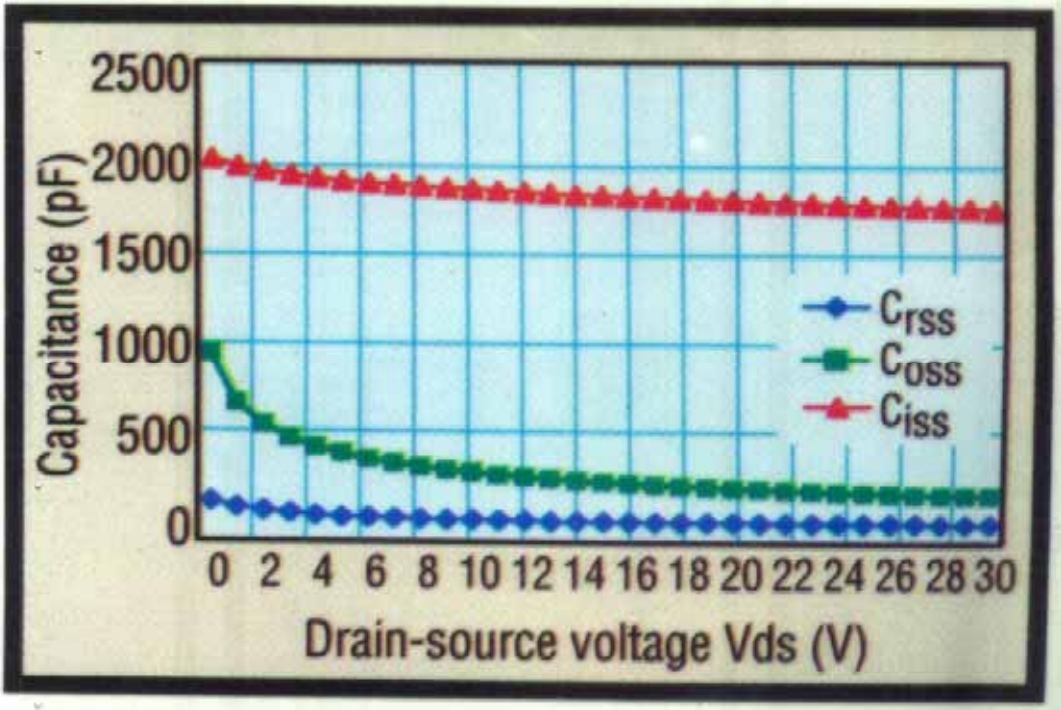


Fig. 8. *Capacitances of a WFET vs. drain voltage.*

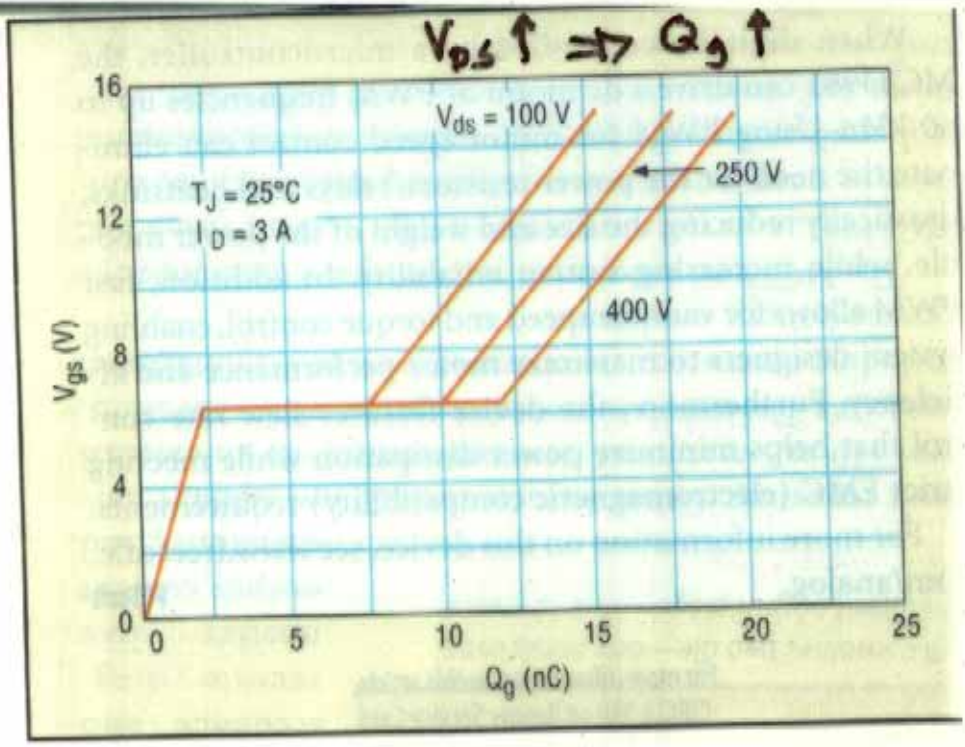


Fig. 1. *A typical MOSFET gate-charge graph.*

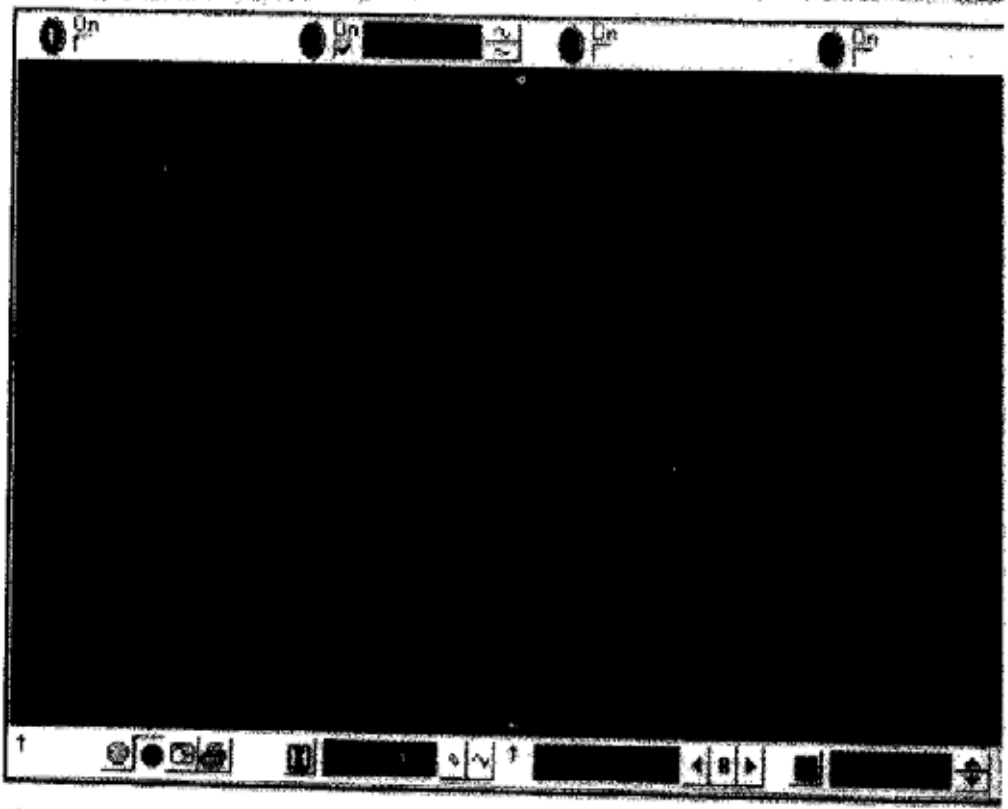


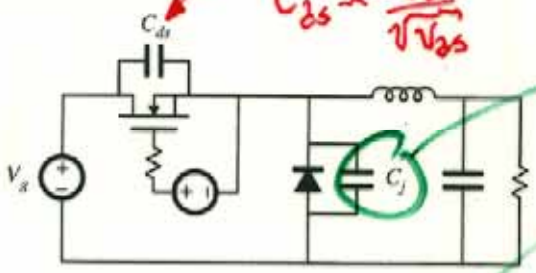
Fig. 3. *When a MOSFET switch is activated at zero V_{dd} the Miller plateau goes away.*

C_{DS} = min ⇒ low Q

Fig 4.52 pg 98

Example: semiconductor output capacitances

Buck converter example



drain to source

$C_{DS} \sim \frac{C_0}{\sqrt{V_{DS}}}$

Typical values? see spec sheets

Energy lost during MOSFET turn-on transition (assuming linear capacitances):

$$W_C = \tfrac{1}{2}(C_{ds} + C_j)V_g^2$$

TR was off is C_{DS} max or min?

TR must "eat" this storing charge during turn-ON

Gate drive loss not covered by ETTLCKBOM

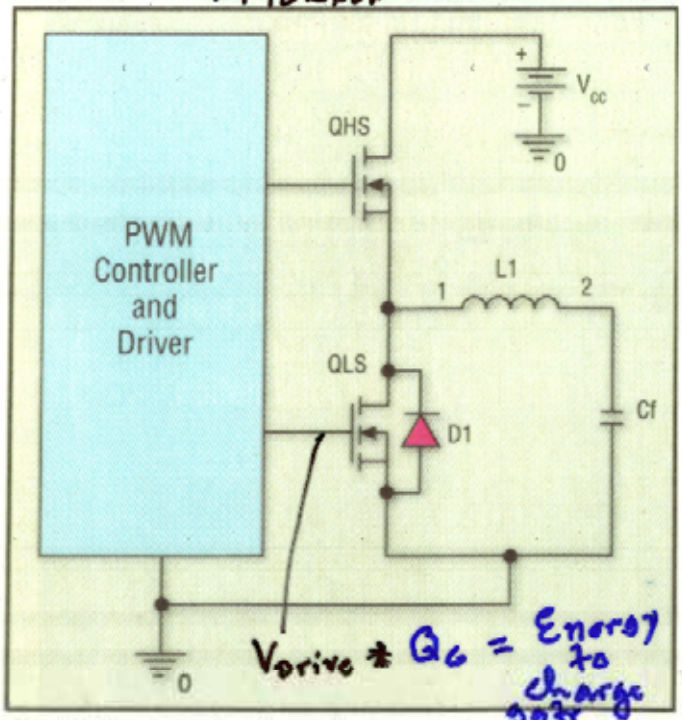
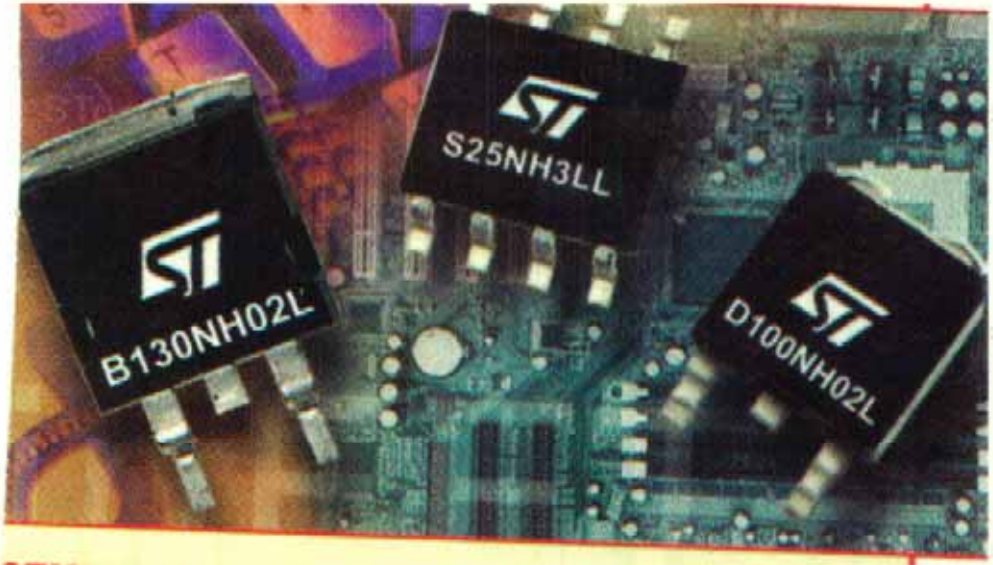


Fig. 1. *The classical synchronous buck converter uses two switching MOSFETs: the high-side (control) device, QHS, and the low-side synchronous rectifier, QLS.* $E = \frac{1}{2} C_g V_g^2 = \frac{Q_g^2}{2 C_g}$



STMicroelectronics tweaks gate geometries and cell densities to improve figure of merit—the product of on-resistance and gate charge—in its StripFET III line.

$R_{ON} * Q_G$

Units nC & mΩ

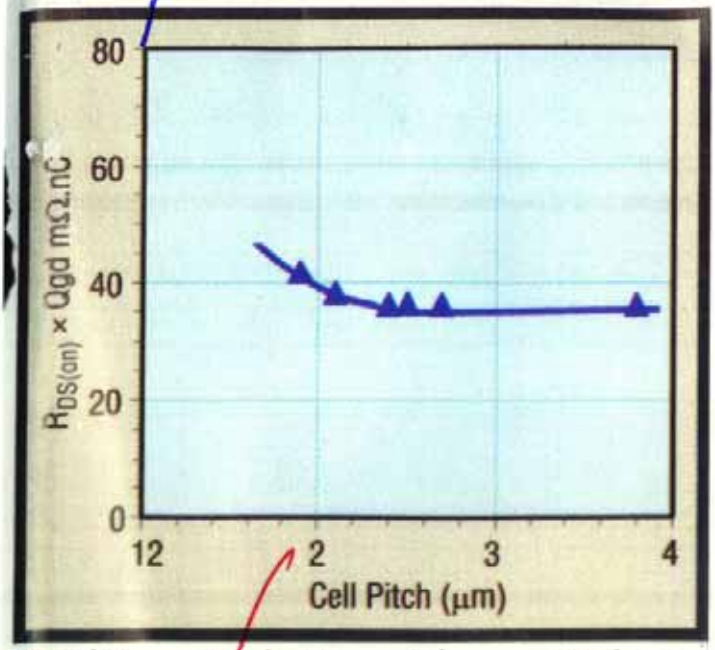
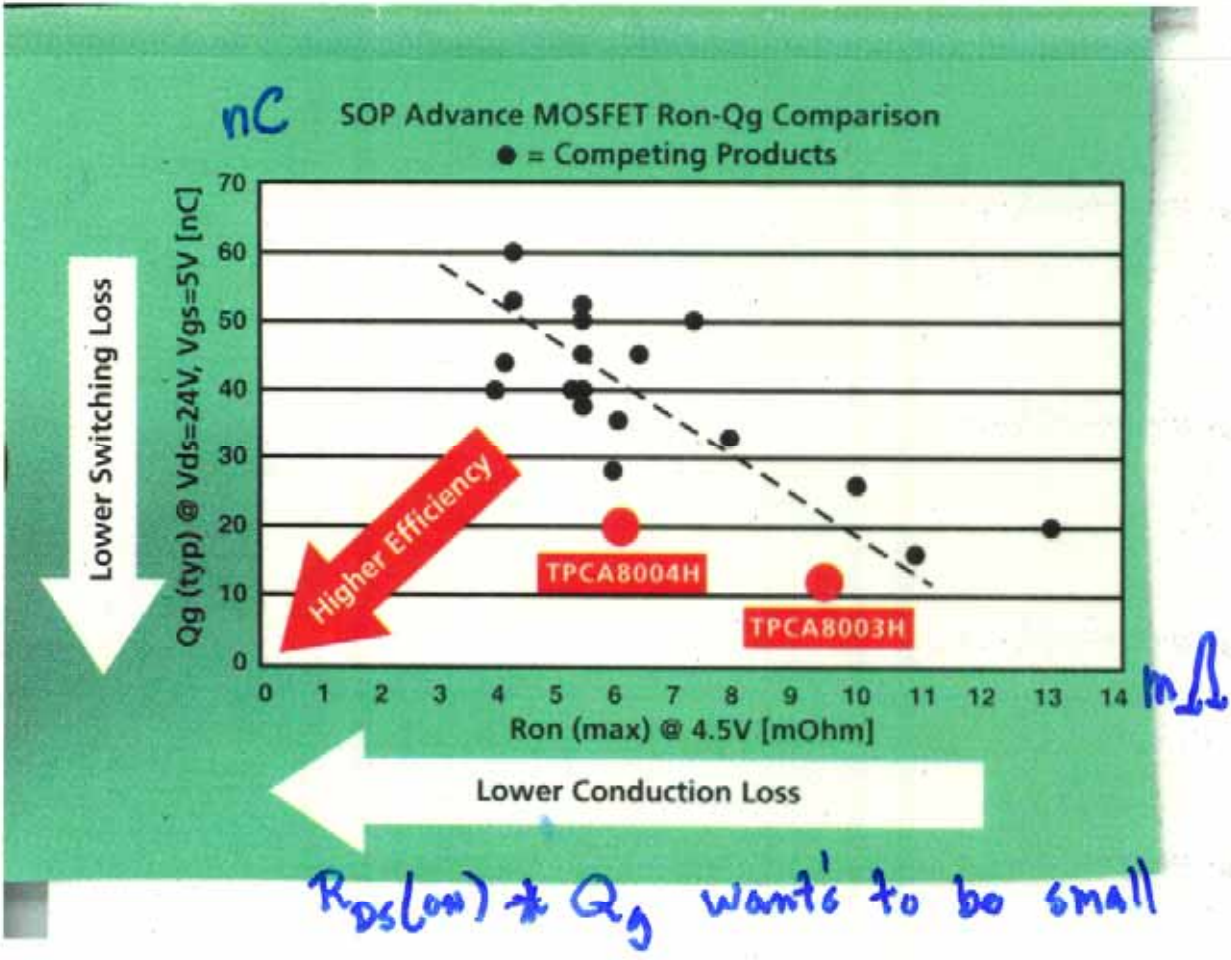
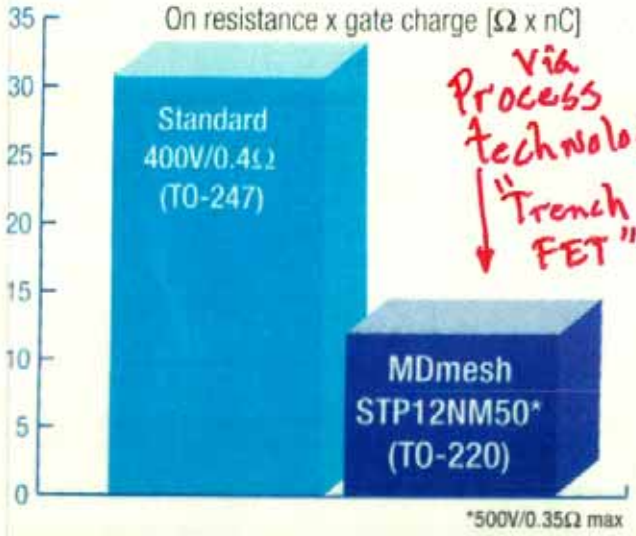


Fig. 3. *Figure of Merit $R_{DS(on)} \times Q_{gd}$ vs. cell density of a conventional PWM Trench MOSFET.*

Will explain soon


nC
SOP Advance MOSFET Ron-Qg Comparison
● = Competing Products
Qg (typ) @ Vds=24V, Vgs=5V [nC]
70
60
50
40
30
20
10
0
Lower Switching Loss
Higher Efficiency
TPCA8004H
TPCA8003H
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
mΩ
Ron (max) @ 4.5V [mOhm]
Lower Conduction Loss
$R_{DS(on)} * Q_g$ want's to be small

MDmesh Cuts R_{on} x Q_g



The MDmesh structure achieves a phenomenal reduction of both on-resistance and gate charge, making it the most suitable switch for high efficiency and high frequency converters.

η for resistive charging

exam 2?

(1) $V_c = V_0(1 - e^{-\frac{t}{RC}})$

(2) $\frac{V_0}{s} \cdot \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{V_0}{s} \cdot \frac{1}{RCs+1}$

$\frac{V_0}{s} \cdot \frac{1}{R + \frac{1}{Cs}} = \frac{V_0}{s} \frac{Cs}{RCs+1} = \frac{V_0 C}{RCs+1}$

(3) $\frac{\left(\frac{V_0 C}{RC}\right)}{s + \frac{1}{RC}}$

(4) $\Rightarrow i = \frac{V_0}{R} e^{-\frac{t}{RC}}$

$$\eta = \frac{\frac{1}{2}CV_0^2}{\frac{1}{2}CV_0^2 + \int_0^\infty i^2 R\,dt}$$

HW

$$\int_0^\infty i^2 R\,dt = \int_0^\infty \left(\frac{V_0}{R} e^{-\frac{t}{RC}}\right)^2 R\,dt$$

$$= \frac{V_0^2}{R} \int_0^\infty e^{-\frac{2t}{RC}}\,dt = \left(\frac{V_0^2}{R}\right)\left(-\frac{RC}{2}\right) \int_0^\infty e^{-\frac{t}{RC}} \left(-\frac{2}{RC}\right) dt$$

$$= \left(\frac{V_0^2}{R}\right)\left(-\frac{RC}{2}\right) e^{-\frac{t}{RC}} \Big|_{t=0}^{t=\infty}$$

$$= -\frac{V_0^2 C}{2}(0 - 1) = \frac{1}{2}CV_0^2$$

$$\eta = \frac{\frac{1}{2}CV_0^2}{\frac{1}{2}CV_0^2 + \frac{1}{2}CV_0^2} = 50\%$$

MOSFET: conclusions

- A majority-carrier device: fast switching speed
- Typical switching frequencies: tens and hundreds of kHz
- On-resistance increases rapidly with rated blocking voltage
- Easy to drive
- The device of choice for blocking voltages less than 500V
- 1000V devices are available, but are useful only at low power levels (100W)
- Part number is selected on the basis of on-resistance rather than current rating

MOSFET: conclusions

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Inside a failed Power MOSFET

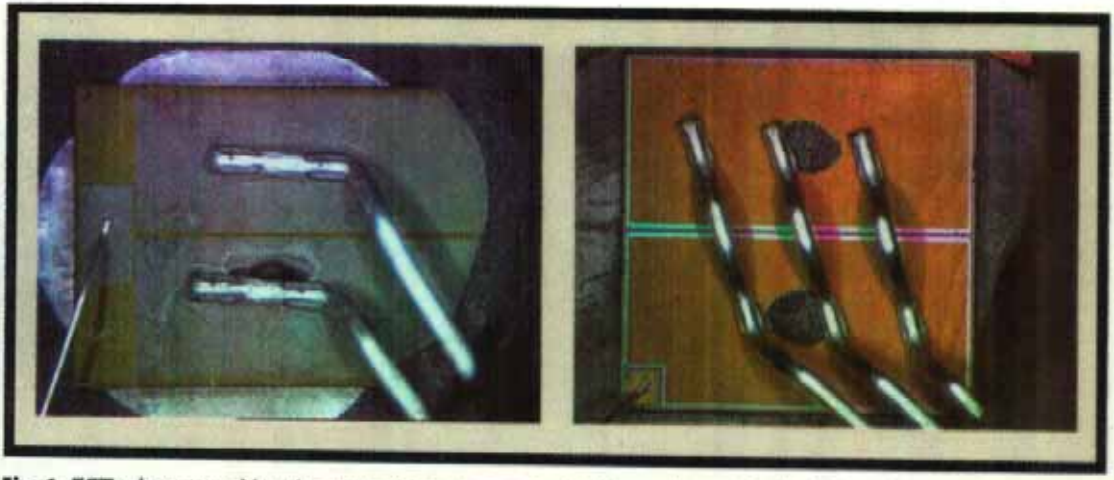


Fig. 6. *FETs destroyed by the capacitor-dump test. Planar is on the left; Trench is on the right. Note the dual damage sites on the trench part.*

You said f_{sw} ↑ better but...

4.3.4. Efficiency vs. switching frequency

$W_{on} \neq W_{off}$ often

Choose diode type to set Q_{rr}

Add up all of the energies lost during the switching transitions of one switching period:

DC loss

$$W_{tot} = W_{on} + W_{off} + W_D + W_C + W_L + \ldots$$

L-C Parasitics

Average switching power loss is

AC loss

$$P_{sw} = W_{tot} f_{sw}$$

$f_s > 500\,kHz$ often the largest term for loss BUT SiC to the rescue

Total converter loss can be expressed as

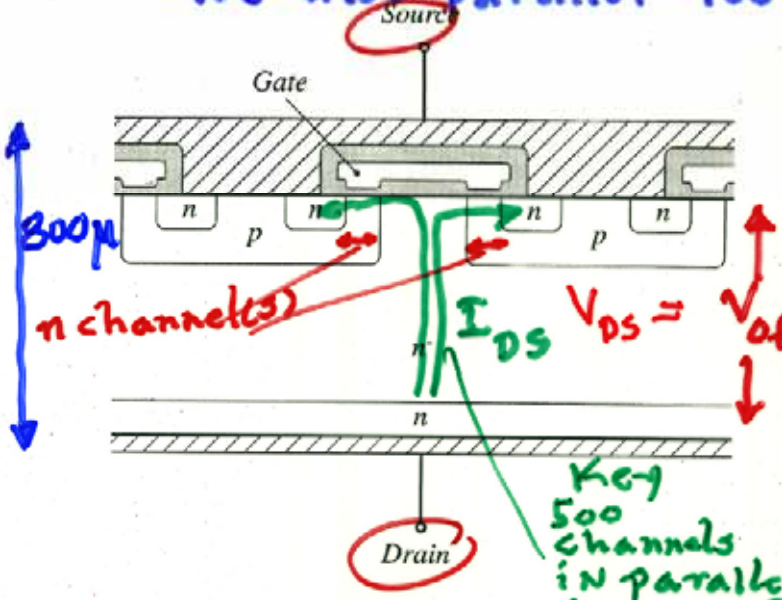
$$P_{loss} = P_{cond} + P_{fixed} + W_{tot} f_{sw}$$

where P_{fixed} = fixed losses (independent of load and f_{sw})
P_{cond} = conduction losses

Fig 4.27 pg 79

4.2.2. The Power MOSFET

This is a verticle structure we also parallel 100 to 1000 of them



- Gate lengths approaching one micron
- Consists of many small enhancement-mode parallel-connected MOSFET cells, covering the surface of the silicon wafer
- Vertical current flow
- n-channel device is shown

11 1000 in a 1-5mm area

Key 500 channels in parallel (microns apart) for low R_{ON}

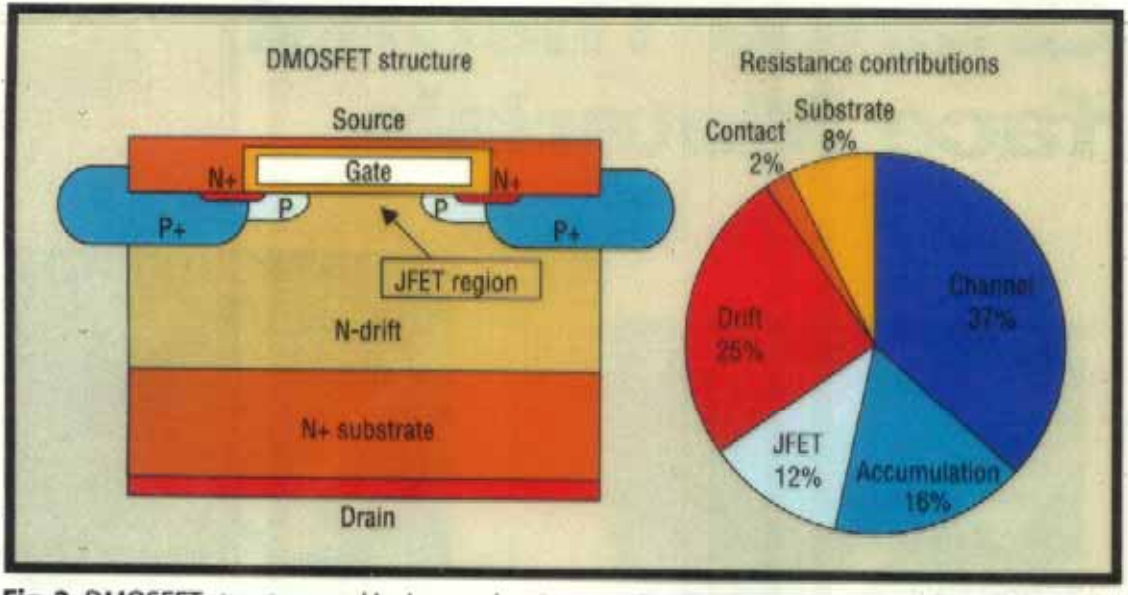


Fig. 2. *DMOSFET structure and its internal resistance distribution.*

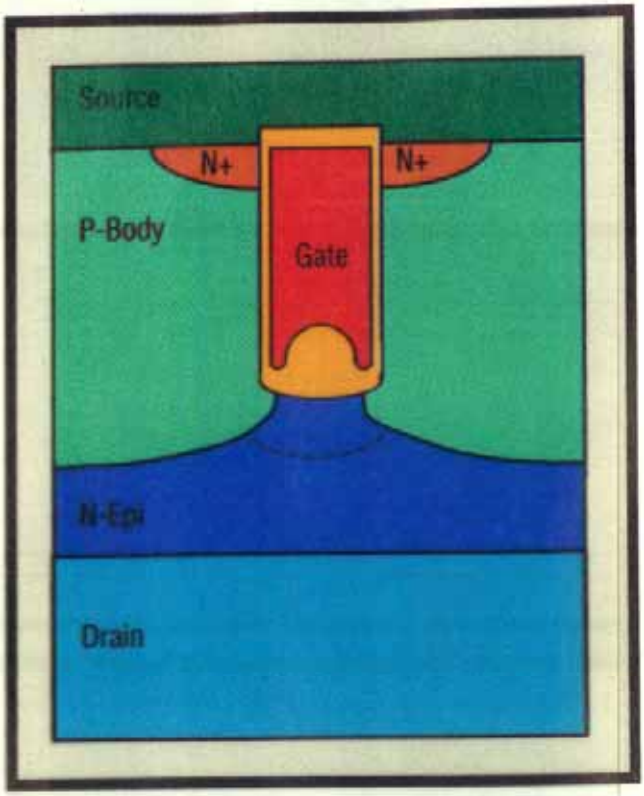


Fig. 4. *Schematic cross section of a W-Gated Trench MOSFET (WFET).*

Conventional Trench MOSFET.

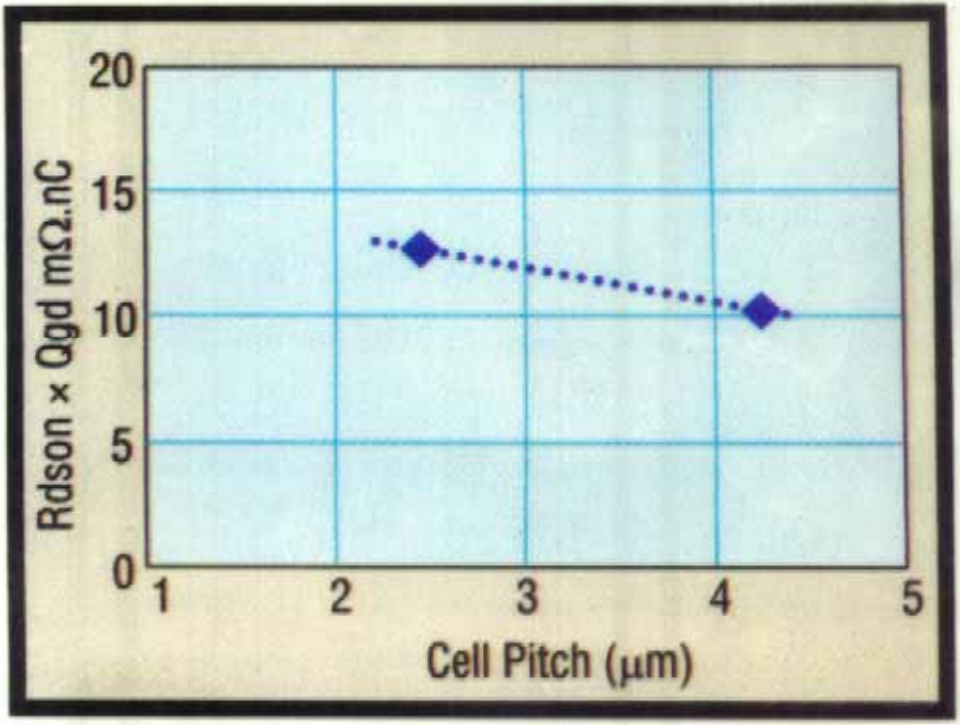


Fig. 7. *Merit $R_{DS(on)} \times Q_{gd}$ vs. cell pitch of a WFET.*

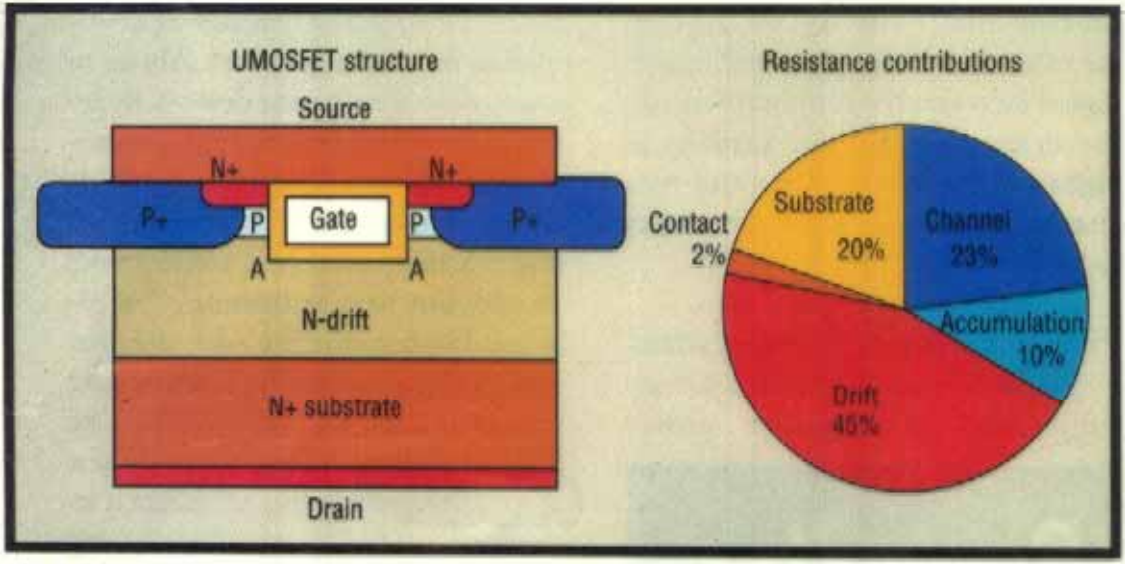
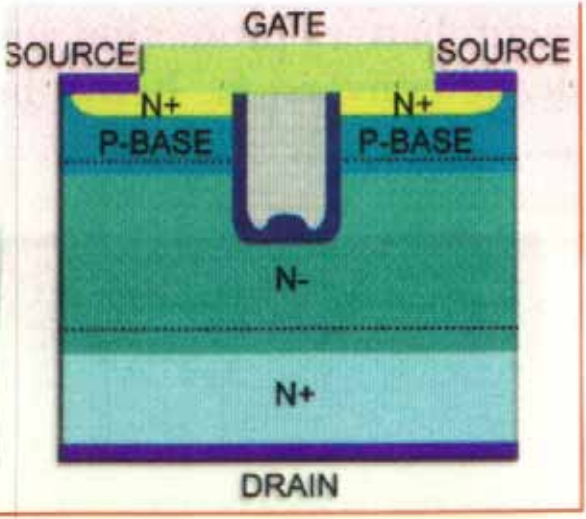


Fig. 3. *Trench of UMOSFET structure and its internal resistance distribution.*



Vishay Siliconix' WFET technology uses a thicker gate oxide at the bottom of the silicon trench to reduce device input capacitance. Additional cell density techniques lower $R_{DS(on)}$.

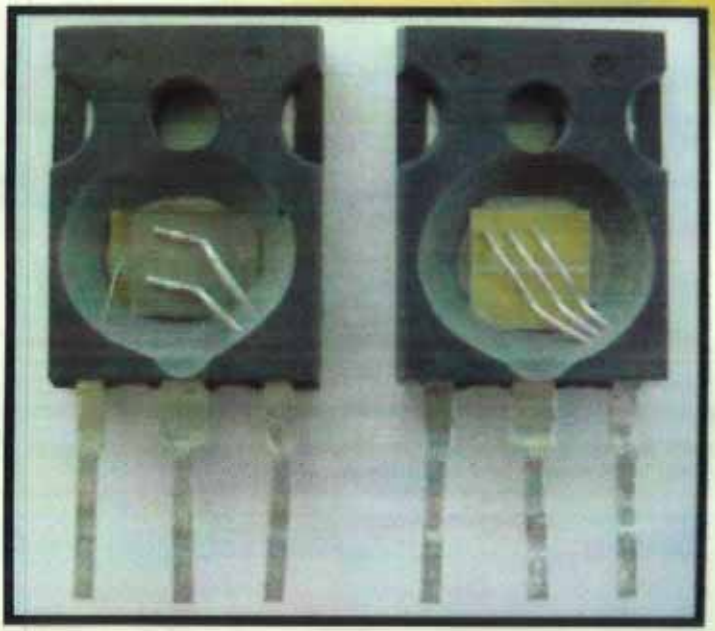
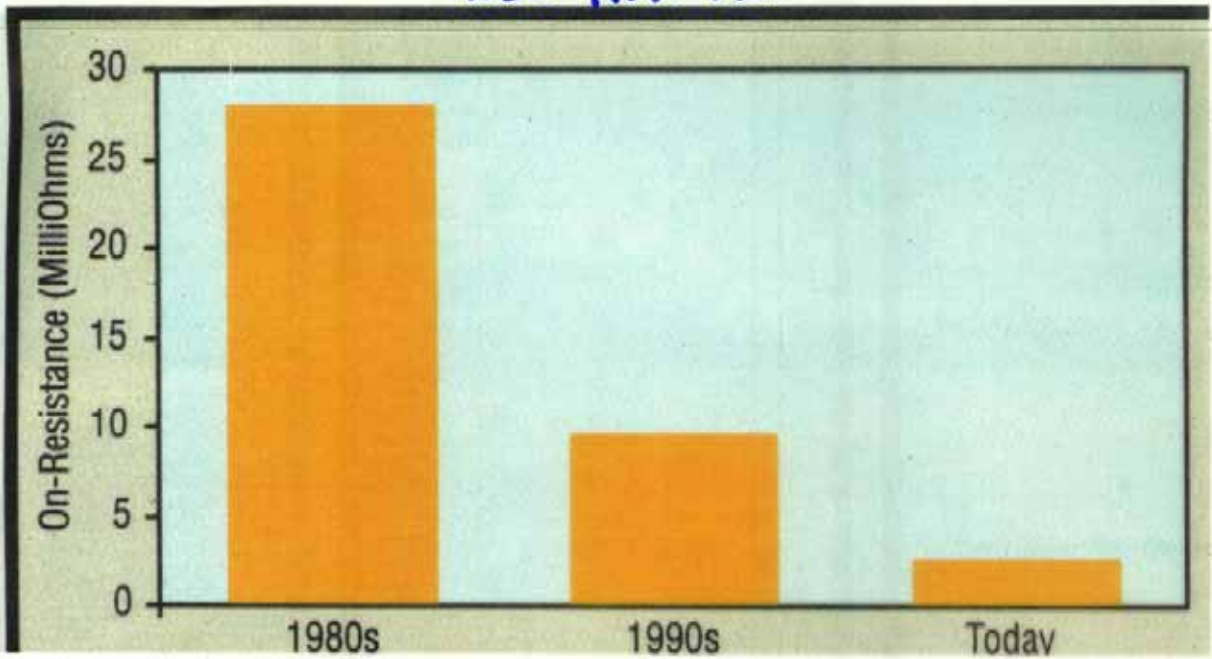


Fig. 1. *Planar (left) and Trench (right) test FETs with their die exposed.*

NEW Power FET



How R_{on} ↓ ?
Yet V_{off} ↑ .

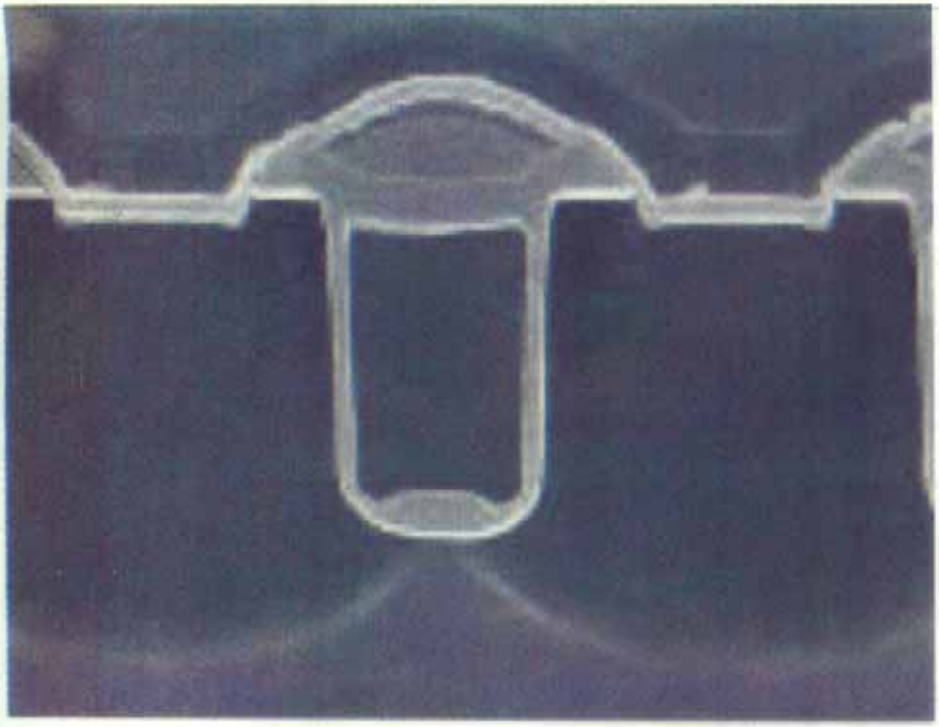


Fig. 5. *SEM cross section of a W-Gated Trench MOSFET WFET.*

	Conventional UMOSFET	WMOSFET	Ratio Conv./WFET
Crss at VDS 0V/30V pf	762/163	207/89	3.7/1.8
Qgd nC	4.5	1.6	2.85
Rds.Qgd mΩ.nC	33.8	12.5	2.7

Table: *Comparison of WFET and conventional trench MOSFET characteristics.*

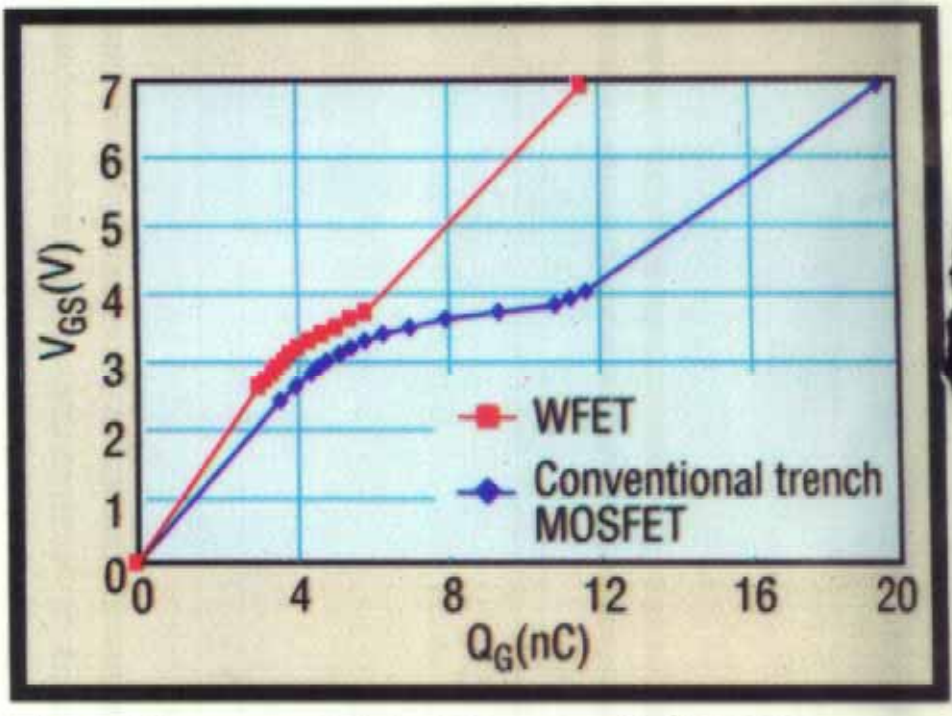


Fig. 6. *Measured Gate Charge of a WFET vs. a Conventional Trench MOSFET.*

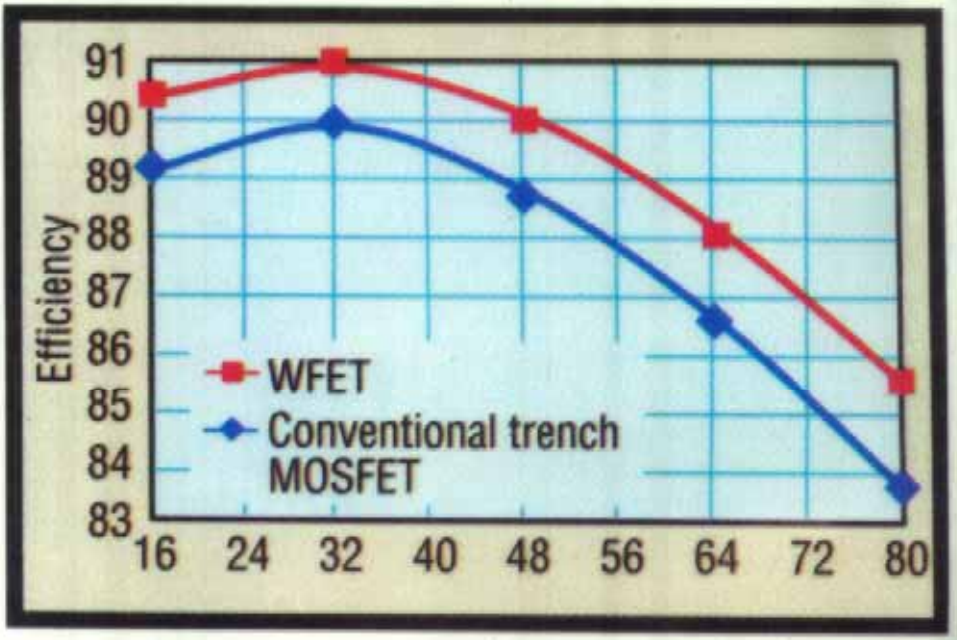


Fig. 9. *Measured efficiency vs. output current for a PWM switch-mode 4-phase dc-to-dc buck converter with 19V V_{IN} and 1.3V V_{OUT}.*

Get R_{DS} and V_{GS} ?
What's clever

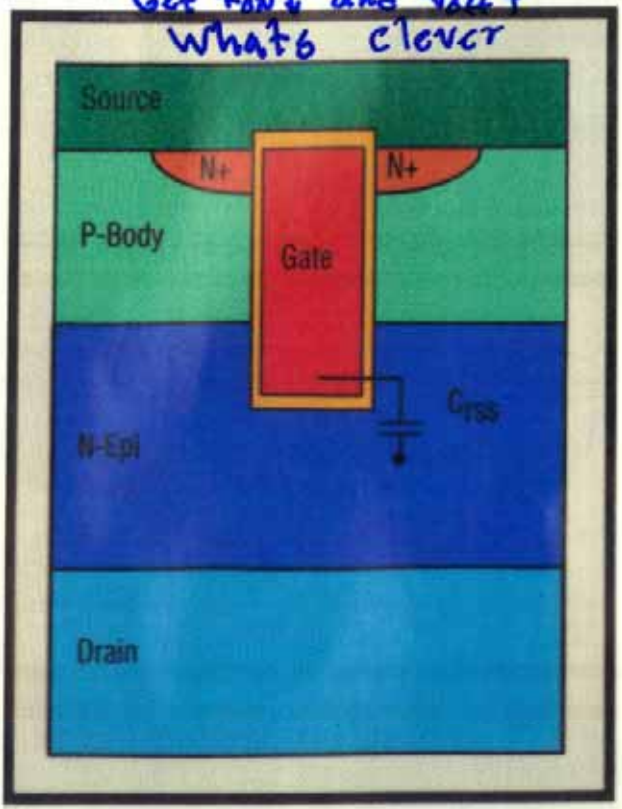


Fig. 2. *Schematic cross section of conventional Trench MOSFET.*