ECE 562

Week 5 Lecture 1

Fall 2008

Week 5 Lecture 1 Summary

- Section notes
  - Slides 3-7 – DC transformers
  - Slides 8-16 – Converter efficiencies
  - Slides 17-21 – Source of losses
  - Slides 22-37 – Overview of loss and efficiency
  - Slides 38-45 – Problem 3.7 homework

Chapter 3. Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

3.1. The dc transformer model

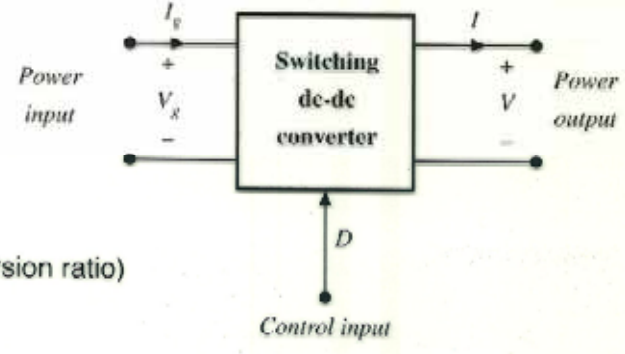
Basic equations of an ideal dc-dc converter:

(1) $P_{in} = P_{out}$

$V_g I_g = V I$ (η = 100%) Key

(2) $V = M(D)\, V_g$

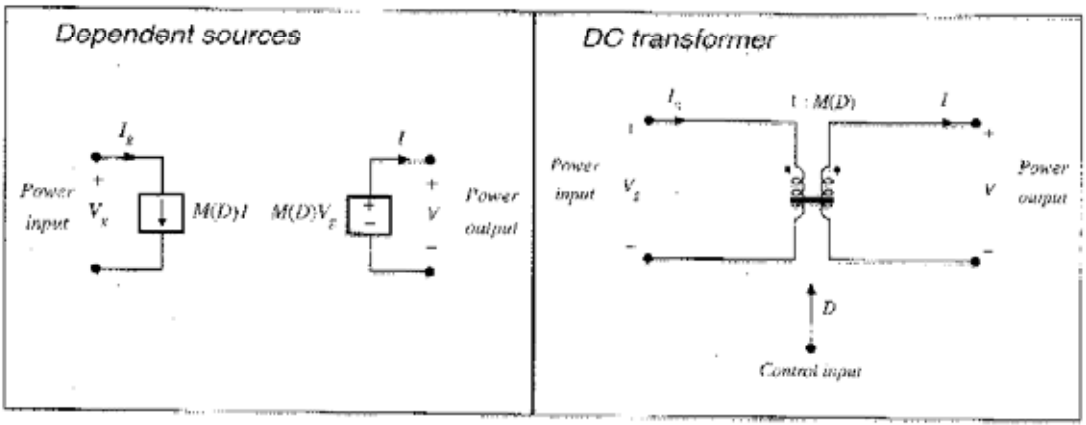
$I_g = M(D)\, I$ (ideal conversion ratio)



These equations are valid in steady-state. During transients, energy storage within filter elements may cause $P_{in} \neq P_{out}$

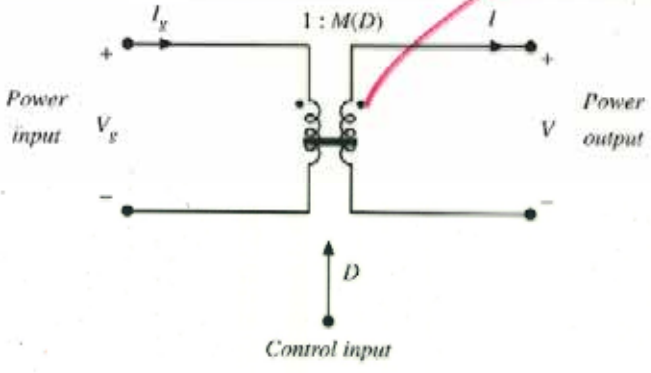
Equivalent circuits corresponding to ideal dc-dc converter equations

$$P_{in} = P_{out} \qquad V_g I_g = V I \qquad V = M(D)\, V_g \qquad I_g = M(D)\, I$$



The DC transformer model

Dot rule ⇒ ?



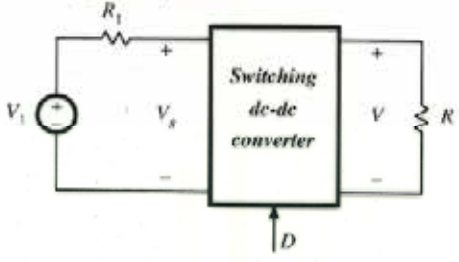
Models basic properties of ideal dc-dc converter:

- conversion of dc voltages and currents, ideally with 100% efficiency
- conversion ratio M controllable via duty cycle

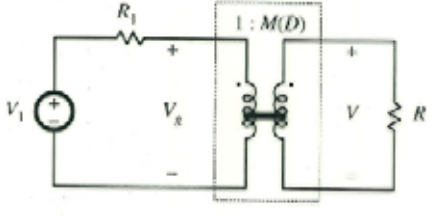
- Solid line denotes ideal transformer model, capable of passing dc voltages and currents
- Time-invariant model (no switching) which can be solved to find dc components of converter waveforms

Example: use of the DC transformer model

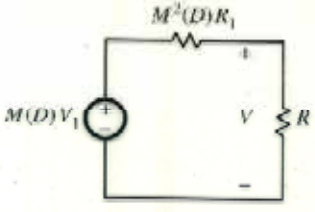
1. Original system



2. Insert dc transformer model



3. Push source through transformer



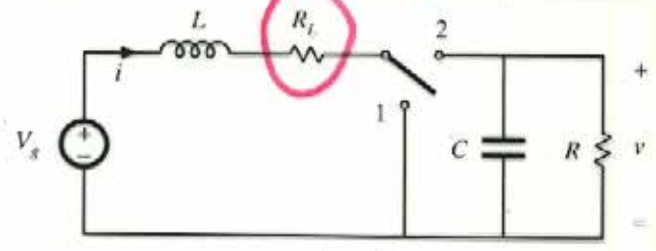
4. Solve circuit

$$V = M(D)\, V_1 \frac{R}{R + M^2(D)\, R_1}$$

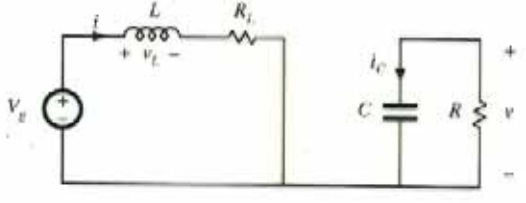
"DC turns ratio" f(D)

Analysis of nonideal boost converter

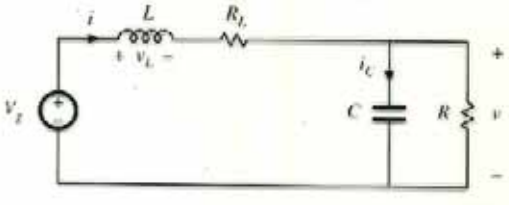
add



switch in position 1



switch in position 2



Inductor voltage and capacitor current waveforms

Average inductor voltage:

$$\langle v_L(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt$$

$$= D(V_g - I R_L) + D'(V_g - I R_L - V)$$

Inductor volt-second balance:

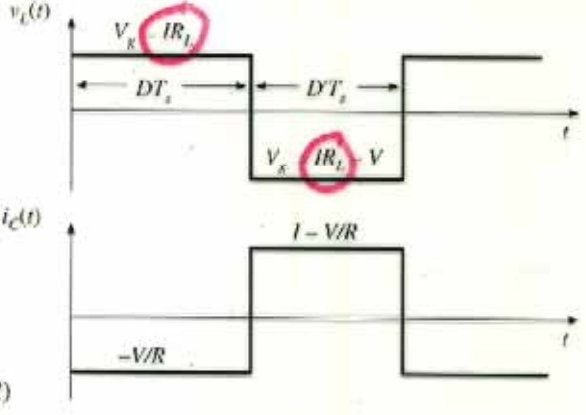
$$0 = V_g - I R_L - D'V$$

Average capacitor current:

$$\langle i_C(t) \rangle = D(-V / R) + D'(I - V / R)$$

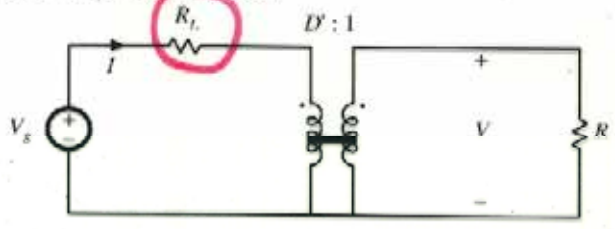
Capacitor charge balance:

$$0 = D'I - V / R$$

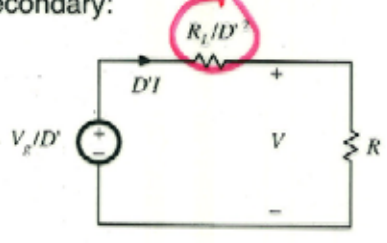


Solution of equivalent circuit

Converter equivalent circuit



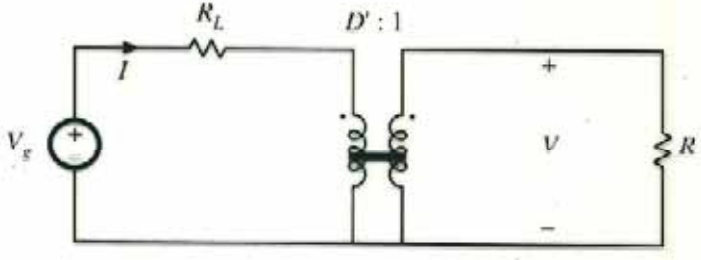
Refer all elements to transformer secondary:



Solution for output voltage using voltage divider formula:

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_L}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

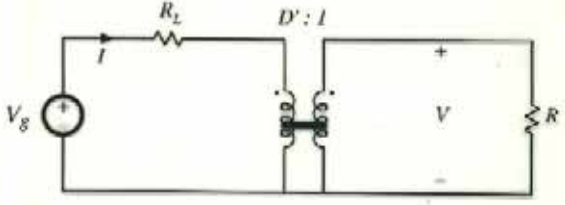
Solution for input (inductor) current



$$I = \frac{V_g}{D'^2 R + R_L} = \frac{V_g}{D'^2} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

trf model

Solution for input (inductor) current



"Average" inductor current

$$I = \frac{V_g}{D'^2 R + R_L} = \frac{V_g}{D'^2} \cdot \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

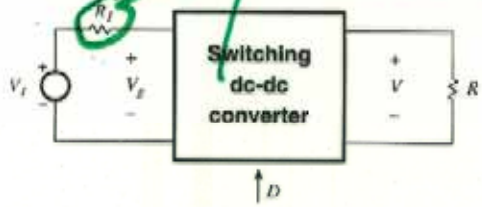
ideal boost

correction factor

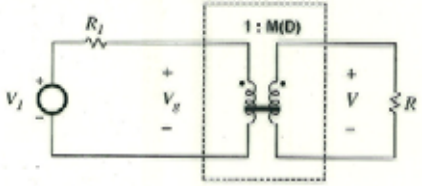
Eq 3.19
pg 48

Example: use of the dc transformer model

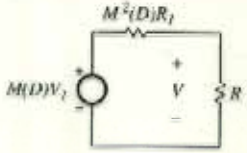
1. Original system



2. Insert dc transformer model



3. Push source through transformer



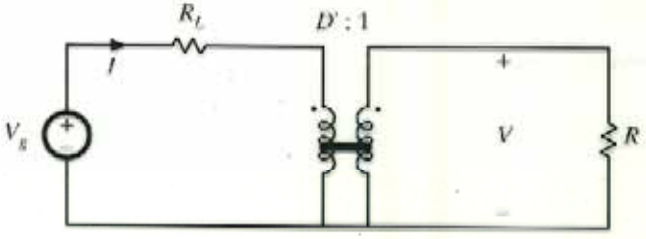
4. Solve circuit

$$V = M(D)\,V_1 \quad \frac{R}{R + M^2(D)\,R_1}$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$



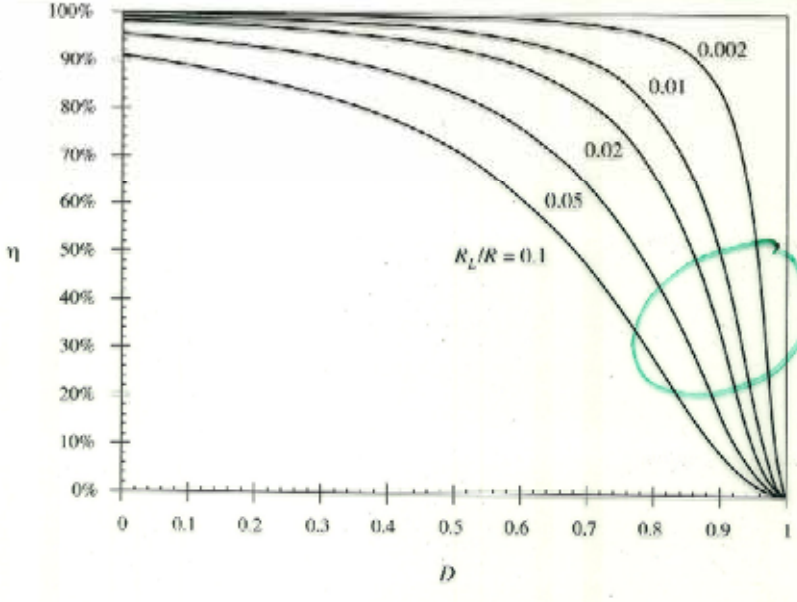
$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V)\,(D'I)}{(V_g)\,(I)} = \frac{V}{V_g}\,D'$$

$\neq 100\%$

$$\eta = \frac{1}{1 + \dfrac{R_L}{D'^2\,R}}$$

Efficiency, for various values of R_L

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}}$$



Solution for output voltage

We now have two equations and two unknowns:

$$0 = V_g - I R_L - D'V$$

$$0 = D'I - V / R$$

Eliminate I and solve for V:

$$\frac{V}{V_g} = \frac{1}{D'} \frac{1}{(1 + R_L / D'^2 R)}$$

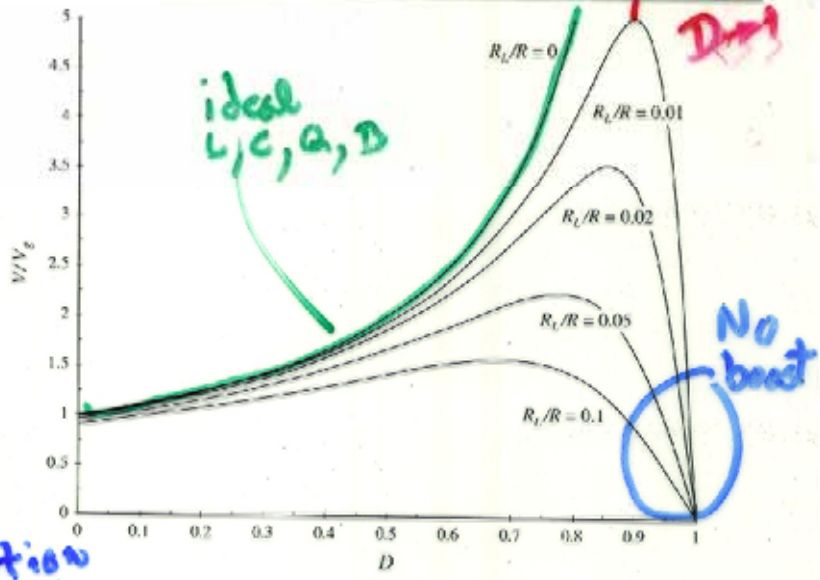


Fig 3.9 p45

Solution for output voltage

lossy buck No $\neq 10 V_g$ possible

We now have two equations and two unknowns:

$$0 = V_g - I R_L - D'V$$

$$0 = D'I - V / R$$

Eliminate I and solve for V:

$$\frac{V}{V_g} = \frac{1}{D'} \frac{1}{(1 + R_L / D'^2 R)}$$

Ch3

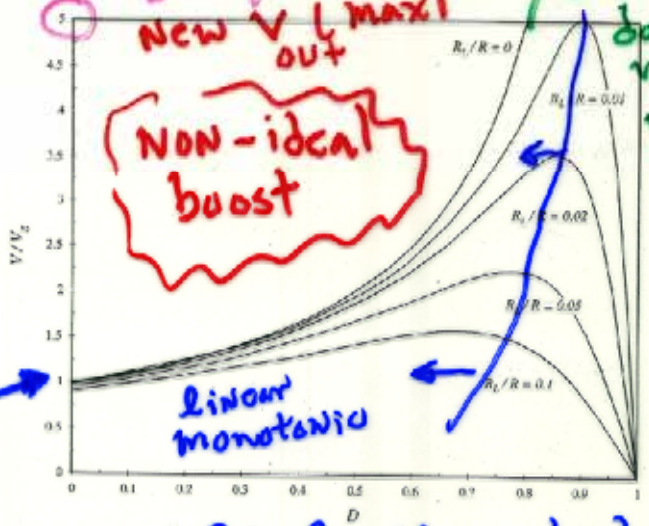
ideal Ch2

Usual boost lower limit

R_L = Load R / 100

NEW V_{out} (max)

NON-ideal boost



linear monotonic

double value V_{out}

V(D) is double valued

HW3.8 what D is highest efficiency

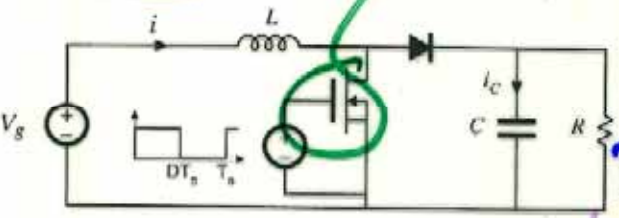
Pg52

3.5. Example: inclusion of semiconductor conduction losses in the boost converter model

Losses are?

Boost converter example

Fig 3.22 Pg 52



Typical FET:

R_{ON} (lowest) 30 mΩ

100 A ⇒ V_{ON} = 3V

Models of on-state semiconductor devices:

1. MOSFET: on-resistance R_{on}
2. Diode: constant forward voltage V_D plus on-resistance R_D

Insert these models into subinterval circuits

Two components

V_D R_{ON} = f(D)

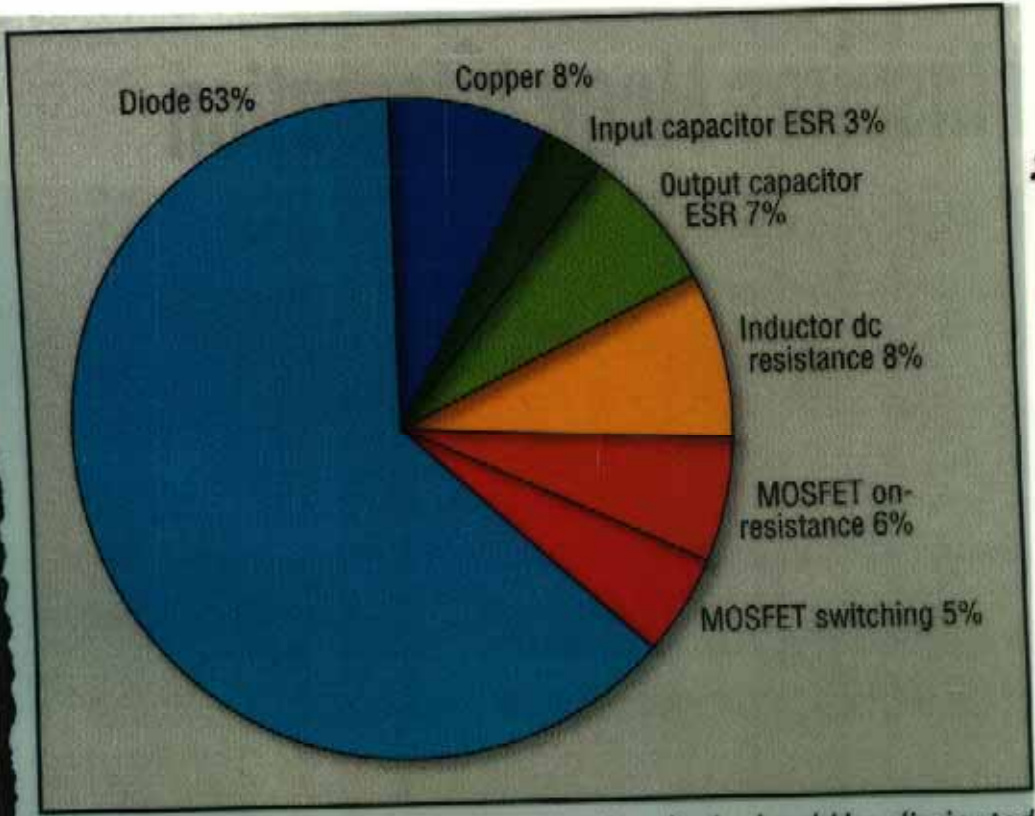


Fig. 6. *Power loss caused by the freewheeling diode should be eliminated to increase the converter's efficiency.*

Losses in a typical buck

Chapter 3

replace D with?

All losses are f(D), f_{sw} etc

Chapter 3. Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

DC only

Not simply $I^2 R_{CU}$ (wire) also f(D)!

3.1. The dc transformer model

3.2. Inclusion of inductor copper loss

3.3. Construction of equivalent circuit model

3.4. How to obtain the input port of the model

3.5. Example: inclusion of semiconductor conduction losses in the boost converter model

3.6. Summary of key points

DC Losses
① FET Sw
② diode

Ch 5 P_{loss} (switch) = $E_{switch} * f_{sw}$

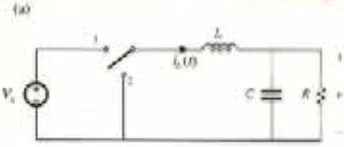
Summary of chapter 3

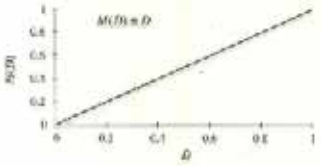
1. The dc transformer model represents the primary functions of any dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, and control of the conversion ratio M via the duty cycle D. This model can be easily manipulated and solved using familiar techniques of conventional circuit analysis.
2. The model can be refined to account for loss elements such as inductor winding resistance and semiconductor on-resistances and forward voltage drops. The refined model predicts the voltages, currents, and efficiency of practical nonideal converters.
3. In general, the dc equivalent circuit for a converter can be derived from the inductor volt-second balance and capacitor charge balance equations. Equivalent circuits are constructed whose loop and node equations coincide with the volt-second and charge balance equations. In converters having a pulsating input current, an additional equation is needed to model the converter input port; this equation may be obtained by averaging the converter input current.

Three basic dc-dc converters

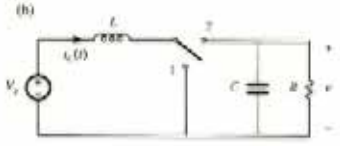
Lossless: f_{sw} ↑ $|I_L|$ ↓ why?

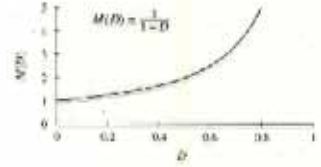
Buck



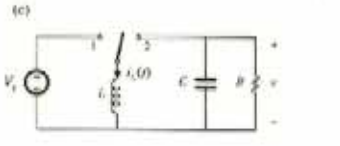


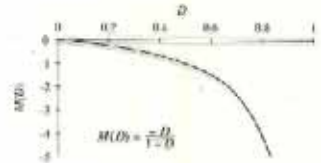
Boost





Buck-boost





f_{sw} ↑ efficiency ↓ Why?

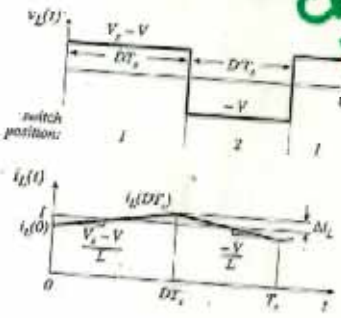
Ch 3 $\eta = f(D)$!

Part I. Converters in equilibrium

Overview of Loss & Efficiency

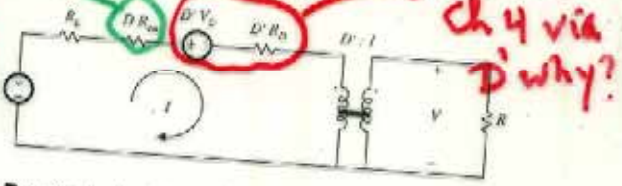
Tr Sw loss on DC basis

Inductor waveforms



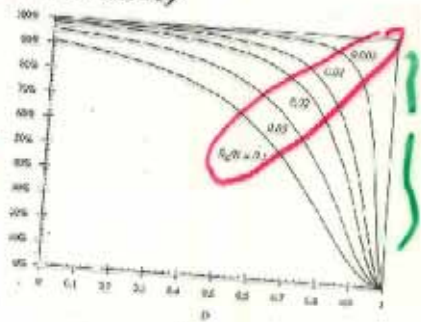
Ch 4 via D why?

Averaged equivalent circuit



diode loss Ch 4 via D' why?

Predicted efficiency



Now $\eta(D)$

Discontinuous conduction mode — Ch 5

Transformer isolation — Ch 6

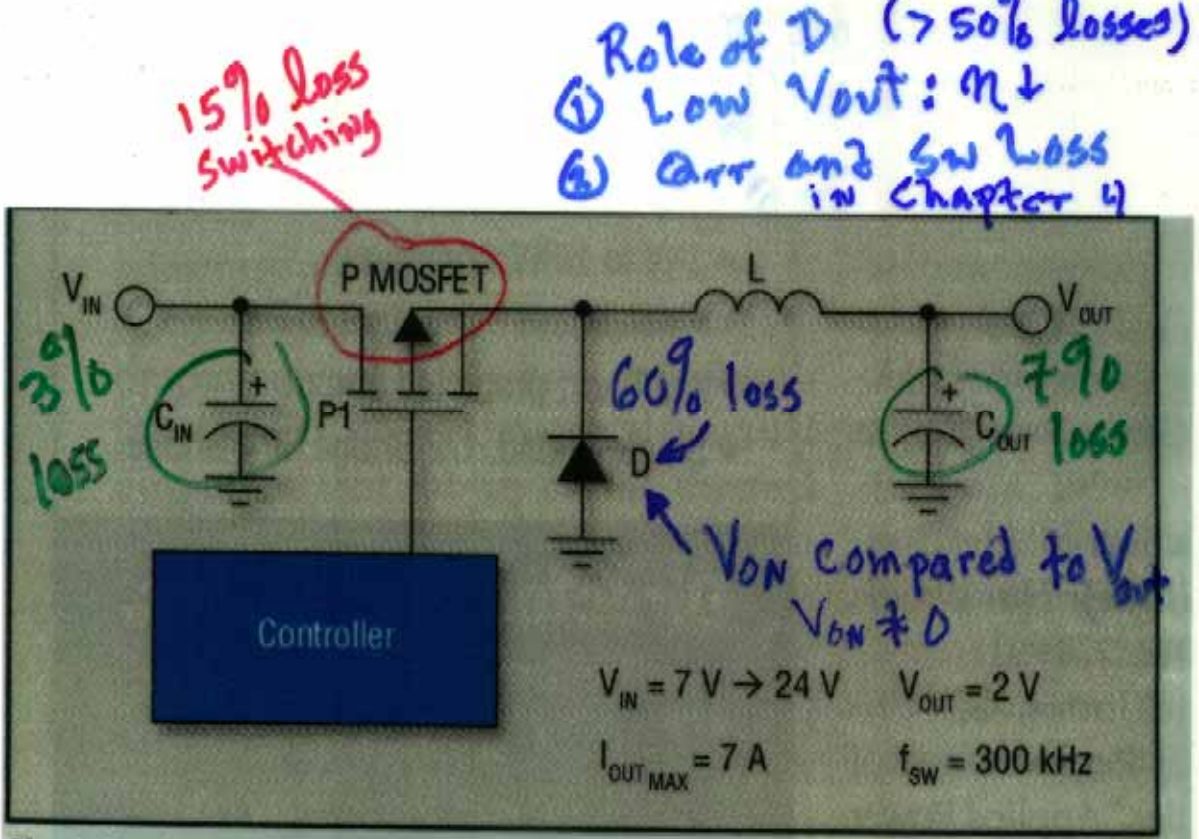


Fig. 1. *Basic stepdown converter circuit with operating parameters.*

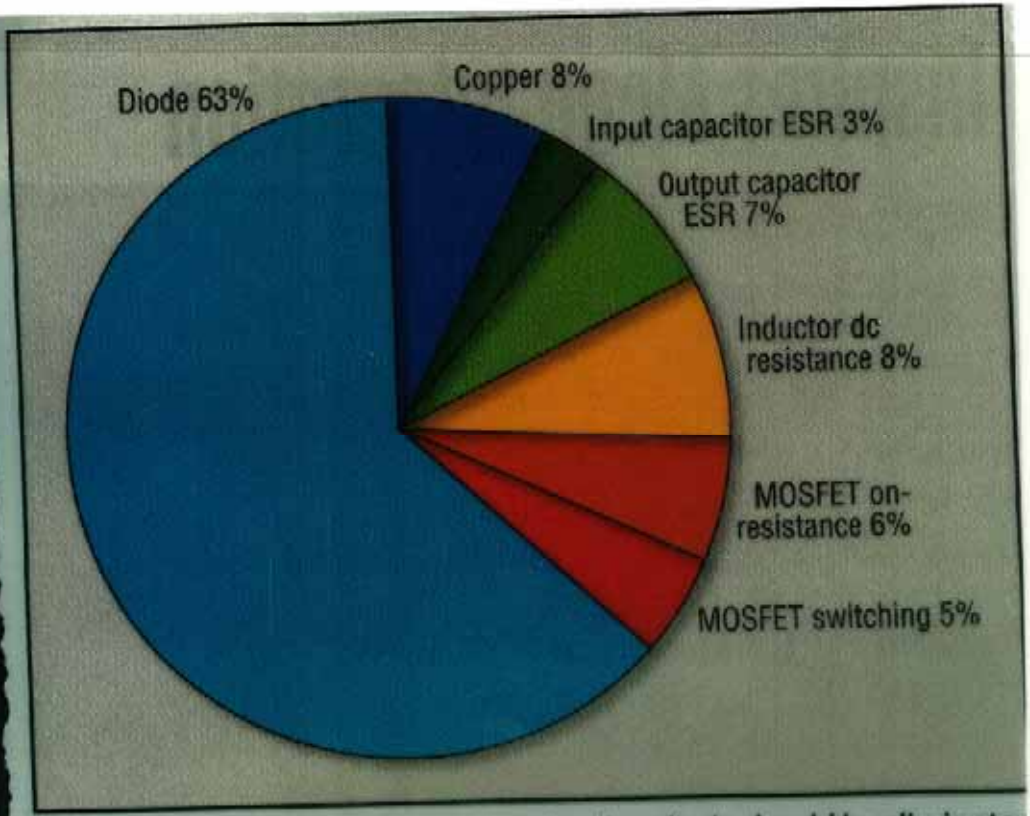
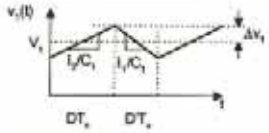


Fig. 6. *Power loss caused by the freewheeling diode should be eliminated to increase the converter's efficiency.*

Use the I_1 waveforms and integrate:



$$\Delta v_{C1} = \frac{I_2}{C_1} DT_s \left(\frac{1}{2}\right)$$

Now from DC analysis:

$$I_2 = \frac{V_2}{R} \text{ and } V_2 = \frac{-D}{D'} V_g \Rightarrow I_2 = \frac{-D\,V_g}{D'\,R}$$

$$\Delta v_{C1} = \frac{V_g D^2 T_s}{2D'RC_1}, \text{ so } C_1(\text{spec}) = \frac{V_g D^2 T_s}{2\Delta v_{C1} RC_1}$$

Start Ch3

III. Static and Dynamic Switch Loss in Real Converters

A. General Switch Issues

Clearly voltage drops across the energy storage inductor, V_L, differ in lossless vs. lossy converters.). The equivalent series resistance of inductors and capacitors add losses. In lossy converters efficiency is then a function of load current ,I_L while in lossless converters it is not . Also, s_u and s_d of di/dt in the inductor for lossless converters will not be equal to that of lossy converters. Hence, M(D) changes from the lossless case and becomes M(d, losses)

losses in C, L OK?

Switch devices also introduce losses. Thus, for example a diode alone adds both $V_D(on) + I_{on}R_D$ and this changes V_L as well as s_d slope.

Consider both DC and RMS currents and their static effects but neglecting dynamic switching losses:..

1. Static or Non-switching power losses:

Reactive elements:

•Capacitors •Inductors on cores

In practice parasitic R, L, and C components arising often make up half the circuit model components though they do not appear on the bill of lading. BOM ea Parasitic

Resistance effects include:

- R_L of the inductor windings including skin effects.
- R_{sw} of the double-pole, double-throw switch devices from device characteristics such as R_{on} of the transistor or R_{on} of the diode.
- ESR of all capacitors = $R_{sr} + \frac{1}{w^2 R_{leak} C^2}$
- ESR effects for L

These may appear in input or output circuits depending on converter topology and cause loss of power efficiency, η, from the ideal case where they are neglected.

Unique to SW choice eg diode: $V_{D(on)}$ and $R_{D(on)}$

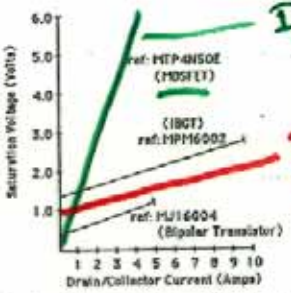
- Switch Device effects
  For example V_{on} and R_{on} of semiconductor devices. See Chapter 5 of Erickson's text

•MOSFET's •IGBT's •diodes
•GTO (Gate turn-off Thyristor)
•MCT (MOS-Controlled Thyristor)

Below we show the V_{on} three switches:for MOSFET(highest value, for the IGBT, and for the BJT(lowest value).

Consider

load up to 10KW



Comparison of saturation voltages between MOSFETs, bipolar power transistors, and IGBTs.

$I_{ON} R_{ON}$ + $I_{ON} V_{ON}$ MOSFET

Bipolar low V_{ON} .3V @ 100A only 30W

95% ⇒ 1KW heat

$$\eta = \frac{P_o}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}};$$

typically $85 < \eta < 95\%$

85% ⇒ 3KW heat

$I^2_{RMS} R$

Both resistive and device losses contribute to loss of efficiency. In summary, wire resistance: $I_L^2 R_L$ and $I_{RMS} \neq I_{AV}$ device losses due to V_{on} of the diode and R_{on} (transistor)

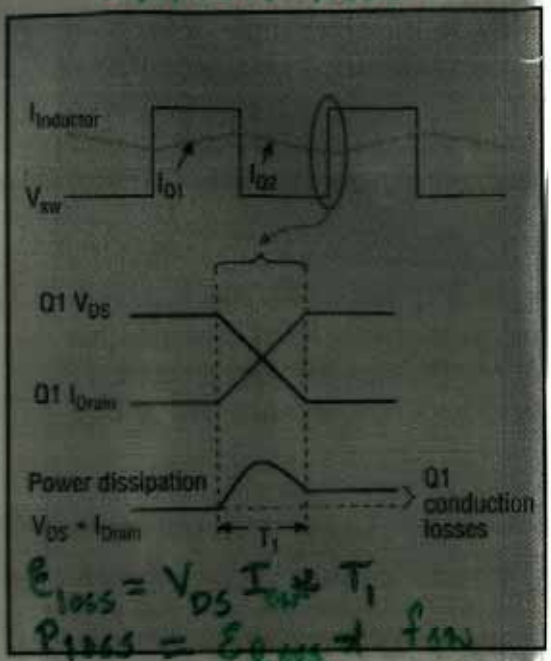
a. Diode V_{on} is fixed at ≈ 2V and $P_D(sw) = I_D V_{on}$
(usually R_{on} of a diode is negligible)

b. Transistor $R_{on}(I)$ or fixed and $P_{tr} = I_D^2 R_{on}$
(usually V_{on} of a diode is negligible)

not I_{AV}

On the next page we show the two extreme switch conditions: cutoff and saturation.

Switch loss



$E_{loss} = V_{DS} I_{sw} * T_1$

$P_{loss} = E_{loss} * f_{sw}$

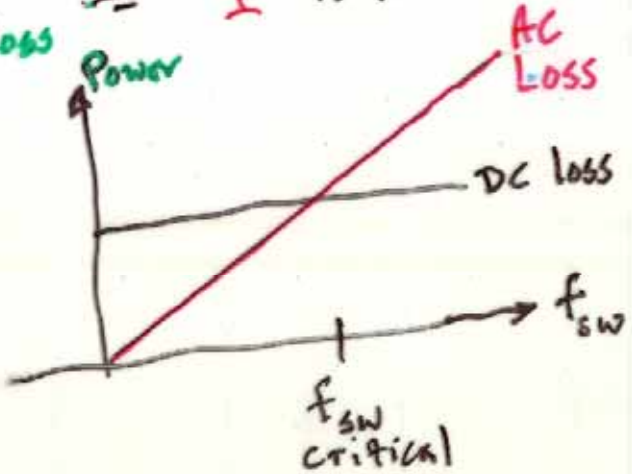
Fig. 2. *In the synchronous buck converter, when Q1 is ON the voltage across it is close to zero, and Vsw is high. When Q1 is OFF, the voltage across it is almost Vin, and Vsw is low. During the switching transition region T1, the voltage and current changes across Q1 result in the*

DC loss Switches: $I_{ON}^2 R_{ON}$ or $I_{ON} V_{ON}$ $\Big\} P^{DC}$

Switching loss:

$$\mathcal{E}(\text{switch}) * f_{SW} = P^{SW}_{loss}$$

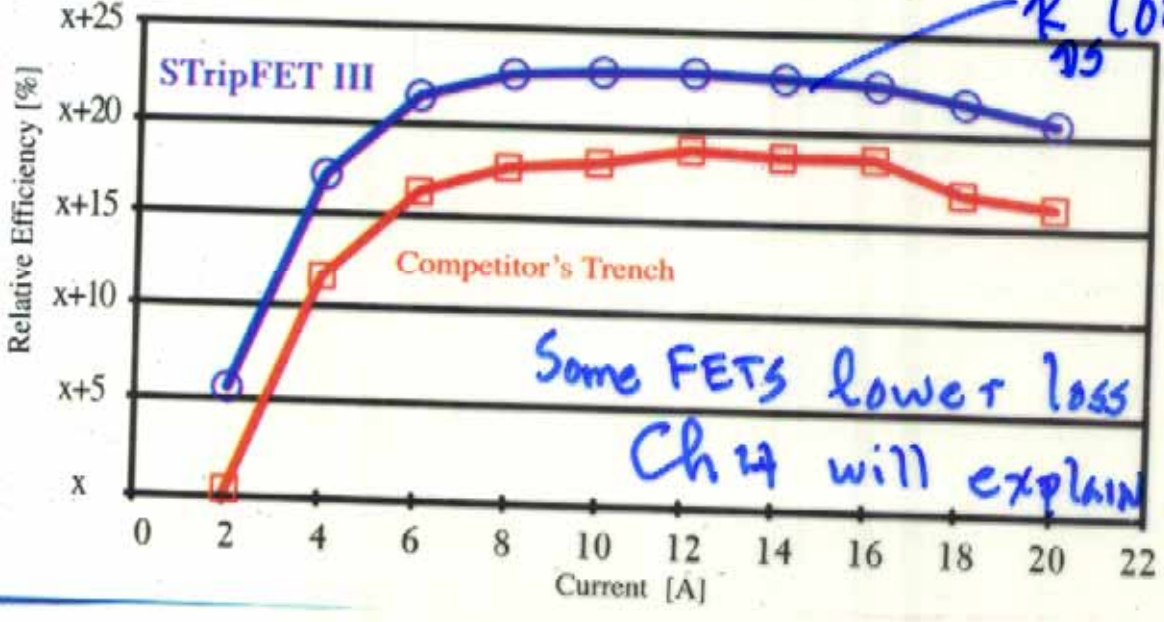
$$P^{total}_{loss} = P^{SW} + P^{DC}$$



Ch4

RELATIVE EFFICIENCY AT 500KHZ

- SINGLE PHASE VIN=12V VOUT=2V



Boost converter example: circuits during subintervals 1 and 2

DC switch loss only !

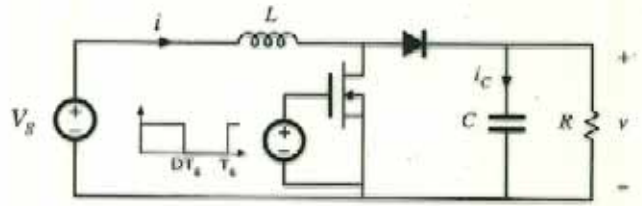
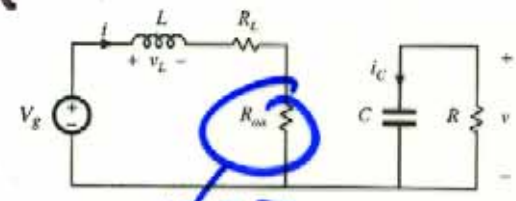


Fig 3.23 p53

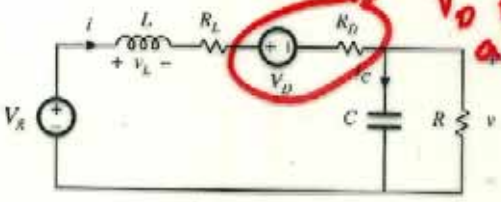
switch in position 1

switch in position 2

diode V_D for all I



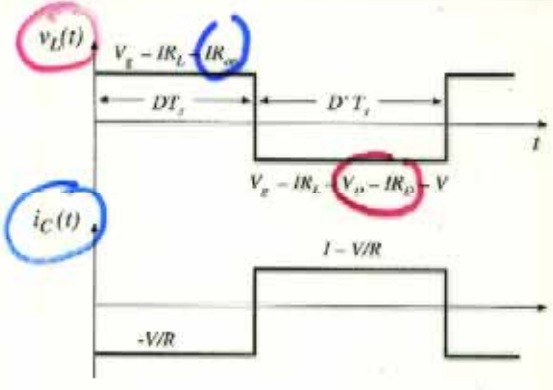
FET: $R_{DS(on)}$



AC sw. loss Ch 4

Average inductor voltage and capacitor current

Fig 3.24
P 53



$$\langle v_L \rangle = D(V_g - IR_L - IR_{on}) + D'(V_g - IR_L - V_D - IR_D - V) = 0$$

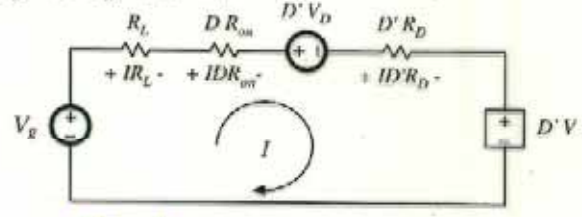
$$\langle i_C \rangle = D(-V/R) + D'(I - V/R) = 0$$

Fig 3.25 / 3.26 pg 54

Construction of equivalent circuits

$\langle v_L \rangle = 0$ Input Circuit Loop

$$V_g - IR_L - IDR_{on} - D'V_D - ID'R_D - D'V = 0$$



$\langle i_C \rangle = 0$

Output Loop

$$D'I - V/R = 0$$

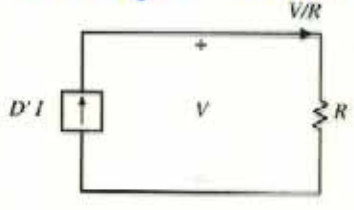
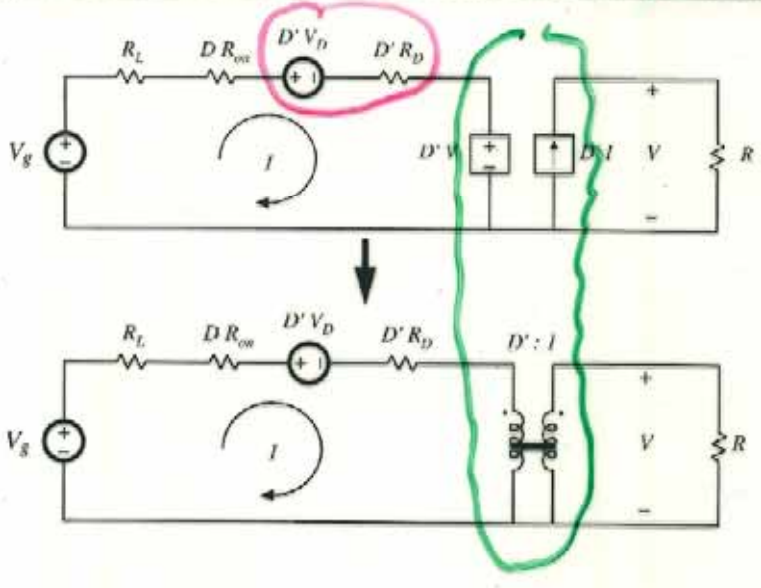


Fig 3.27 / 3.28
P55

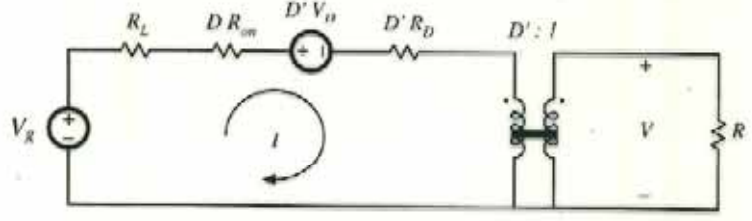
Complete equivalent circuit

Combine both loops together



Solution for output voltage

Fig 3.28



diode losses

$$V = \left(\frac{1}{D'}\right)\left(V_g - D'V_D\right)\left(\frac{D'^2R}{D'^2R + R_L + DR_{on} + D'R_D}\right)$$

$$\frac{V}{V_g} = \left(\frac{1}{D'}\right)\left(1 - \frac{D'V_D}{V_g}\right)\left(\frac{1}{1 + \frac{R_L + DR_{on} + D'R_D}{D'^2R}}\right)$$

Eq 3.34

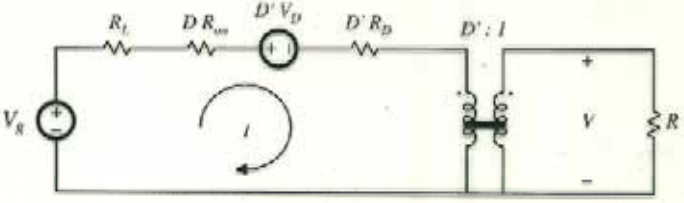
ideal boost

switch loss corrections

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$



$$\eta = D'\frac{V}{V_g} = \frac{\left(1 - \frac{D'V_D}{V_g}\right)}{\left(1 + \frac{R_L + DR_{on} + D'R_D}{D'^2R}\right)}$$

Only DC losses
No switch loss

Conditions for high efficiency: ← Battery Operated Boost

$$V_g / D' >> V_D$$

and $$D'^2R >> R_L + DR_{on} + D'R_D$$

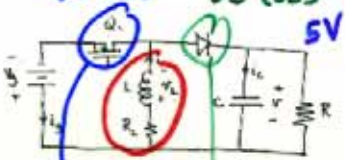
1.5V Alkaline
up to 5V

Problem 3.7 : Tutorial Solution

DC loss

DC loss ($No\ I_D R_{D(on)}$)

5V

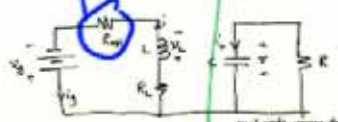


$R = \frac{5V}{1A} = 5\,\Omega$

f_s = switch
L = inductor
C = big
V_g = 1.5V
R_{on} = 35 mΩ
V_D = 0.5V
R_L = ?

a) Circuit equivalent circuit

when transistor Q1 conducting $0 < t < DT_s$



most simple approximation

$v_L = V_g - i R_L - i R_{on} \approx V_g - I R_L - I R_{on}$

$i_c = -\frac{v}{R} \approx -\frac{V}{R}$

$i_g = i \approx I$

when diode conducting $DT_s < t < T_s$

$v_L = -V - i R_L - V_D \approx -V - I R_L - V_D$

$i_c = i - V/R \approx I - \frac{V}{R}$

$i_g = 0$

Next week practical R L C

Choose to achieve $\eta = 90\%$

Inductor volt-second balance: $\langle v_L \rangle = 0 = D\left(V_g - IR_L - IR_{on}\right) + D'\left(-V - IR_L - V_b\right)$

Capacitor charge balance: $\langle i_c \rangle = 0 = D\left(-\frac{V}{R}\right) + D'\left(I - \frac{V}{R}\right)$

Average input current: $\langle i_g \rangle = I_g = D(I) + D'(0)$

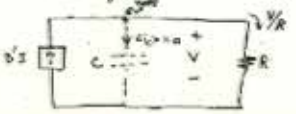
Construct equivalent circuits

Inductor equation: $\langle v_L \rangle = 0 = DV_g - IR_L - DIR_{on} - D'V - D'V_b$ (note $D + D' = 1$)

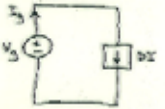
a loop equation

Capacitor equation: $\langle i_c \rangle = 0 = D'I - \frac{V}{R}$

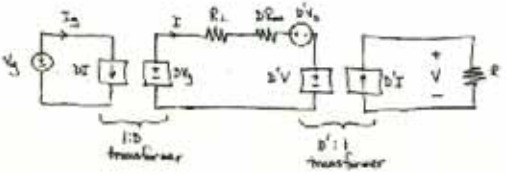
a node equation

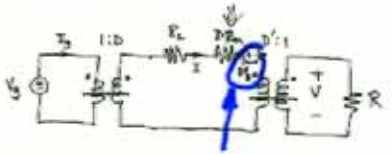


Input port equation: $I_g = DI$ = current flowing out of V_g source

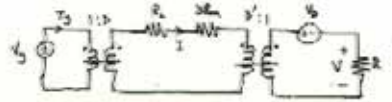


Combine the three circuits:





Can push the $D'V_D$ source through the $D':1$ transformer:



$|V_D|$ insight on η

The diode forward voltage drop V_D is effectively in series with the load, and directly reduces V. To obtain an efficient converter, we require $V_D \ll V$.

b) Choose R_m such that $\eta = 0.70$ when $V_g = 12V$, $V = 5V$,
$V_D = 0.5V$, $R = 5\Omega$, $R_m = 0.035\Omega$

Efficiency:

use circuit model —

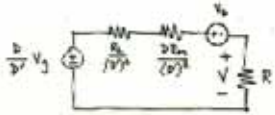
$P_{in} = V_g I_g = V_g \cdot (DI)$

$P_{out} = V \cdot D'I$

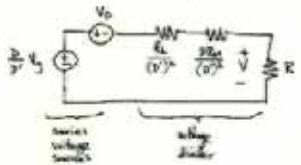
$\Rightarrow \eta = P_{out}/P_{in} = \frac{V}{V_g} \frac{D'I}{DI} = \frac{D'}{D} \frac{V}{V_g}$

Solve model for $\frac{V}{V_g}$

Push all elements to output side of converter (through dc transformers). Model becomes



Push V_0 source to left:



L&C without ESR do not dissipate any power - No effect on efficiency here

Solution of circuit:

$$V = \underbrace{\left(\frac{D}{D'}V_g - V_0\right)}_{\text{series voltage sources}} \underbrace{\frac{R}{R + \frac{R_1}{(D')^2} + \frac{DR_{on}}{(D')^2}}}_{\text{voltage divider ratio}}$$

algebra

So

$$\frac{V}{V_g} = \left(\frac{D}{D'}\right) \frac{\left(1 - \frac{D'V_0}{DV_g}\right)}{\left(1 + \frac{R_1}{(D')^2 R} + \frac{DR_{on}}{(D')^2 R}\right)}$$

diode DC

FET DC

Ch2 ideal

Key Ch3 Real

Hence, the efficiency is

$$\eta = \frac{D'}{D}\frac{V}{V_g} = \frac{\left(1 - \frac{D'V_D}{DV_g}\right)}{\left(1 + \frac{R_L}{(D')^2R} + \frac{DR_{on}}{(D')^2R}\right)} \qquad (i)$$

and $\frac{V}{V_g} = \frac{2}{D'}\eta$ (ii)

Now, we want $\eta = 0.7$ when $V = 5$ and $V_g = 15$

There are two equations and two unknowns:

Equations (i) and (ii) above

Unknowns R_L and D

The easiest way to solve these equations is to first solve (ii) for D:

$$\frac{V}{V_g} = \frac{D}{1-D}\eta \Rightarrow \left(1-D\right)\left(\frac{V}{V_g}\right) = D\eta$$

$$\Rightarrow \frac{V}{V_g} = D\left(\eta + \frac{V}{V_g}\right)$$

$$\Rightarrow D = \frac{\left(\frac{V}{V_g}\right)}{\eta + \left(\frac{V}{V_g}\right)} = \frac{\left(\frac{5}{15}\right)}{0.7 + \frac{5}{15}} = 0.526$$

We can now solve (i) for R_L: for $\eta = 90\%$

$$1 + \frac{R_L}{D'^2R} + \frac{DR_{on}}{D'^2R} = \frac{\left(1 - \frac{D'V_D}{DV_g}\right)}{\eta}$$

$$\Rightarrow R_L = D'^2R\cdot\left[\frac{1}{\eta} - \frac{D'V_D}{DV_g\eta} - 1 - \frac{DR_{on}}{D'^2R}\right]$$

$$= (1-0.526)^2(5\,\Omega)\left[\frac{1}{0.7} - \frac{(1-0.526)(0.5)}{(0.526)(15)(0.7)} - 1 - \frac{(0.526)(0.185\,\Omega)}{(1-0.526)^2(5\,\Omega)}\right]$$

$$= 21\,m\Omega$$

c) Compute power loss in each element

Use equivalent circuit model (derived in part a)

Loss in inductor winding resistance $= I^2 R_L$

Note $I = \frac{V}{D'R} = \frac{(5V)}{(1-0.32)(5\Omega)} = 5.75A$

so $I^2 R_L = 0.69\,W$ ← Comparable to other loss

Loss in mosFET on-resistance $= I^2 D R_{on}$

$= 0.95W$

Loss in diode forward voltage drop $= \left(\frac{V}{R}\right) V_D$

$= 0.5W$

check: $P_{out} = (5V)(1A) = 5W$

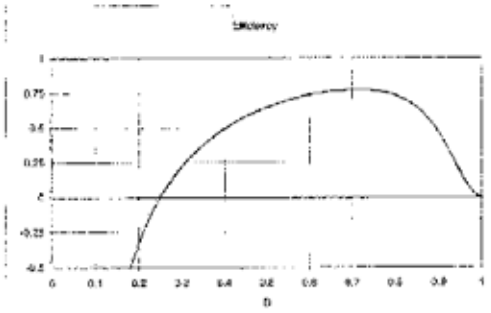
$P_{loss} = (0.69W) + (0.95W) + (0.5W)$

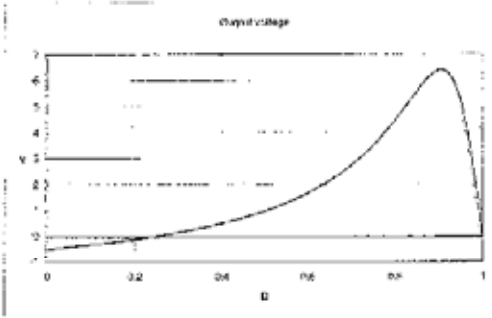
$= 2.14W$

$P_{in} = P_{out} + P_{loss} = 7.14W$

$\Rightarrow \eta = \frac{5W}{7.14W} = 0.70$ ✓

Part (f)


Efficiency
1
0.75
0.5
0.25
0
-0.25
-0.5
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
D


Output voltage
7
6
5
4
3
2
1
0
0.2
0.4
0.6
0.8
1
D

c) Discuss plot

- Correct voltage ($v=5$) and efficiency ($\eta=0.7$) are indeed obtained at $D=0.826$
- Predicted efficiency is negative for $D<0.25$! This is complete nonsense. What is wrong with the model at low duty cycle?

Note that the output voltage (and hence also the output current) are predicted to reverse polarity for $D<0.25$. This cannot happen, because the diode will be reverse-biased when it is supposed to conduct.

We are modeling the diode as a constant 0.5V source during the diode conduction interval. According to the model, this source supplies power for $D<0.25$, leading to negative efficiency. Of course, this cannot happen, and the model breaks down.

Ch5 What actually happens at low duty cycle is that the converter enters a new mode of operation, known as the discontinuous conduction mode. The origins of this mode are studied in detail in Section 4.1 and Chapter 5.