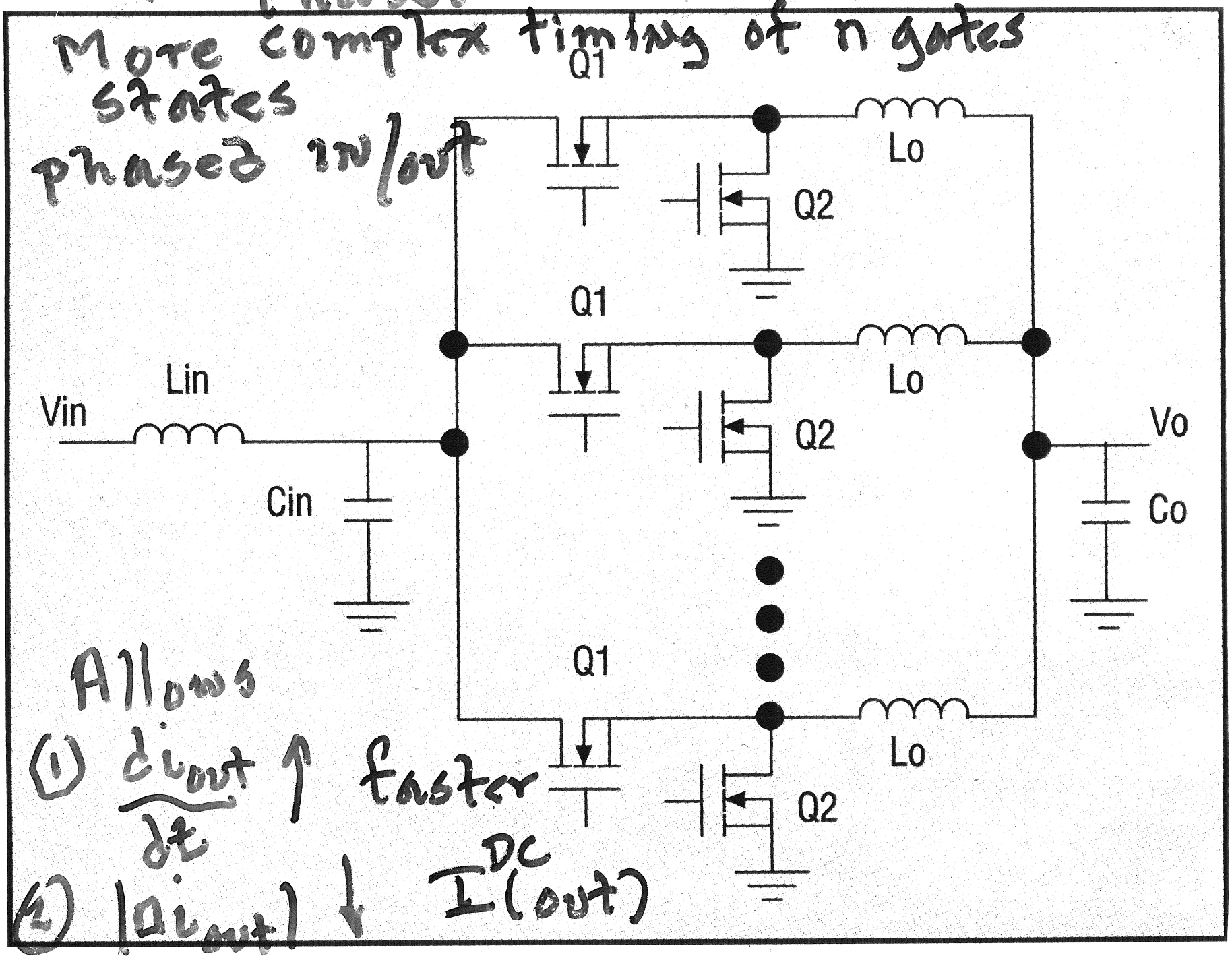

Multiphase interleaved buck converter. (Courtesy of Intersil Corp.)

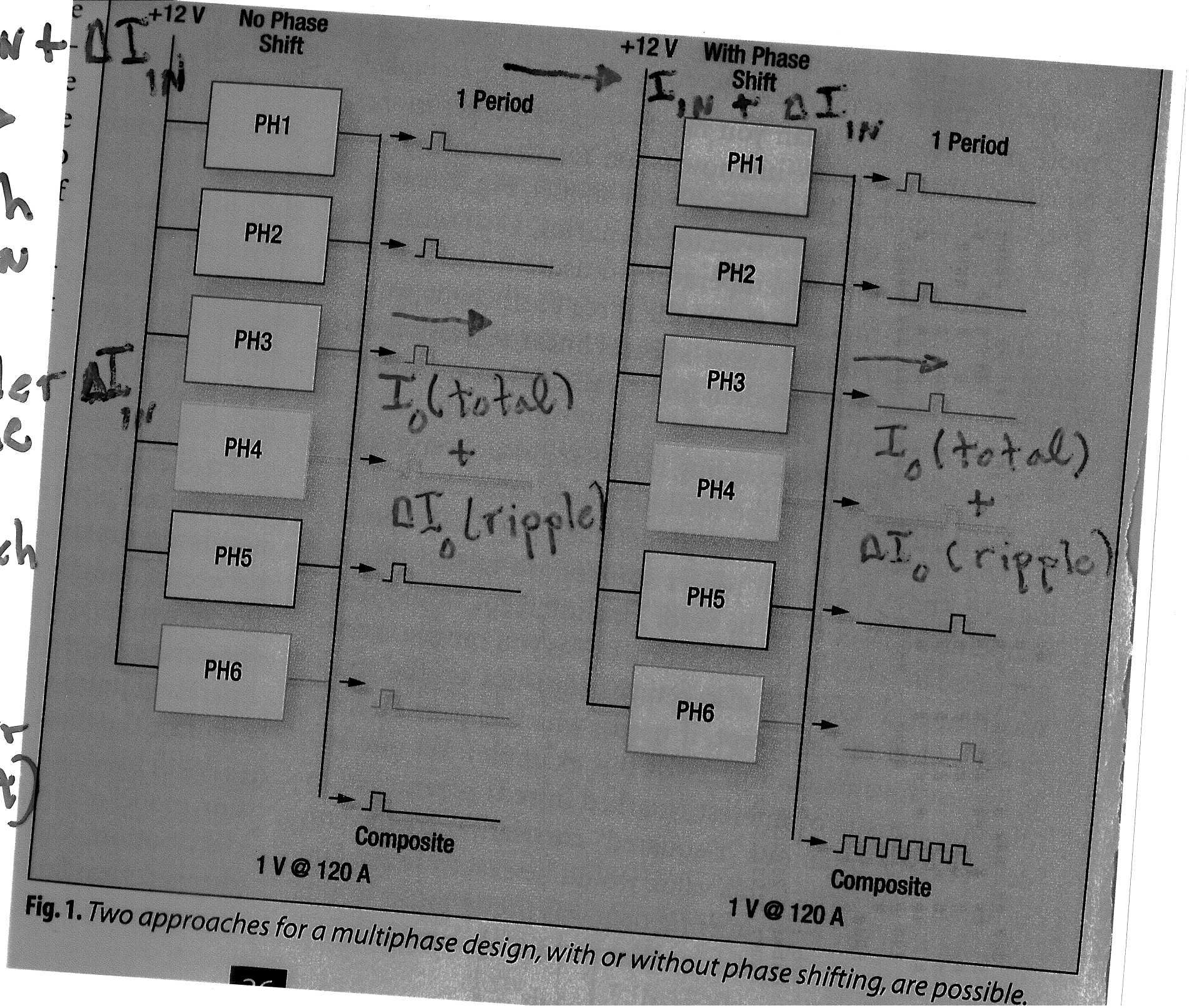

Fig. 1. *Two approaches for a multiphase design, with or without phase shifting, are possible.*

N fixed

Phase $\frac{360}{N}$ Staggered On/Off

Simultaneous ON/off

Parameter	Interleaved	Noninterleaved
RMS input ripple	10.38 A	37.2 A
Peak-to-peak input ripple	24.3 A ~ 7X ~	145 A
RMS output ripple	0.75 A	10.1 A
Peak-to-peak output ripple	2.65 A ~ 16X ~	34.7 A
Ripple frequency	1.38 MHz ~ 5X ~	230 kHz

Table 2. *Ripple current simulation results.*

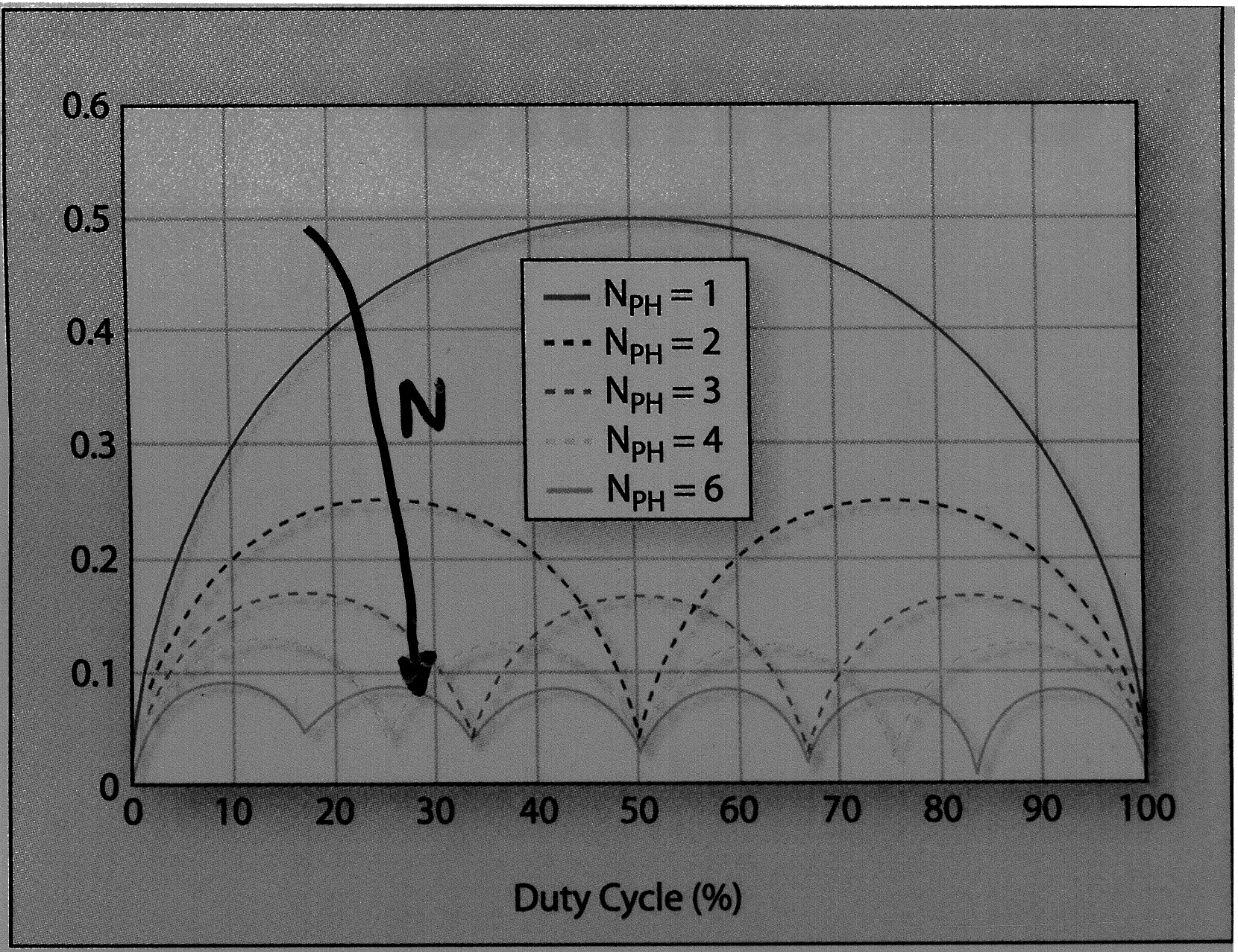

Fig. 2. *The plots of normalized rms input ripple current versus duty cycle show that ripple current is a periodic function of duty cycle whose magnitude decreases as the number of phases increases.*

Periodi
minima
in
ΔI(D)
IN
adds
subtle
path

Both
N and D
choices
reduce
ΔI
IN

ACTIVE CURRENT SHARING MULTIPHASE DC-DC CONVERTER

(1)

United States Patent **7,479,772**

Zane , et al. **January 20, 2009**

A converter module for use as a phase in a multiphase DC-DC converte having a data bus for transferring current-sharing information is provided The converter module includes a power stage and a controller. The powe stage comprises an input for receiving an input voltage and an outpu for providing an output voltage and an output current. The controller i coupled to the power stage to receive a feedback signal from the powe stage. The controller further comprises a data bus port configured tc receive the current-sharing information from the data bus and provide updated current-sharing information to the data bus.

Inventors: Zane; Regan A. (Superior, CO), Maksimovic; Dragan (Boulder, CO), Zhang; Yang (Boulder, CO)

Assignee: The Regents of the University of Colorado (Boulder, CO)

Appl. No.: 11/364,886

Filed: February 27, 2006

DYNAMIC MULTIPHASE OPERATION

(2)

United States Patent **7,479,766**

Sutardja , et al. **January 20, 2009**

An output regulator comprises M switch arrays, where M is an intege greater than 2. A controller selectively enables N of the M switch array in response to a sense signal. The sense signal is based on an output of the output regulator. The controller generates drive signals to control the N o the M switch arrays, where N is an integer greater than or equal to 0 anc less than or equal to M. When N is greater than 0, the controller dynamically sets a phase interval between the N of the M switch arrays to one of greater than 360/N or less than 360/N.

Inventors: Sutardja; Sehat (Los Altos Hills, CA), He; Runsheng (Sunnyvale, CA)

Assignee: Marvell World Trade Ltd. (St. Michael, BB)

Appl. No.: 11/895,673

Filed: August 27, 2007