ECE 562

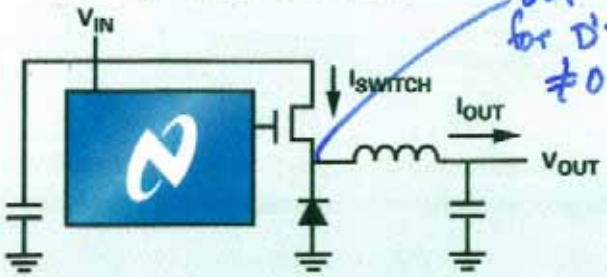
Week 3 Lecture 1

Week 3 Lecture 1
Summary

- Section notes
  - Slides 3-11 – Buck converters
  - Slides 12-21 – Current sensors and waveforms
  - Slides 22-31– Commercial chip characteristics
  - Slides 32-34 Convertor efficiencies
  - Slides 35-69 – Homework review


RULE #9
IT PAYS TO USE THE
RIGHT TOOLS FOR THE JOB

Non-synchronous buck



V_{out} ? for $D'T_{SW} \neq 0$

Function: Step-down ($V_{OUT} < V_{IN}$)

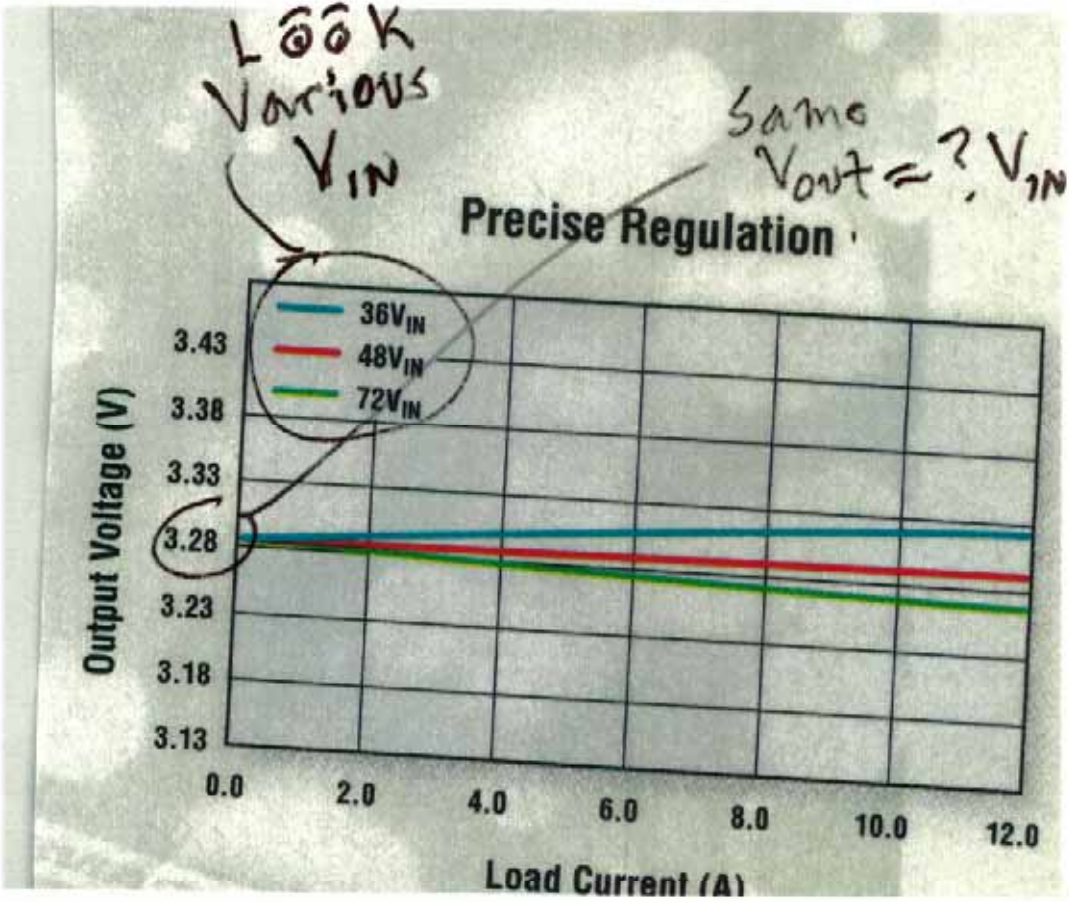
When to use: Typically when V_{IN} is 3x to 5x V_{OUT} and I_{OUT} is > 0.5A and < 5A

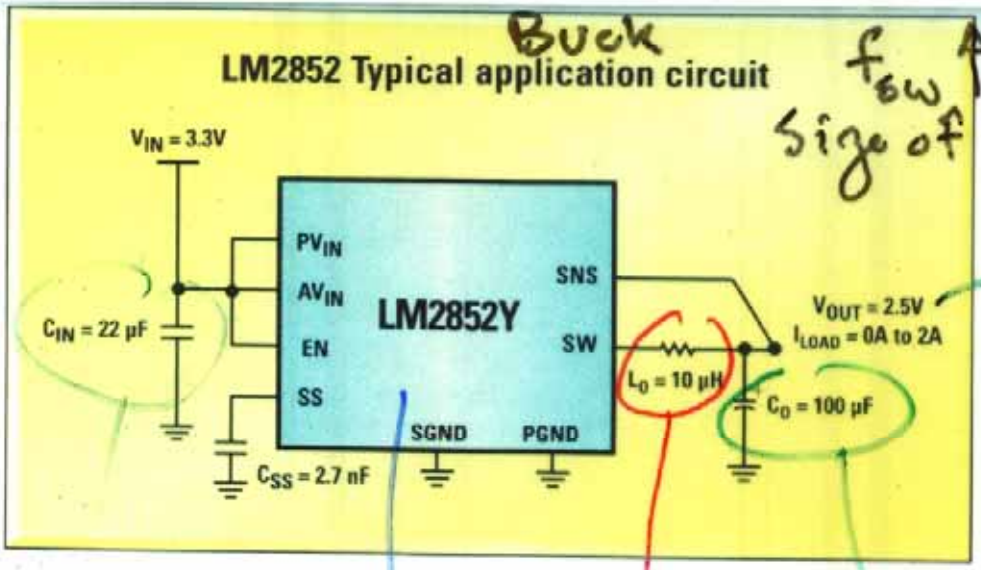
Characteristics: Easy to design and good efficiency for the above-mentioned typical $V_{IN}/V_{OUT}/I_{OUT}$ conditions

Devices to use: All buck integrated regulators and controllers

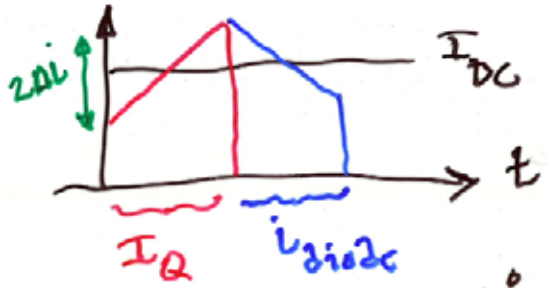
Qrr of diode: Ch 3 losses
Cost of diode
? smart diode ?

Why are diode losses high ?
which transition of diode has most loss ON-off or off-ON


LOOK
Various
V_{IN}
Same
$V_{out} = ? V_{IN}$
Precise Regulation
$36V_{IN}$
$48V_{IN}$
$72V_{IN}$
3.43
3.38
3.33
3.28
3.23
3.18
3.13
Output Voltage (V)
0.0
2.0
4.0
6.0
8.0
10.0
12.0
Load Current (A)


Buck
LM2852 Typical application circuit
f_{SW} ↑
Size of L & C?
V_{IN} = 3.3V
PV$_{IN}$
AV$_{IN}$
EN
SS
LM2852Y
SNS
SW
SGND
PGND
C_{IN} = 22 µF
C_{SS} = 2.7 nF
L_O = 10 µH
C_O = 100 µF
V_{OUT} = 2.5V
I_{LOAD} = 0A to 2A
V_O(min) = .8
> 0.8
C_{IN}(ex)
$f_{SW} \sim \frac{1}{2}$ MHz
Internal FETS for all switches
L_{EX}
C_{EX} low ESR caps
You choose Just add big C_L

$i_L(t)$ is sum of $I_D + I_L$



L acts as a "flywheel"

Δi

$$2\,\Delta i = \frac{V_{IN} - V_{out}}{L}\left(\frac{D}{f_{SW}}\right) \quad \Delta t$$

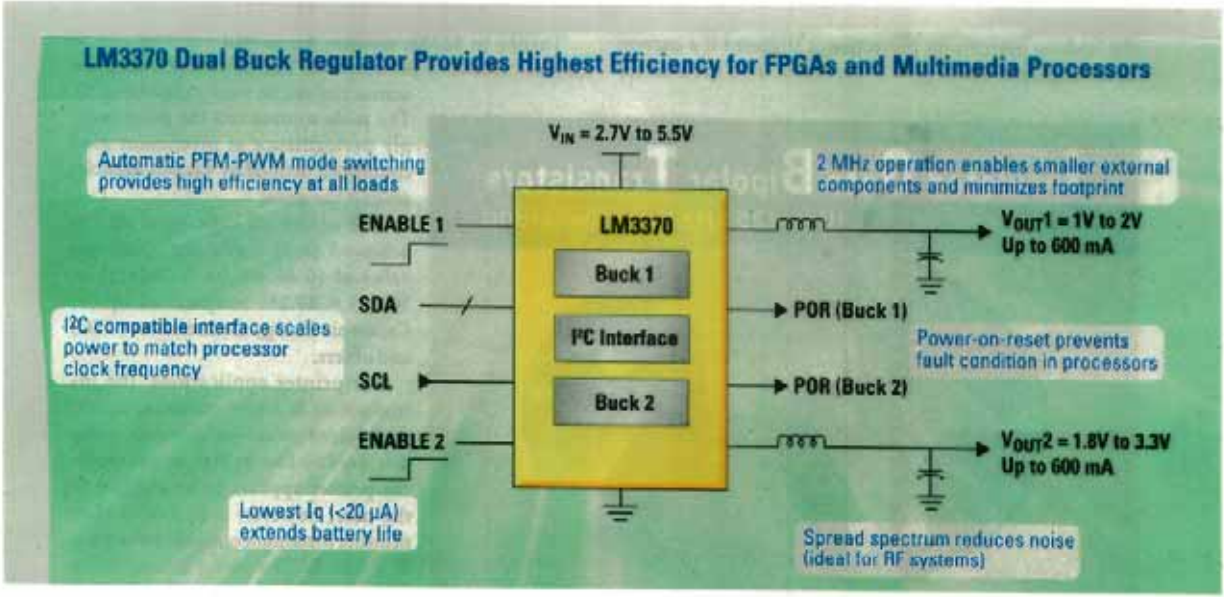
Choose desired Δi

Pick L f_w

Pick $D \equiv \frac{V_o}{V_{IN}}$

$$2\,\Delta V_c = \frac{I_{load}}{C}\left(\frac{D}{f_{SW}}\right) \quad \Delta t$$

BOGO
for low i applications



Synchronous Rectification in High–Performance Power Converter Design

— *By Robert Selders, Jr., Applications Engineer*

nmos?

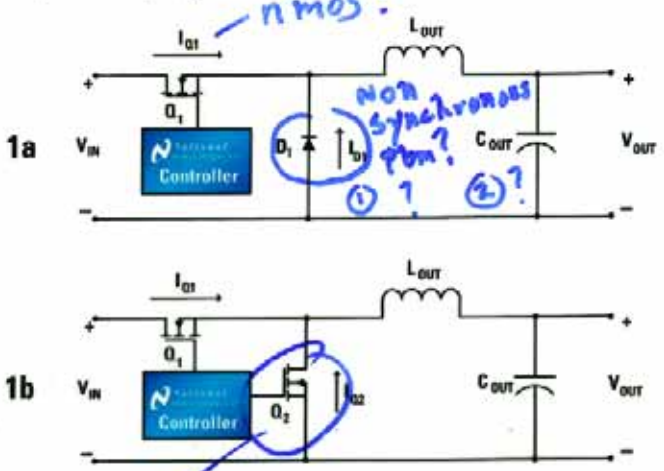


Figure 1. (a) Non-synchronous and (b) Synchronous Buck Converters

— replace (V_{ON} 1V) power diode.

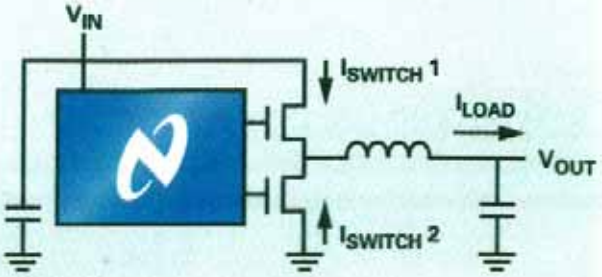
① avoid shoot through from Q_{FF}

② Always CCM (no need Ch5)

③ $V_{ON} = I * R^{Q_2}_{ON}$ (parallel FETs

④ Need 100A in mΩ → 0.1V

Synchronous buck



Function: Step-down ($V_{OUT} < V_{IN}$)

When to use: When high efficiency is required with high-output current (> 5A) or low duty cycles ($V_{IN} > 5 \times V_{OUT}$ and/or $I_{OUT} < 0.5A$)

Characteristics: A second switch replaces the diode in the basic buck topology, reducing losses in the conditions mentioned above

Devices to use: Any "synchronous rectification" buck integrated regulator or controller

Figure 2: Step-down configurations

Cost of FET Drives ?
VS
"Smart" diode

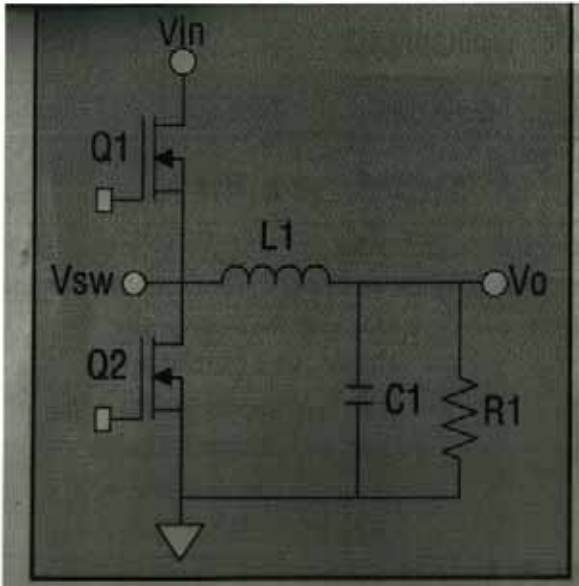


Fig. 1. *Simplified schematic of a typical synchronous buck converter. The inductor current always flows through either Q1 or Q2. During the on-time, Q1 is ON, and inductor current increases. During the off-time, Q2 is ON, and the inductor current decreases. At the on/off transition times, the inductor current has to quickly switch from one FET to the other one.*

$V_{FET}(ON) = I R_{ON}$

~~if too high use V_{CE} (bipolar)~~ $\sim$ 0.1V

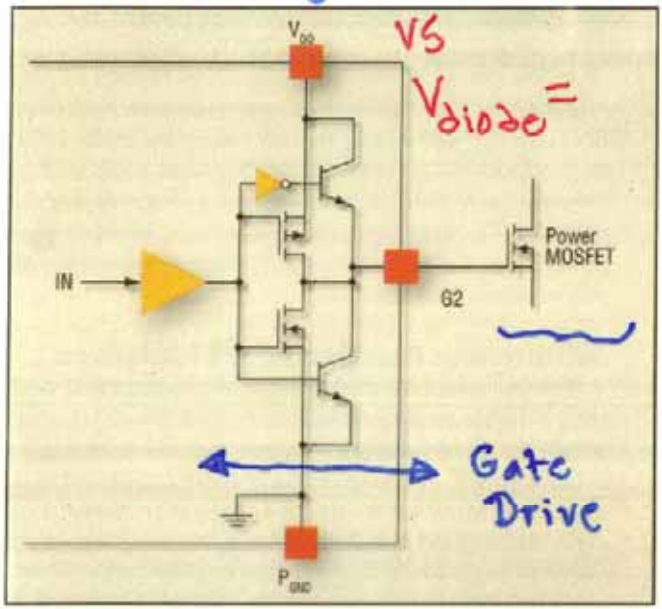
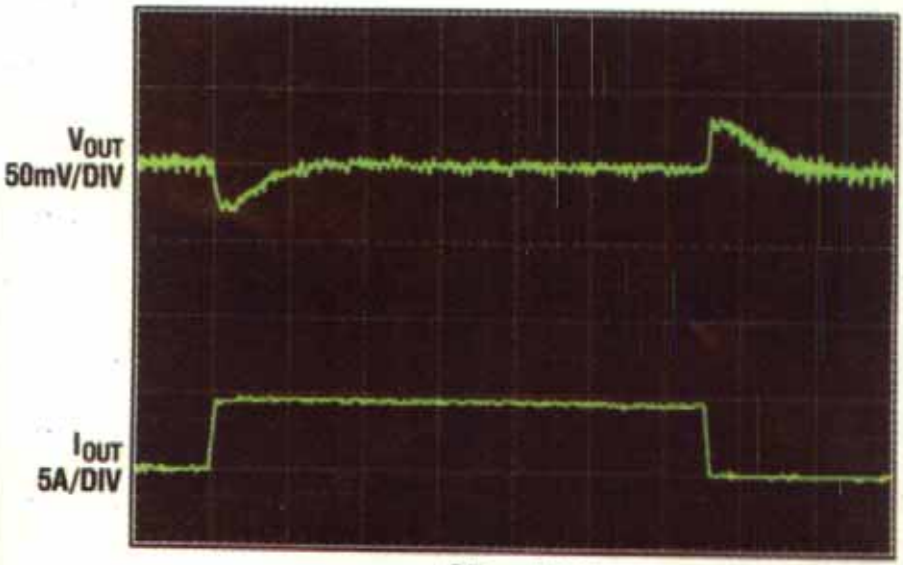


Fig. 3. *The TrueDrive gate-drive architecture (low-side only) from Texas Instruments places bipolar and MOS transistors in parallel to deliver the rated drive current while lowering the pull-down impedance for better dv/dt immunity.*

Ultrafast Transient Response

2% ΔV_{OUT} with a 5A Step



V_{IN} = 12V, V_{OUT} = 1.5V, 0A to 5A Load Step

(C_{OUT} = 3 x 22µF CERAMICS, 470µF POS CAP)

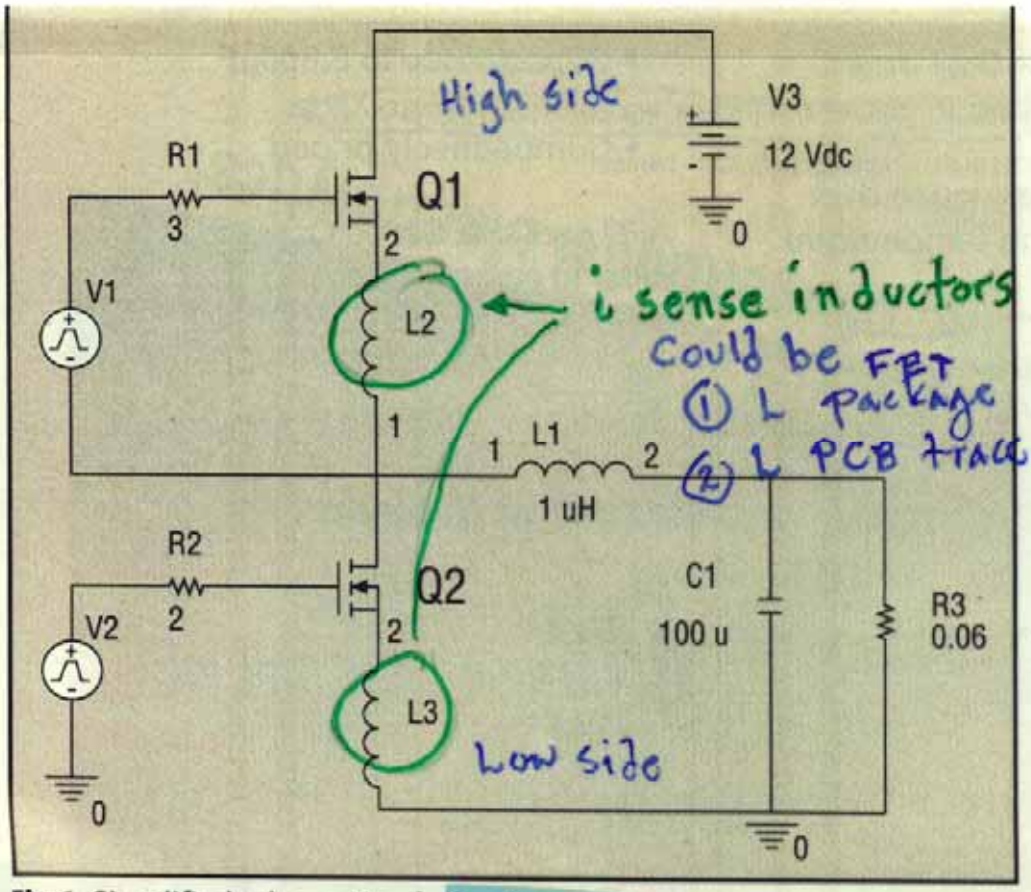


Fig. 1. *Simplified schematic of a buck converter.*

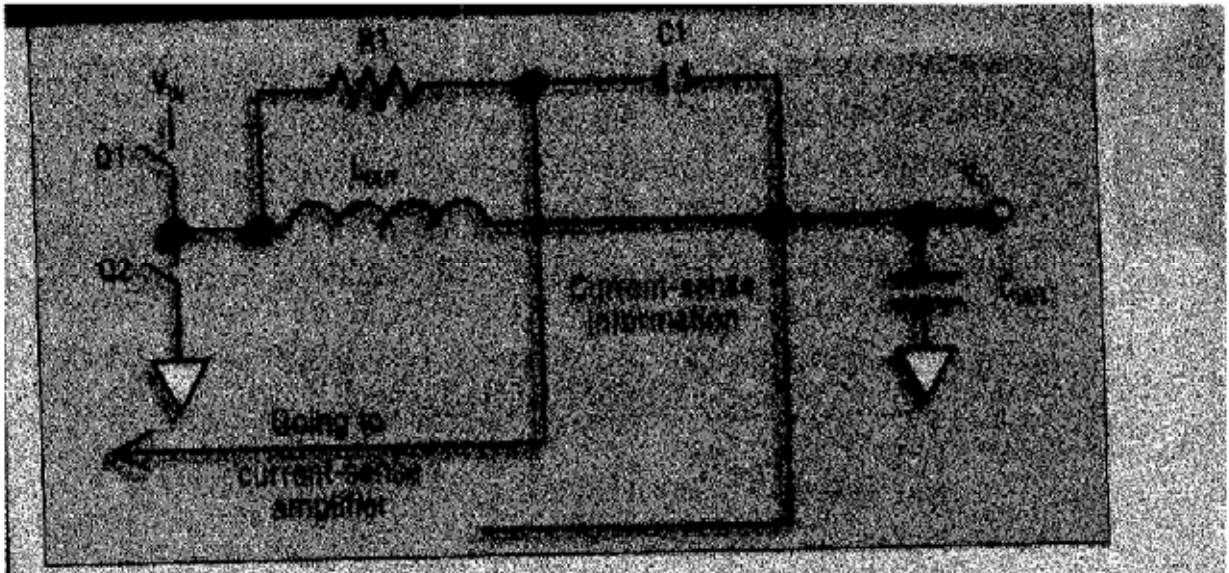
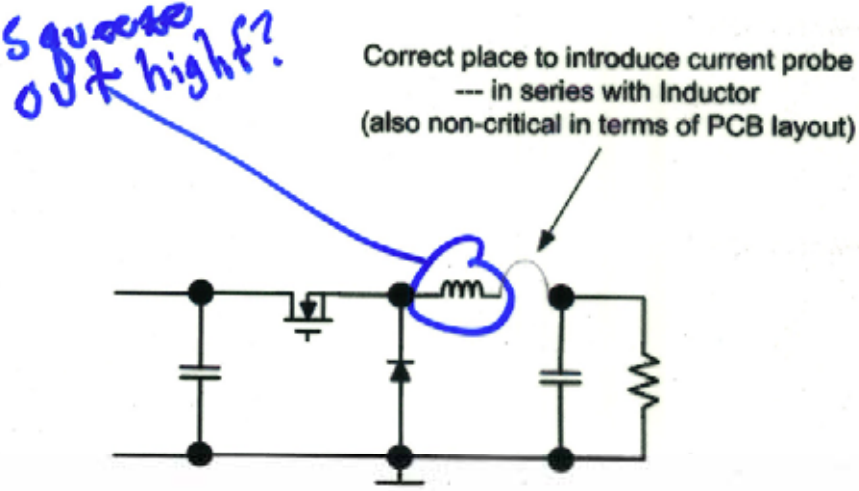


Fig. 2. *Replacing R_{SENSE} with an inductor for current sensing reduces power losses and increases the efficiency of the regulator. Voltage-sensing information is across C1.*

Current Probe Insertion --- Correct Location

The correct location to introduce a current probe (or current sense resistor), for any topology --- is in *series with the inductor*. Note that this is the length from the switchir node to the output capacitor. This particular "stretch of land" is *not* critical.



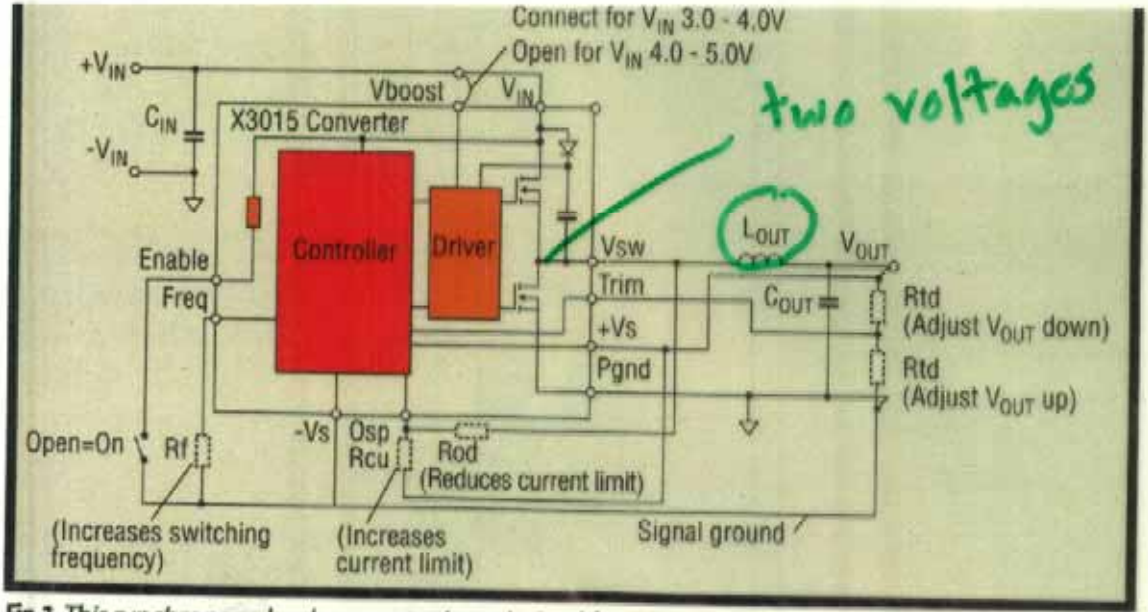


Fig. 1. *This synchronous buck converter is optimized for minimum switching and conduction losses.*

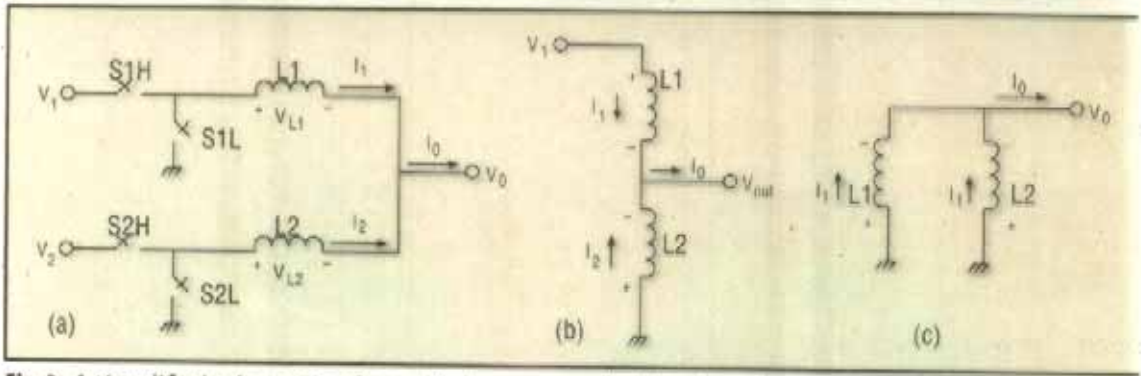
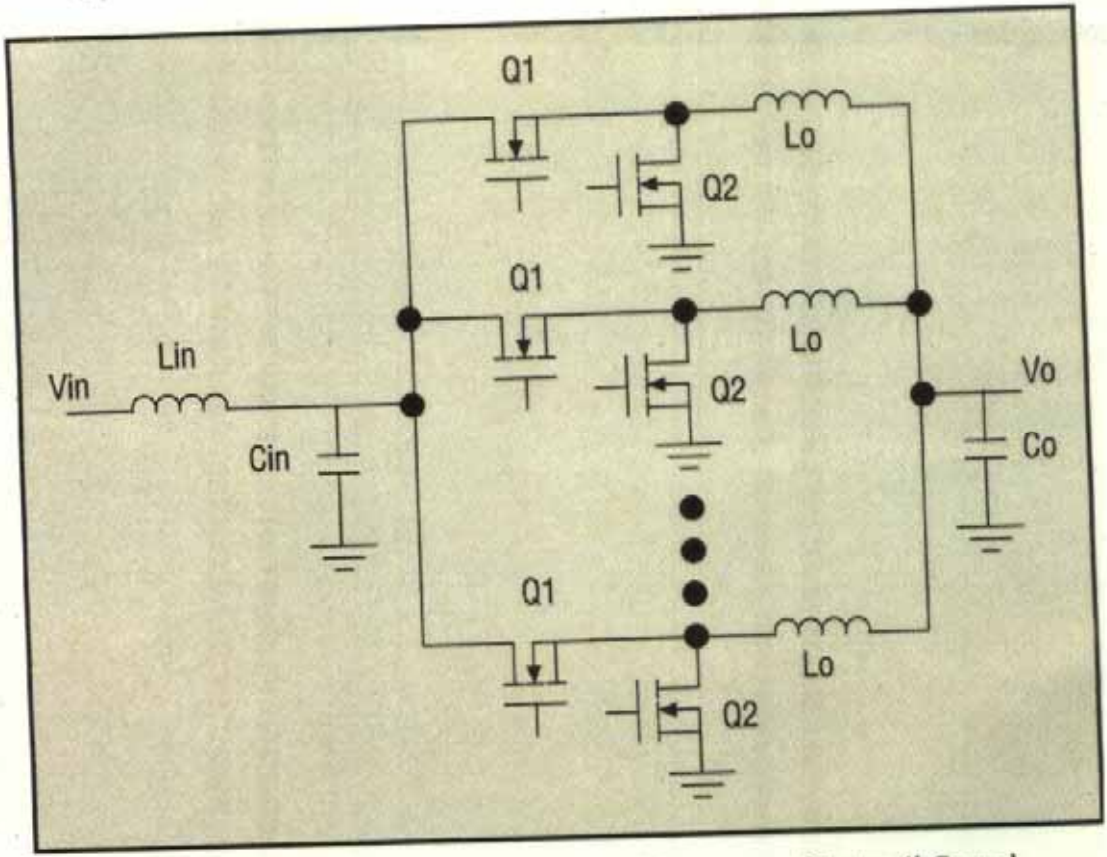


Fig. 2. *A simplified schematic of a multiphase uncoupled buck regulator (a) illustrates the two basic switching actions. In state one (b), S1H and S2L are closed while S1L and S2H are open. The input then sources energy to L1 and the output, and L2 sources energy to the output. In state two (c), S1L and S2L are closed, and S1H and S2H are open. Thus, both inductors source energy to the output. These operations are reversed for states three and four (not shown).*



Multiphase interleaved buck converter. (Courtesy of Intersil Corp.)

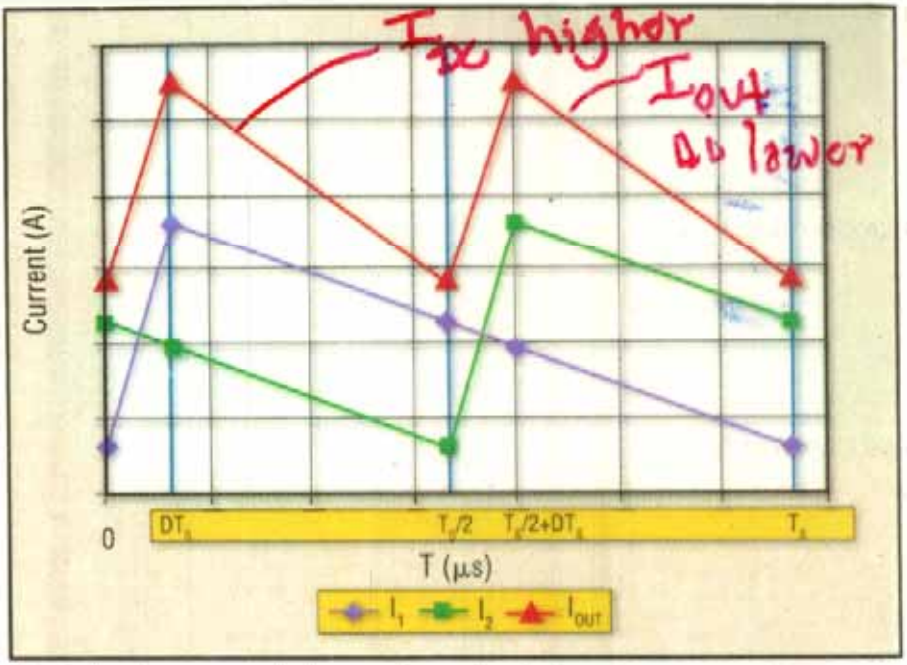


Fig. 3. *In the uncoupled two-phase buck, the phase currents are out of phase.*

$$2\Delta i \simeq \frac{V_o - V_{in}}{L} \frac{D}{f_{sw}} \frac{1}{n}$$

how 360° is split by parallel bucks

$n \uparrow \quad \Delta i \downarrow$

Latest f ↑ * 5

The Good Stuff

- Up to 2.5MHz switching frequency
- >4MHz sync capability
- Minimum pulse width <25ns
- Fast current limit: <35ns
- Built-in 180V start-up circuitry
- <1mA quiescent current
- Built-in MOSFET driver: 3Ω sink, 7Ω source
- Programmable undervoltage lockout
- Programmable soft start
- Resistor programmable current sense threshold
- Primary power limit for fault conditions
- Low current <5µA shutdown mode
- 50% duty cycle limit with MIC9130
- 75% duty cycle limit with MIC9131
- 16-pin SOIC and QSOP packages

$5 / chip

Applications:

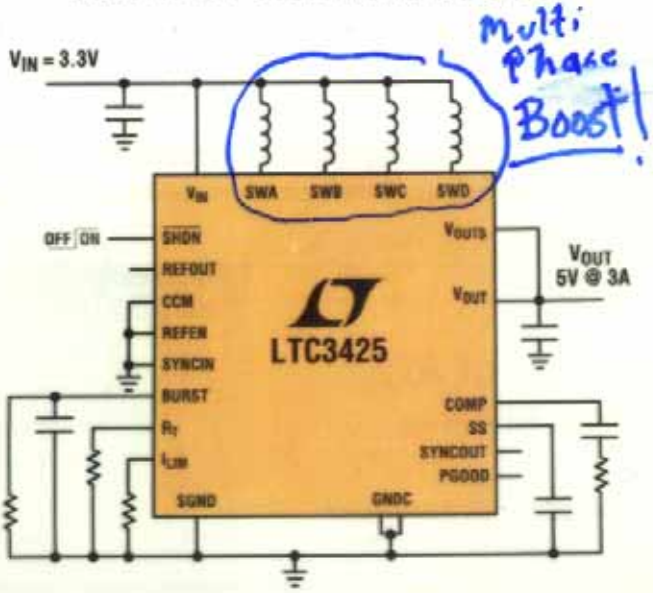
- Low-voltage, high-density distributed power systems
- Point-of-load regulation for high-performance DSPs, FPGAs, ASICs and microprocessors
- Broadband, networking and optical communications infrastructure
- Portable computing/notebook PCs

Features:

- 3-V to 6-V input
- 30-mΩ, 12-A peak MOSFET switches for high efficiency at 6-A continuous output
- 0.9-V to 3.3-V adjustable output voltage range with 1.0% initial accuracy, fixed versions available
- Wide PWM frequency — fixed 350 kHz, 550 kHz or adjustable 280 kHz to 700 kHz
- Load protected by peak current limit and thermal shutdown
- Complete set of design tools: EVM, software tool and datasheets
- TPS5461x starts at $4.99 per device in quantities of 1,000

Synchronous Boost

3.3V to 5V @ 3A with LTC3425



Features

- Switching Frequencies up to 4MHz
- High Efficiency Operation: Up to 96%
- Quiescent Currents as low as 10µA
- Very Fast Transient Response
- EMI Control Techniques Reduce Interference
- Minimal External Components
- Small, ≤ 1mm Profile Packages

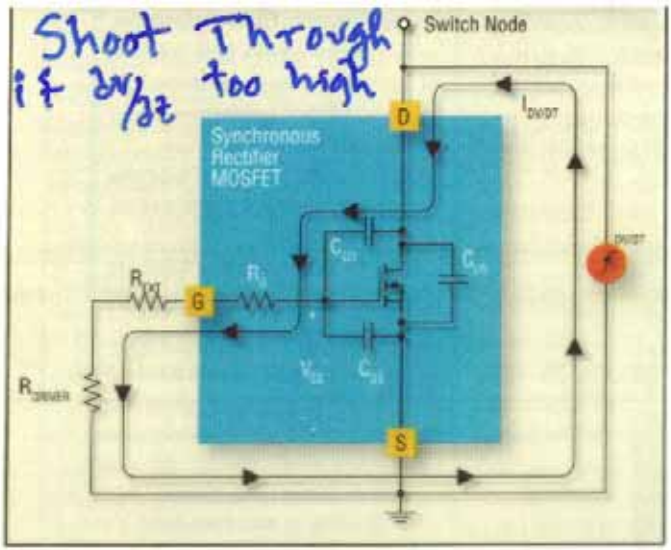


Fig. 1. *Turn-on of the high-side MOSFET (not shown) produces a voltage transient dv/dt across the low-side (synchronous) MOSFET, which leads to the off-state current conduction shown here.*

(1) +V rail connected to D
Δ dv/dt when UPPER FET ON

(2) Via C_{gd} lower FET ON
Short at ☹

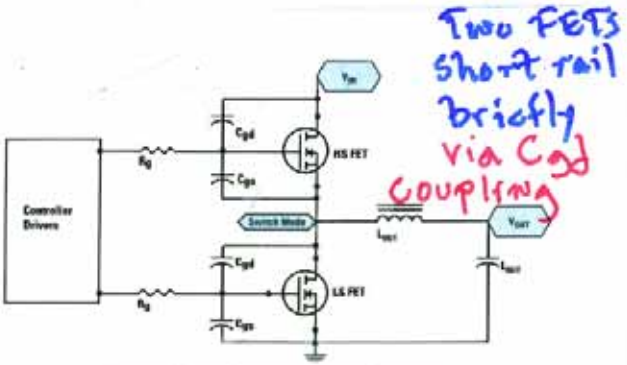


Figure 3. Synchronous Buck Converter

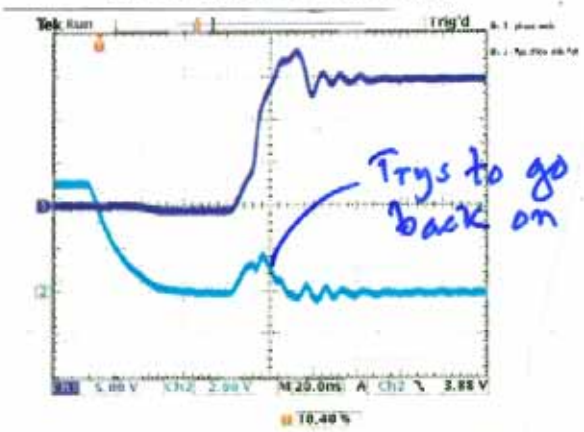


Figure 4. dv/dt induced step on the low-side MOSFET
Ch 1 Switch node
Ch 2 Vgs _ low-side MOSFET

MOSFET V_{GS} - Q_G

DV/DT IMMUNITY

Extra Credit

Th
V_{GS} to avoid shoot through

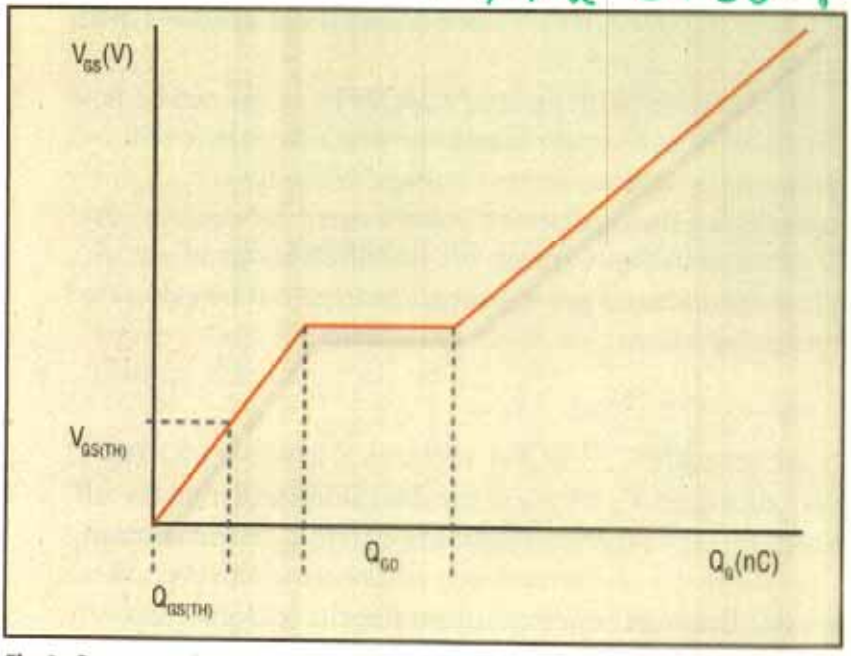
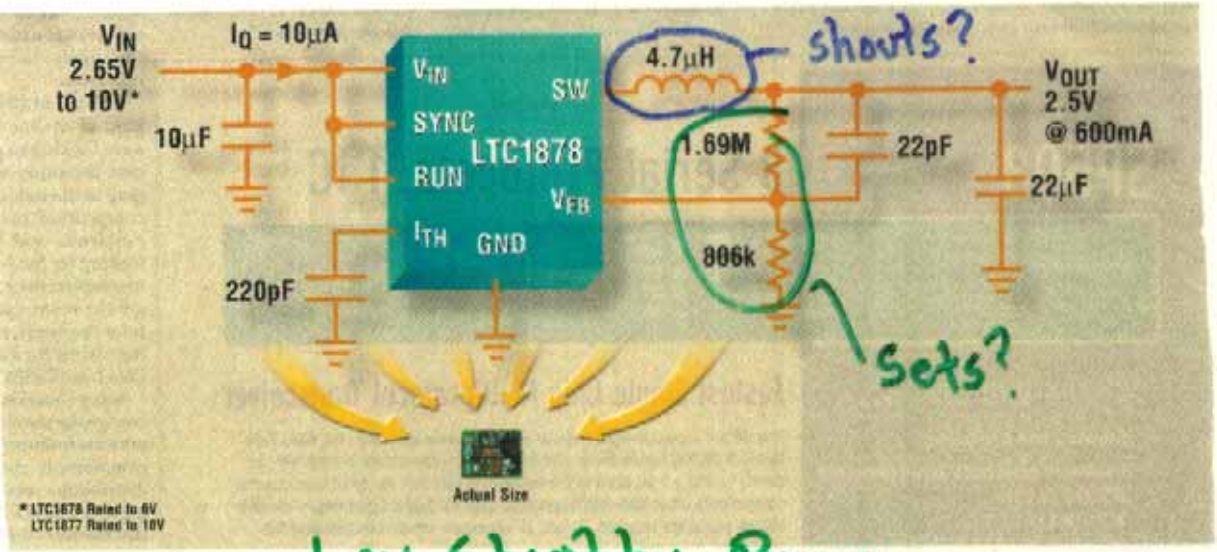


Fig. 2. $Q_{GS(TH)}$ *and* Q_{GD} *may be determined from the MOSFET gate-charge curve.*



Low Standby Powa

95% Efficient Synchronous Step-Down Regulators Draw Only 10µA

Linear Technology

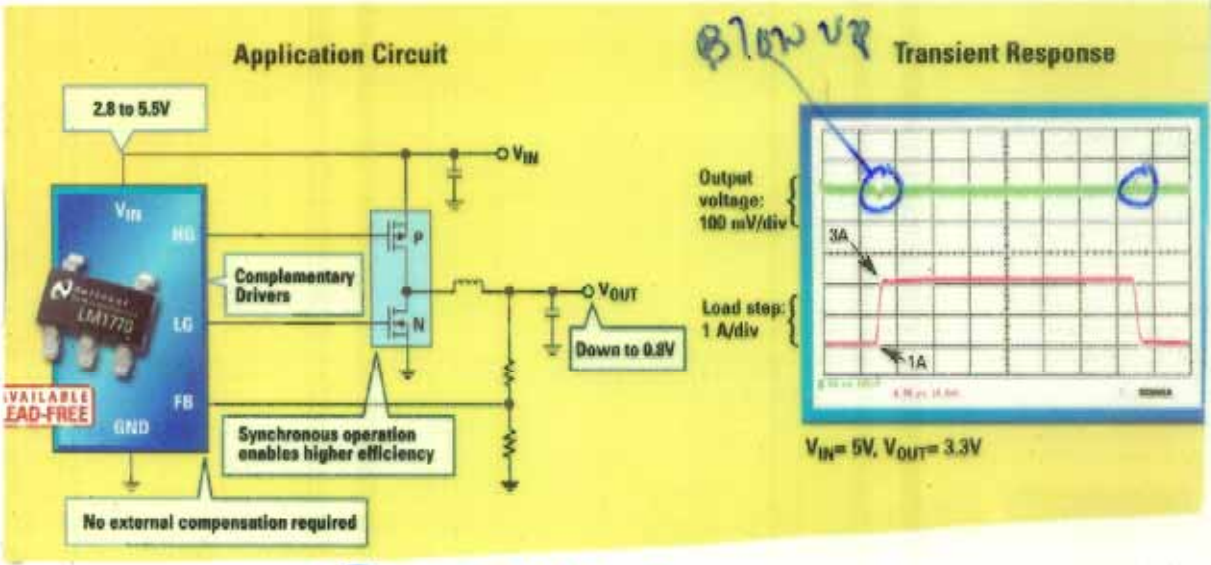
Meaning

Need external L C's R

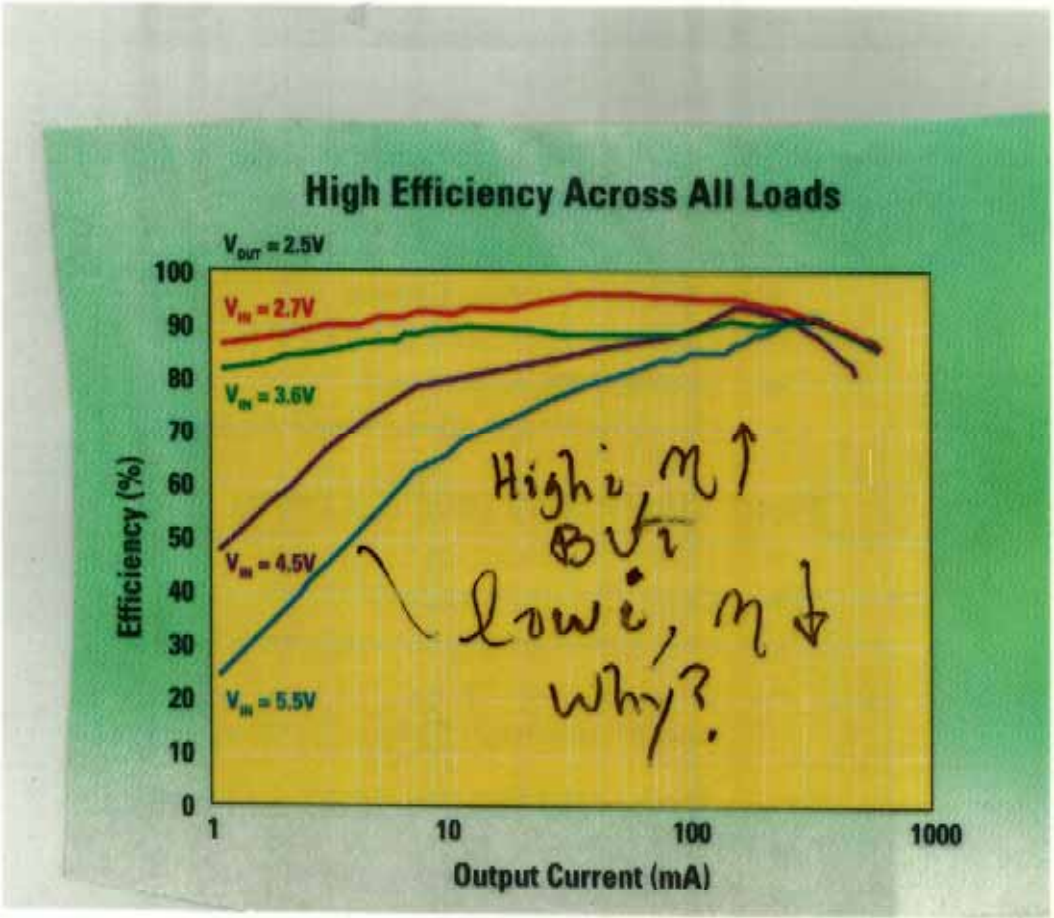
Features

- No External FETs or Schottky Diode Required
- 10µA Quiescent Current
- Up To 95% Efficiency
- 2.65V to 10V Input Voltage (LTC1877)
- 600mA Output Current
- <1µA Shutdown Current
- Selectable Burst Mode™ Operation
- 550kHz Constant Frequency Operation Synchronizable from 400kHz to 700kHz
- Uses Ceramic or Tantalum Capacitors
- Small, Thin 8-Pin MSOP Package

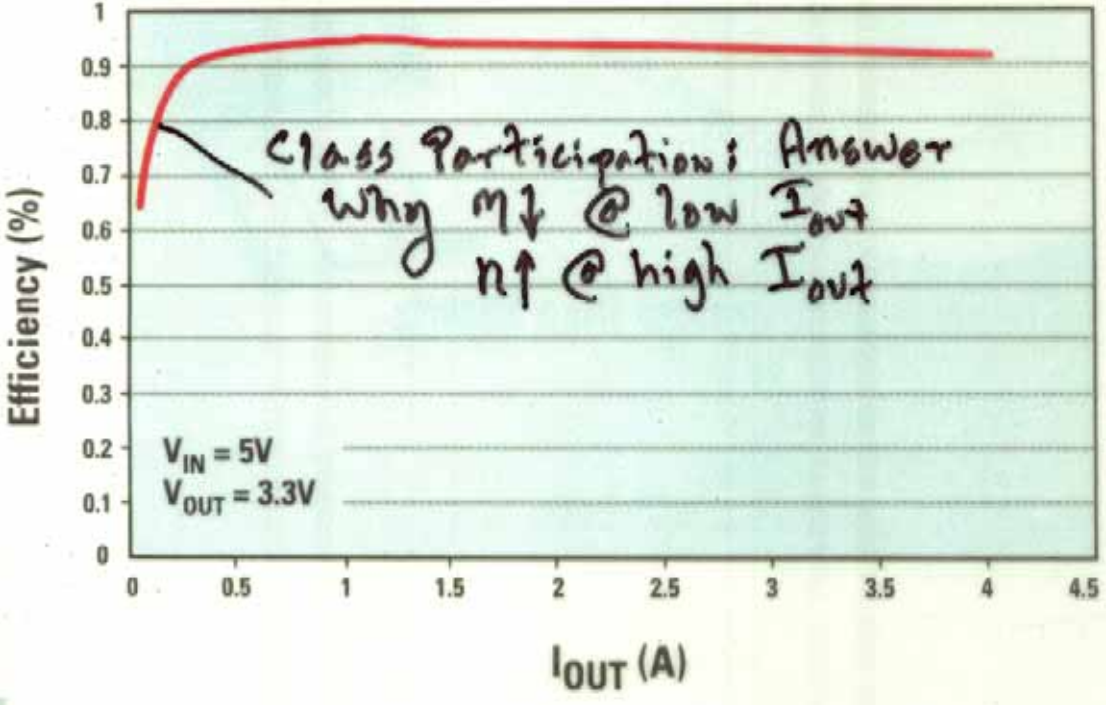
High-Efficiency LM1770 Synchronous Controller for Low-Voltage DC-DC Conversion



For Talk #1


High Efficiency Across All Loads
V_{OUT} = 2.5V
V_{IN} = 2.7V
V_{IN} = 3.6V
V_{IN} = 4.5V
V_{IN} = 5.5V
Efficiency (%)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000
Output Current (mA)
High i, η ↑
But
low i, η ↓
Why?

>90% Efficiency Over Load Current

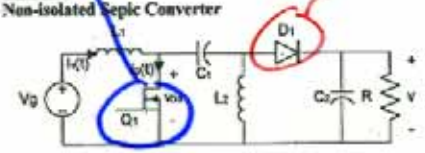


Active switch L2

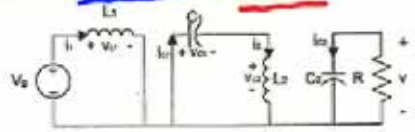
complement diode

HW #1
Ch. 2 Prob. 2, 3, 4, 6

Prob. 2.2
Non-isolated Sepic Converter

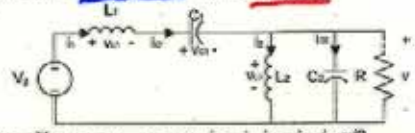


(a)
Position 1. Transistor is on and the Diode is off.



$v_{L1} = V_g$, $v_{L2} = -v_{c1}$, $i_{c1} = i_2$, $i_{c2} = -v/R$
Using the small ripple approximation $\Rightarrow v_{L1} = V_g$, $v_{L2} = -V_{c1}$, $i_{c1} = I_2$, $i_{c2} = -V/R$

Position 2. Transistor is off and the Diode is on.



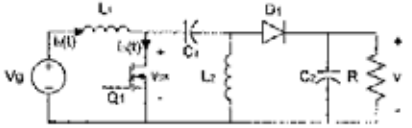
$v_{L1} = V_g - v_{c1} - v$, $v_{L2} = v$, $i_{c1} = i_1$, $i_{c2} = i_1 - i_2 - v/R$
Using the small ripple approximation $\Rightarrow v_{L1} = V_g - V_{c1} - V$, $v_{L2} = V$, $i_{c1} = I_1$, $i_{c2} = I_1 - I_2 - V/R$

CCM two state

HW #1
Ch. 2 Prob. 2, 3, 4, 6

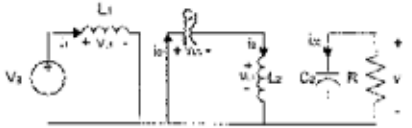
Prob. 2.2

Non-isolated Sepic Converter



(a)

Position 1. Transistor is on and the Diode is off



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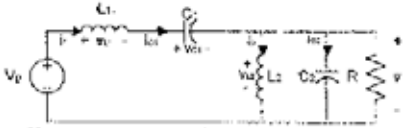
Using the small ripple approximation $\Rightarrow v_{L1} = V_g$, $v_{L2} = -V_{c1}$, $i_{c1} = I_2$, $i_{c2} = -V/R$

Position 2. Transistor is off and the Diode is on.

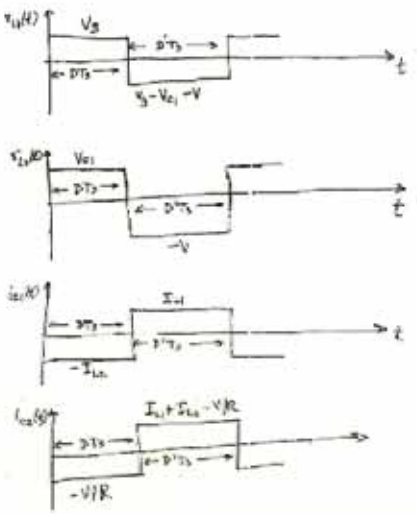


$v_{L1} = V_g - v_{C1} - v$, $v_{L2} = v$, $i_{c1} = i_1$, $i_{c2} = i_1 - i_2 - v/R$

Using the small ripple approximation $\Rightarrow v_{L1} = V_g - V_{c1} - V$, $v_{L2} = V$, $i_{c1} = I_1$, $i_{c2} = I_1 - I_2 - V/R$

V-sec balance on L's
I-sec balance on C's

Waveforms:



V_2 out
i_{L1} & i_{L2} not shown

i_{L1} & i_{L2}

i_0

Volt-second balance

$$\langle v_{L1} \rangle_{T_s} = D(V_g) + D'(V_g - V_{c1} - V) = 0$$

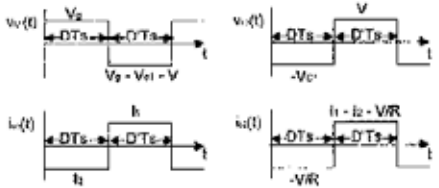
$$\langle v_{L2} \rangle_{T_s} = D(V_{c1}) + D'(-V) = 0$$

with $D' = 1 - D$

charge balance

$$\langle i_{c1} \rangle_{T_s} = D(-I_{L2}) + D'(I_{L1}) = 0$$

$$\langle i_{c2} \rangle_{T_s} = D\left(-\frac{V}{R}\right) + D'\left(I_{L1} + I_{L2} - \frac{V}{R}\right) = 0$$



Equating the DC components of the above waveforms to zero and knowing $D' = 1 - D$:

$\langle v_{s1} \rangle = DV_g + D'(V_g - V_{c1} - V) = 0$

$\langle v_{s2} \rangle = D(-V_{c2}) - D'V = 0$

$\langle i_{s1} \rangle = DI_2 + D'I_1 = 0$

$\langle i_{s2} \rangle = D(-V/R) - D'(I_1 - I_2 - V/R) = 0$

The solution to this system of equations for the DC components of the capacitor voltages and the inductor currents yields:

$\mathbf{V_{c1} = V_g}$

$\mathbf{V_{c2} = V = DV_g/D' = DV_g/(1-D)}$

$\mathbf{I_{L1} = I_1 = (D/D')^2 V_g/R}$

$\mathbf{I_{L2} = I_2 = -DV_g/D'R}$

(b) Known: $V = 28$ volts, $18v \le V_g \le 36v$, $I_{test} = 2A$

(1) We have the following equation relating D, V_g, and V which we can use to solve for D:

$V = DV_g/(1-D)$ *solving for* D yields $\Rightarrow D = V/(V+V_g)$.

Substituting in the knowns gives the range for $D \Rightarrow \mathbf{0.4375 \le D \le 0.6078}$

(2) We know the load current and voltage thus we can get the resistance

$R = V/I = 28v/2A = 14\Omega$.

We found the range for D in Part 1 and the resistance was just calculated so we can derive a range for the current I_1 using the equation from part a.

$I_1 = (D/(1-D))^2 V_g/R \Rightarrow \mathbf{1.56A \le I_1 \le 3.13A}$

Four equations and four unknowns $(V, V_{C1}, I_{L1}, I_{L2})$.

Solution:

$$V_{C1} = V_g$$

$$V = \frac{D}{1-D} V_g$$

$$I_{L1} = \frac{D}{D'} \frac{V}{R} = \left(\frac{D}{1-D}\right)^2 \frac{V_g}{R}$$

$$I_{L2} = \frac{V}{R} = \frac{D}{(1-D)} \frac{V_g}{R}$$

Part (b): voltage regulator behavior

controller automatically adjusts D, to maintain $V = 28$ volts.

Input voltage varies over the range $18 \le V_g \le 36$.

Load current = 2A = $\frac{V}{R}$, so $R = \frac{(28 \text{ volts})}{(2 \text{ amps})} = 14 \Omega$.

over what ranges do D and I_{L1} vary?

we know that $V = \frac{D}{1-D} V_g$. Solve for D:

$$V - DV = DV_g$$

$$V = D(V + V_g)$$

$$\Rightarrow D = \frac{V}{V + V_g}$$

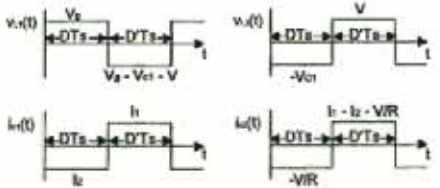
D range

and from above, $I_{L1} = \frac{D}{1-D} \frac{V}{R} = \frac{V^2}{V_g R}$

I range

V	V_g	D	I_{L1}
28	18	$\frac{28}{46} = 0.609$	$\frac{28^2}{(18)(14)} = 3.11$ A
28	36	$\frac{28}{64} = 0.438$	$\frac{28^2}{(36)(14)} = 1.56$ A

End of problem 2.2



Key

Equating the DC components of the above waveforms to zero and knowing $D' = 1 - D$:

$\langle v_{s1} \rangle = DV_g + D'(V_g - V_{c1} - V) = 0$

$\langle v_{s2} \rangle = D(-V_{c1}) + D'V = 0$

$\langle i_{s1} \rangle = DI_2 + D'I_1 = 0$

$\langle i_{s2} \rangle = D(-V/R) + D'(I_1 - I_2 - V/R) = 0$

The solution to this system of equations for the DC components of the capacitor voltages and the inductor currents yields:

$\mathbf{V_{c1} = V_g}$

$\mathbf{V_{c2} = V = DV_g/D' = DV_g/(1-D)}$

$\mathbf{I_{L1} = I_1 = (D/D')^2 V_g/R}$

$\mathbf{I_{L2} = I_2 = -DV_g/D'R}$

(b) Known: $V = 28$ volts, $18v \le V_g \le 36v$, $I_{out} = 2A$

(1) We have the following equation relating D, V_g, and V which we can use to solve for D:

$V = DV_g/(1-D)$ solving for D yields $\Rightarrow D = V/(V+V_g)$.

Substituting in the knowns gives the range for D $\Rightarrow$ **$0.4375 \le D \le 0.6078$**

(2) We know the load current and voltage thus we can get the resistance

$R = V/I = 28v/2A = 14\Omega$.

We found the range for D in Part 1 and the resistance was just calculated so we can derive a range for the current I_1 using the equation from part a.

$I_1 = (D/(1-D))^2 V_g/R$ $\Rightarrow$ **$1.56A \le I_1 \le 3.11A$**

Sepic

Inductor current waveforms

Fig 2.24 a-b pg 30

Interval 1 slopes, using small ripple approximation:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g}{L_1}$$

$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_1 - V_2}{L_2}$$

up

down

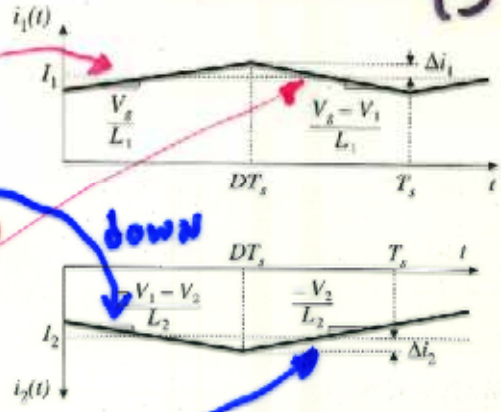
down

Interval 2 slopes:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g - V_1}{L_1}$$

$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_2}{L_2}$$

up

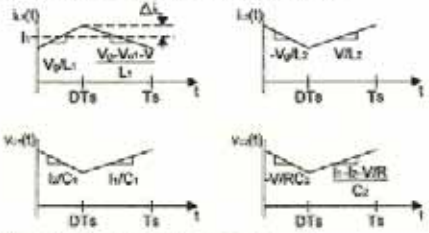


Overview Solution

Prob. 2.3

For the Sepic of Pbm. 2.2 (above)

(a) Use $di_L(t)/dt = v_L(t)/L$ and $dv_c(t)/dt = i_c(t)/C$



(Change in x) = (slope)*(length of subinterval)

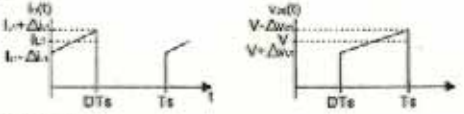
$2\Delta i_{L1} = V_g DT_s/L_1 \Rightarrow \Delta i_{L1} = V_g DT_s/2L_1$

$-2\Delta i_{L2} = -V_g DT_s/L_2 \Rightarrow \Delta i_{L2} = V_g DT_s/2L_2$

$-2\Delta v_{c1} = I_2 DT_s/C_1 = -V_g D^2 T_s/D'RC_1 \Rightarrow \Delta v_{c1} = V_g D^2 T_s/2D'RC_1$

$-2\Delta v_{c2} = -VDT_s/RC_2 = -V_g D^2 T_s/D'RC_2 \Rightarrow \Delta v_{c2} = V_g D^2 T_s/2D'RC_2$

(b)



$i_{D2}(t) = I_1 - I_2$

$i_{D2}(t)_{peak} = I_1 + \Delta i_{L1} - I_2 + \Delta i_{L2}$

$I_{D2peak} = (V_g/R)(D/D')^2 + (V_g/R)(D/D') + (I_{c1}+I_{c2})V_g DT_s/2L_1L_2$

$v_{DS}(t)_{peak} = v_{C2} + v_{C1} + \Delta v_{c1} + \Delta v_{c2} = V_g/D' + V_g D^2 T_s(C_1+C_2)/2RD'C_1C_2$

Tutorial
Solution to Problem 2.3

See solution to problem 2.2 for subinterval circuits, equations, small ripple approximation, capacitor current and inductor voltage waveforms, and solution for dc voltages and currents

$i_c(t)$
$v_L(t)$

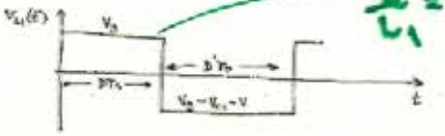
a) Derive expressions for inductor current ripples and capacitor voltage ripples

[both i_{L1} v_{L2}

Inductor L_1

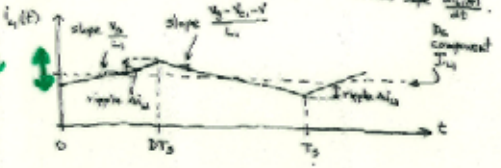
Voltage waveform (from problem 2.2):

$\frac{V_g}{L_1} = \frac{di_{L1}}{dt}$



Slope of inductor current is found using $L_1 \frac{d i_{L1}(t)}{dt} = v_{L1}(t)$

so $\frac{d i_{L1}(t)}{dt} = \frac{v_{L1}(t)}{L_1}$. [During a given subinterval, the voltage $v_{L1}(t)$ is essentially constant $\Rightarrow$ constant slope $\frac{d i_{L1}(t)}{dt}$.



Bulk ripple (i.e., peak-to-average) = Δi_{L1}

peak-to-peak ripple = $2\Delta i_{L1}$

During first subinterval, $i_{L1}(t)$ changes from $(I_{L1} - \Delta i_{L1})$ to $(I_{L1} + \Delta i_{L1})$, for a total change of $2\Delta i_{L1}$

$T_s \sim \frac{1}{f_{sw}}$

$$\left(\text{change in } i_{L1}(t)\right) = (\text{slope})(\text{time})$$

$$\left(2\Delta i_{L1}\right) = \left(\frac{V_g}{L_1}\right)(DT_s) \quad \text{for first subinterval}$$

so $$\boxed{\Delta i_{L1} = \frac{V_g D T_s}{2 L_1}}$$

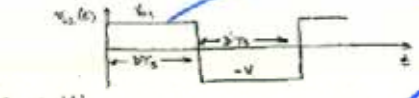
$L_1(\Delta i_{L1}, D, V_g, f_{sw})$

$L_1 \sim D$

The same result could be derived via a similar analysis of subinterval 2.

Inductor L_2

Voltage waveform, from problem 2.2:



so we obtain

$2\Delta i$

$\frac{V_{C1}}{L_2} = \frac{di_2}{dt}$

$i_{L_1}(t)$ tracks

First subinterval:

$$\underbrace{2\Delta i_{L2}}_{\text{change}} = \underbrace{\left(\frac{V_{c1}}{L_2}\right)}_{\text{slope}} \underbrace{\left(DT_s\right)}_{\text{time}}$$

$= i_{L2}(t)$

Solve for Δi_{L2}:

$$\Delta i_{L2} = \frac{V_{c1} DT_s}{2L_2}$$

$L_2(V_g, \Delta i_{L_2}, D, f_{sw})$

In problem 2.2, it was found that $V_{c1} = V_g$, so

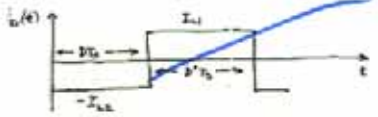
$$\boxed{\Delta i_{L2} = \frac{V_g DT_s}{2L_2}}$$

← easy design guide

$L_2 \sim D$

Capacitor C_1

Current waveform, from problem 2.2:



$\frac{I_{L2}}{C_1} = \frac{di_{C1}}{dt}$

so the capacitor voltage waveform is found using the relationship $i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt}$

Slope $\frac{dv_{c1}(t)}{dt} = \frac{i_{c1}(t)}{C_1}$

During a given subinterval, the current $i_{c1}(t)$ is essentially constant $\Rightarrow$ constant slope.

Slope during first subinterval $0 < t < DT_s$ is $-\frac{I_{L2}}{C_1}$

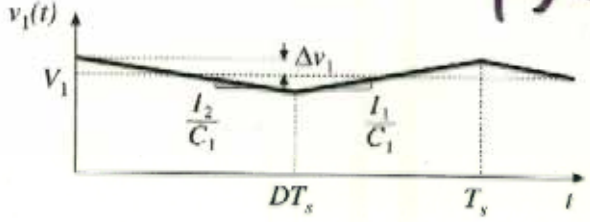
Slope during second subinterval $DT_s < t < T_s$ is I_{L2}/C_1

Capacitor C_1 waveform

Fig 2.24c
Pg 30

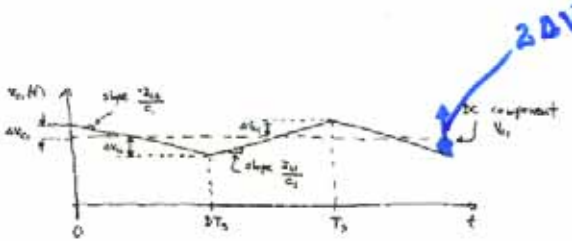
Subinterval 1:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_2}{C_1}$$



Subinterval 2:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_1}{C_1}$$



During the first subinterval, $v_C(t)$ changes by

$$\underbrace{(-2\,\Delta V_{C1})}_{\substack{\text{change}\\ \text{during}\\ 0<t<DT_s}} = \underbrace{\left(-\frac{I_{L2}}{C_1}\right)}_{\text{slope}}\underbrace{(DT_s)}_{\text{time}}$$

Solve for ΔV_{C1}:

$$\Delta V_{C1} = \frac{I_{L2}\,DT_s}{2C_1}$$

C_1 (ΔV_{C1}, D, V_g, f_{sw} and R

Substitute solution for I_{L2} (from problem 2.2): $I_{L2} = \frac{D}{D'}\frac{V_g}{R}$

$$\Delta V_{C1} = \frac{D}{D'}\frac{V_g T_s}{2RC_1}$$

} choose C_1 more complex

$$C_1 = f\left(D, \Delta V_{C1}, R\right)$$

$$C_1 \sim \frac{D}{D'}^2$$

Summary
Ripple magnitudes

Pg 31

Analysis results

$$\Delta i_1 = \frac{V_g D T_s}{2 L_1}$$

$$\Delta i_2 = \frac{V_1 + V_2}{2 L_2} D T_s$$

$$\Delta v_1 = \frac{-I_2 D T_s}{2 C_1}$$

Use dc converter solution to simplify:

$$\Delta i_1 = \frac{V_g D T_s}{2 L_1}$$

$$\Delta i_2 = \frac{V_g D T_s}{2 L_2}$$

$$\Delta v_1 = \frac{V_g D^2 T_s}{2 D' R C_1}$$

Q: How large is the output voltage ripple?

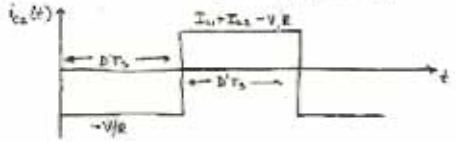
It is not zero

Requires 2nd order analysis

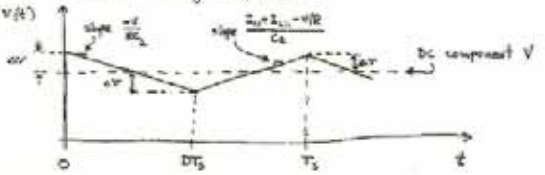
Section 2.5 Pg 32

Capacitor C_2

Current waveform $i_{C2}(t)$ from problem 2.2:



So the capacitor voltage waveform is



Change in capacitor voltage during first subinterval is

$$(-2\Delta v) = \left(-\frac{V}{RC_2}\right)(DT_s)$$

$$\Rightarrow \Delta v = \frac{VDT_s}{2RC_2}$$

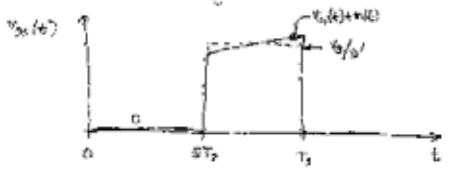
Substitute solution for V from problem 2.2: $V = \frac{D}{D'}V_g$

$$\Delta v = \frac{D^2}{D'}\frac{V_g T_s}{2RC_2}$$

C_2 choice also complex

$$C_2 \sim \frac{D^2}{(1-D)^2}$$

So the transistor voltage waveform is



End of problem 6.3

b) Sketch the waveforms of the transistor voltage $v_{DS}(t)$ and transistor current $i_D(t)$, and give expressions for their peak values.

Again, refer to schematic and waveforms in solution to problem 2.2. The transistor current $i_D(t) = i_{D1}(t)$ is sketched in the problem 2.2 solution.

The transistor drain-to-source voltage $v_{DS}(t)$ is equal to approximately zero during the first subinterval, when the transistor conducts. During the second subinterval, the transistor is off and the diode conducts. The converter circuit is then as sketched on p.3 of the prob 2.2 solution. It can be seen that

(a) $v_{D1}(t) = v_1(t) + v(t)$ for subinterval 2

small ripple approximation

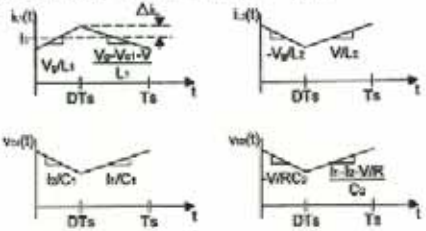
$$\begin{aligned} v_{DS}(t) &\approx V_g - V \\ &= V_g + \frac{D}{D'} V_g \qquad \text{using solution for } V_1 \text{ and } V \\ &= V_g \left(\frac{D'+D}{D'} \right) \qquad \text{with } D'+D = 1 \\ &= \frac{1}{D'} V_g \end{aligned}$$

A caveat: eq (a) above is expressed in terms of quantities that have small ripple: $v_{D1}(t)$ and $v(t)$. We could have instead written $v_{D1}(t) = V_g - v_1(t)$, but the result would not be useful because the switching ripple in $v_1(t)$ is not small and cannot be ignored!

Prob. 2.3
For the Sepic of Phm. 2.2 (above)

Summary

(a) Use $di_L(t)/dt = v_L(t)/L$ and $dv_C(t)/dt = i_C(t)/C$



(Change in x) = (slope)*(length of subinterval)

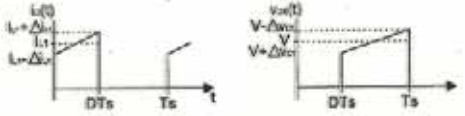
$2\Delta i_{L1} = VgDTs/L_1 \Rightarrow \Delta i_{L1} = VgDTs/2L_1$

$-2\Delta i_{L2} = -VgDTs/L_2 \Rightarrow \Delta i_{L2} = VgDTs/2L_2$

$-2\Delta v_{C1} = I_2DTs/C_1 = -VgD^2Ts/D'RC_1 \Rightarrow \Delta v_{c1} = VgD^2Ts/2D'RC_1$

$-2\Delta v_{c2} = -VDTs/RC_2 = -VgD^2Ts/D'RC_2 \Rightarrow \Delta v_{c2} = VgD^2Ts/2D'RC_2$

(b)



$i_D(t) = I_1 - I_2$

$i_D(t)_{peak} = I_1 + \Delta i_{D1} - I_2 + \Delta i_{D2}$

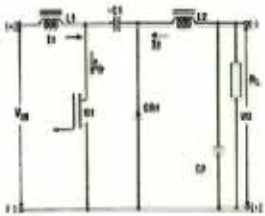
$I_{Dpeak} = (Vg/R)(D/D')^2 + (Vg/R)(D/D') + (L_1+L_2)VgDTs/2L_1L_2$

$v_{DS}(t)_{peak} = v_{C2} + v_{C1} + \Delta v_{c1} + \Delta v_{c2} = Vg/D' + VgD^2Ts(C_1+C_2)/2RD'C_1C_2$

TYPE OF CONVERTER

CUK (Step Up/Down)

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = -\left(\frac{t_{on}}{T_S - t_{on}}\right) = -\left(\frac{D}{1-D}\right)$$

inverting

PEAK DRAIN CURRENT •

$$I_{DMAX} = I_1 + I_2 = I_1\left(\frac{1}{D}\right)$$

PEAK DRAIN VOLTAGE •

$$V_{DS} = 2\,V_{IN}$$

AVERAGE DIODE CURRENTS •

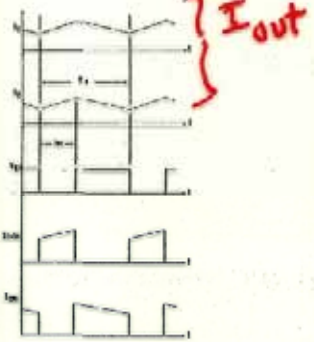
$$I_{CR1} = I_1 + I_2$$

$$I_1 + I_2 = I_1\left(\frac{1}{D}\right)$$

DIODE VOLTAGES (VRM) •

$$V_{RM} = V_O + V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

Simple, low ripple input and output current, capacitive isolation protects against switch failure.

DISADVANTAGES

High drain current. C1 has high ripple current requirement (low ESR). High voltage required for Q1. Voltage inversion.

TYPICAL APPLICATIONS

Low noise, inverse output voltages.

APPLICABLE HARRIS PRODUCTS

HIP5060, HIP5061, HIP5062, HIP5063

Low EMC both i_{IN} & i_{out} are ripple → 0

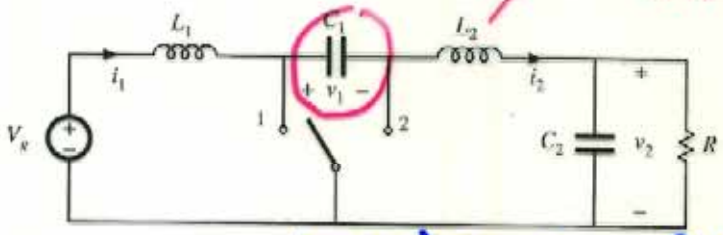
2.4 Cuk converter example

HW Ch 5 #5

$V_L = V_{L1} - V_{L2}$ (left − right)

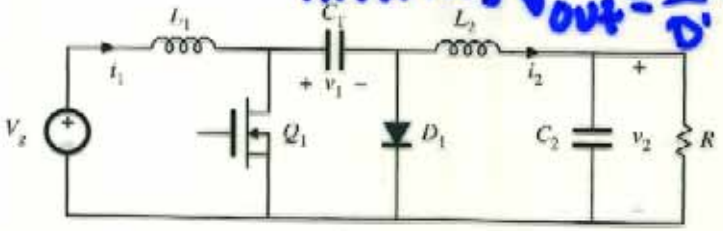
Cuk converter, with ideal switch

Fig 2.20 pg 27



inverting $V_{out} = \frac{D}{D'} V_{in}$

Cuk converter: practical realization using MOSFET and diode



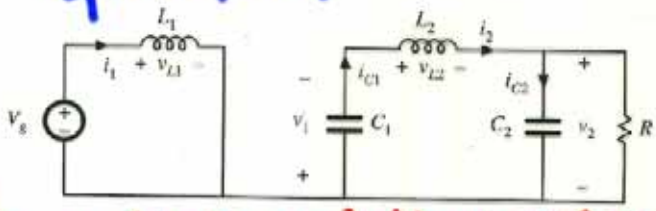
Cuk converter circuit
with switch in positions 1 and 2

Fig 2.21
Pg 28

i_1 ramps up

Switch in position 1:
MOSFET conducts

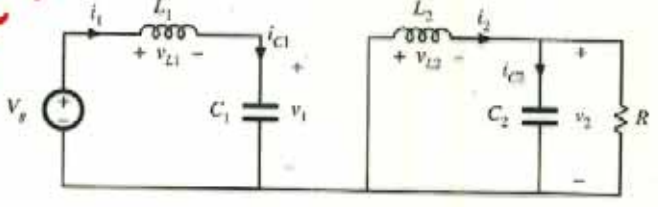
Capacitor C_1 releases energy to output



C_1 is discharged then recharged!

Switch in position 2:
diode conducts

Capacitor C_1 is charged from input



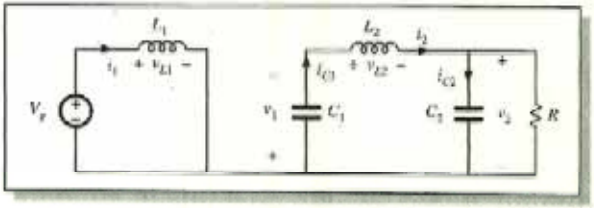
Waveforms during subinterval 1

MOSFET conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g$$
$$v_{L2} = -v_1 - v_2$$
$$i_{C1} = i_2$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$

series leg



Small ripple approximation for subinterval 1:

$$v_{L1} = V_g$$
$$v_{L2} = -V_1 - V_2$$
$$i_{C1} = I_2$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Caps act as "DC sources" for Δt

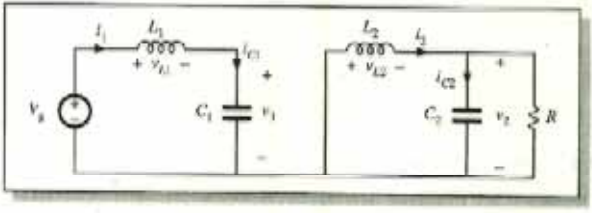
Waveforms during subinterval 2

Diode conduction interval

Q OPEN

Inductor voltages and capacitor currents:

$$v_{L1} = V_g - v_1$$
$$v_{L2} = -v_2$$
$$i_{C1} = i_1$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



Small ripple approximation for subinterval 2:

$$v_{L1} = V_g - V_1$$
$$v_{L2} = -V_2$$
$$i_{C1} = I_1$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Equate average values to zero

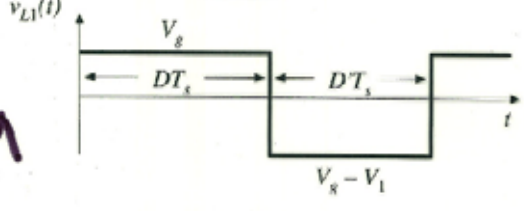
4 Equations from 2L and 2C

The principles of inductor volt-second and capacitor charge balance state that the average values of the periodic inductor voltage and capacitor current waveforms are zero, when the converter operates in steady state. Hence, to determine the steady-state conditions in the converter, let us sketch the inductor voltage and capacitor current waveforms, and equate their average values to zero.

Waveforms:

Inductor voltage $v_{L1}(t)$

Fig 2.22a Pg 29



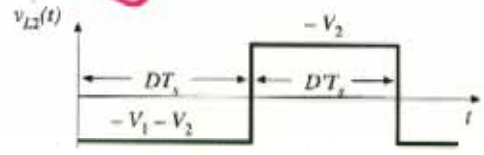
Volt-second balance on L_1:

$$\langle v_{L1} \rangle = DV_g + D'(V_g - V_1) = 0$$

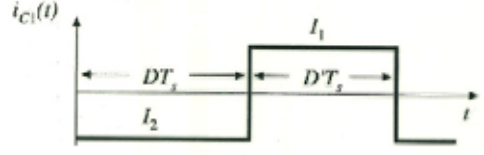
Equate average values to zero

Figs 2.22 b c
Pg 29

Inductor L_2 voltage



Capacitor C_1 current



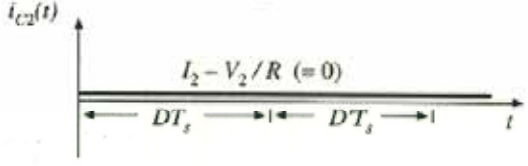
Average the waveforms:

$$\langle v_{L2} \rangle = D(-V_1 - V_2) + D'(-V_2) = 0$$
$$\langle i_{C1} \rangle = DI_2 + D'I_1 = 0$$

Equate average values to zero

Fig 2.22 d
pg 29

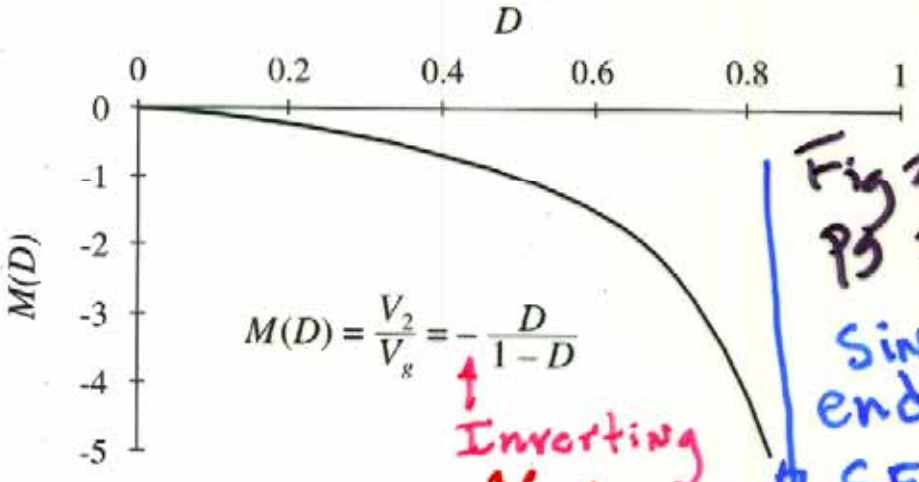
Capacitor current $i_{C2}(t)$ waveform



$$\langle i_{C2} \rangle = I_2 - \frac{V_2}{R} = 0$$

Note: during both subintervals, the capacitor current i_{C2} is equal to the difference between the inductor current i_2 and the load current V_2/R. When ripple is neglected, i_{C2} is constant and equal to zero.

Cuk converter conversion ratio $M = V/V_g$



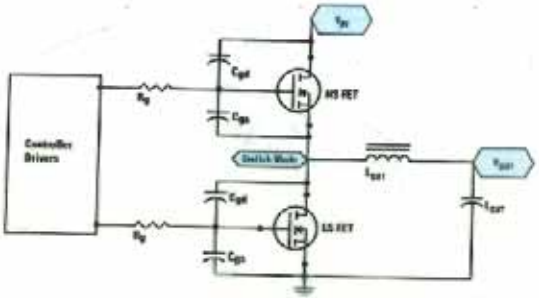


Figure 3. Synchronous Buck Converter

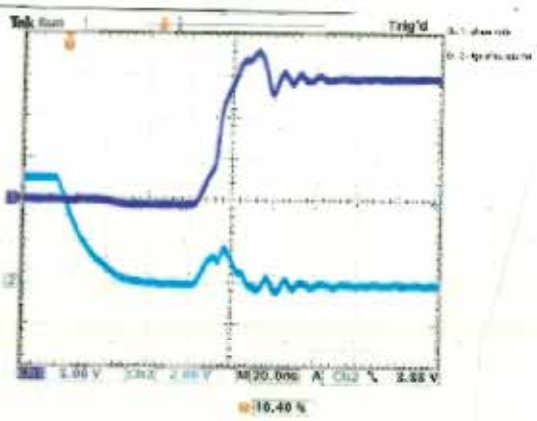


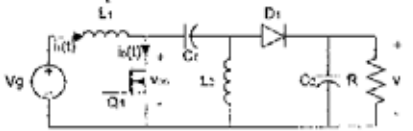
Figure 4. dv/dt induced step on the low-side MOSFET
Ch 1 Switch node
Ch 2 Vgs _ low-side MOSFET

HW #1

Ch. 2 Prob. 2, 3, 4, 6

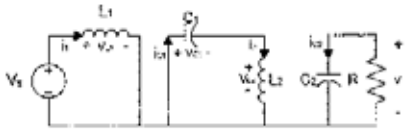
Prob. 2.2

Non-isolated Sepic Converter



(a)

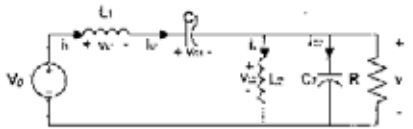
Position 1. Transistor is on and the Diode is off.



$v_{L1} = V_g$, $v_{L2} = -v_{C1}$, $i_{d1} = i_2$, $i_{d2} = -v/R$

Using the small ripple approximation $\Rightarrow v_{L1} = V_g$, $v_{L2} = -V_{c1}$, $i_{d1} = I_2$, $i_{d2} = -V/R$

Position 2. Transistor is off and the Diode is on.

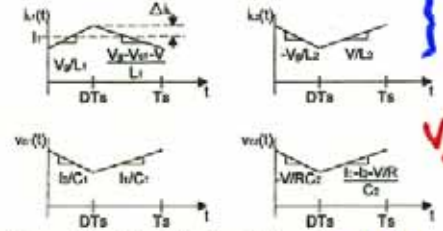


$v_{L1} = V_g - v_{c1} - v$, $v_{L2} = v$, $i_{d1} = i_1$, $i_{d2} = i_2 - v/R$

Using the small ripple approximation $\Rightarrow v_{L1} = V_g - V_{c1} - V$, $v_{L2} = V$, $i_{d1} = I_1$, $i_{d2} = I_2 - V/R$

Prob. 2.3
For the Sepic of Phm. 2.2 (above)

(a) Use $di_k(t)/dt = v_k(t)/L$ and $dv_k(t)/dt = i_k(t)/C$



(Change in x) = (slope)*(length of subinterval)

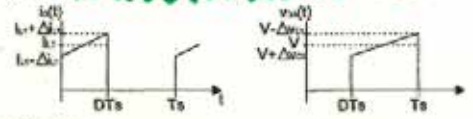
$2\Delta i_{L1} = V_g DT_s/L_1 \Rightarrow \Delta i_{L1} = V_g DT_s/2L_1$

$-2\Delta i_{L2} = -V_g DT_s/L_2 \Rightarrow \Delta i_{L2} = V_g DT_s/2L_2$

$-2\Delta v_{C1} = I_2 DT_s/C_1 = -V_g D^2 T_s/D'RC_1 \Rightarrow \Delta v_{c1} = V_g D^2 T_s/2D'RC_1$

$-2\Delta v_{C2} = -VDT_s/RC_2 = -V_g D^2 T_s/D'RC_2 \Rightarrow \Delta v_{c2} = V_g D^2 T_s/2D'RC_2$

(b)

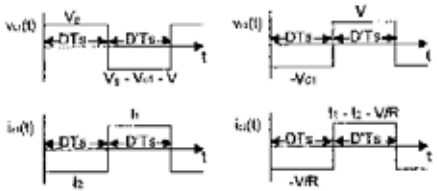


$i_D(t) = I_1 - I_2$

$i_{D(t)peak} = I_1 + \Delta i_{D1} - I_2 = \Delta i_{D2}$

$I_{D,rms} = (V_g/R)(D/D')^2 + (V_g/R)(D/D') + (L_1+L_2)V_g DT_s/2L_1L_2$

$v_{DS}(t)_{max} = v_{C2} + v_{C1} + \Delta v_{c1} + \Delta v_{c2} = V_g/D' + V_g D^2 T_s(C_1+C_2)/2RD'C_1C_2$



Equating the DC components of the above waveforms to zero and knowing $D' = 1 - D$:

$\langle v_{L1} \rangle = DV_g + D'(V_g - V_{c1} - V) = 0$

$\langle v_{L2} \rangle = D(-V_{c1}) + D'V = 0$

$\langle i_{c1} \rangle = DI_2 - D'I_1 = 0$

$\langle i_{c2} \rangle = D(-V/R) + D'(I_1 - I_2 - V/R) = 0$

The solution to this system of equations for the DC components of the capacitor voltages and the inductor currents yields:

$\mathbf{V_{c1} = V_g}$

$\mathbf{V_{c2} = V = DV_g/D' = DV_g/(1-D)}$

$\mathbf{I_{L1} = I_1 = (D/D')^2V_g/R}$

$\mathbf{I_{L2} = I_2 = -DV_g/D'R}$

(b) Known: $V = 28$ volts, $18v \le Vg \le 36v$, $I_{load} = 2A$

(c) We have the following equation relating D, Vg, and V which we can use to solve for D:

$V = DVg/(1-D)$ solving for D yields $\Rightarrow D = V/(V+Vg)$.

Substituting in the knowns gives the range for $D \Rightarrow \mathbf{0.4375 \le D \le 0.6078}$

(d) We know the load current and voltage thus we can get the resistance

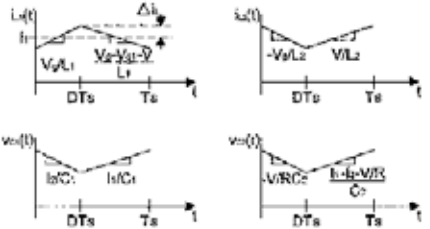
$R = V/I = 28v/2A = 14\Omega$.

We found the range for D in Part 1 and the resistance was just calculated so we can derive a range for the current I_1 using the equation from part a.

$I_1 = (D/(1-D))^2Vg/R \Rightarrow \mathbf{1.56A \le I_1 \le 3.11A}$

Prob. 2.3
For the Sepic of Phm. 2.2 (above)

(a) Use $di_L(t)/dt = v_L(t)/L$ and $dv_c(t)/dt = i_c(t)/C$



(Change in x) = (slope)*(length of subinterval)

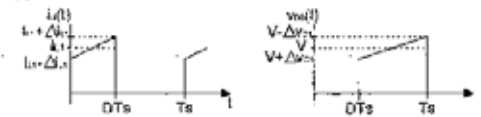
$2\Delta i_{L1} = V_g DTs/L_1 \Rightarrow \Delta i_{L1} = V_g DTs/2L_1$

$-2\Delta i_{L2} = -V_g DTs/L_2 \Rightarrow \Delta i_{L2} = V_g DTs/2L_2$

$-2\Delta v_{c1} = I_2 DTs/C_1 = -V_g D^2 Ts/D'RC_1 \Rightarrow \Delta v_{c1} = V_g D^2 Ts/2D'RC_1$

$-2\Delta v_{c2} = -VDTs/RC_2 = -V_g D^2 Ts/D'RC_2 \Rightarrow \Delta v_{c2} = V_g D^2 Ts/2D'RC_2$

(b)



$i_D(t) = I_1 - I_2$

$i_{D(t)peak} = I_1 + \Delta i_{L1} - I_2 + \Delta i_{L2}$

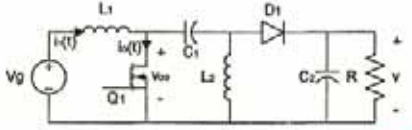
$i_{Dpeak} = (V_g/R)(D/D')^2 - (V_g/R)(D/D') + (L_1+L_2)V_g DTs/2L_1L_2$

$v_{DS}(t)_{peak} = v_{C2} - v_{C1} + \Delta v_{c1} + \Delta v_{c2} = V_g/D' + V_g D^2 Ts(C_1+C_2)/2RD'C_1C_2$

Hints

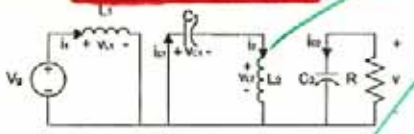
HW #1
Ch. 2 Prob. 2, 3, 4, 6

Prob. 2.2
Non-isolated Sepic Converter



(a)

Position 1. Transistor is on and the Diode is off.

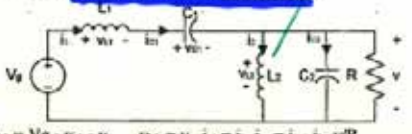


$v_{L1} = V_g$, $v_{L2} = -v_{c1}$, $i_{c1} = i_2$, $i_{d2} = -v/R$

Using the small ripple approximation $\Rightarrow v_{L1} = V_g$, $v_{L2} = -V_{c1}$, $i_{c1} = I_2$, $i_{d2} = -V/R$

different assumption for i_2

Position 2 Transistor is off and the Diode is on.



$v_{L1} = V_g - v_{c1} - v$, $v_{L2} = v$, $i_{d1} = i_1$, $i_{d2} = i_1 - i_2 - v/R$

Using the small ripple approximation $\Rightarrow v_{L1} = V_g - V_{c1} - V$, $v_{L2} = V$, $i_{c1} = I_1$, $i_{d2} = I_1 - I_2 - V/R$

Assume FET (ON / off) diode (off / ON)

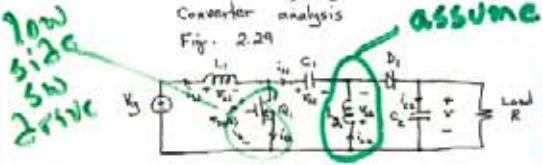
L_1, L_2, C_2, C_1 are big!

Tutorial

Solutions to Problem 2.2

A dc voltage regulator based on the SEPIC converter analysis

Fig. 2.29



A comment: Label voltage and current for each inductor and capacitor. Defined directions of current and voltage must be consistent:

(2):  i flows from + to −

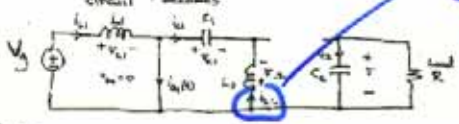
v_{C1}

First subinterval: 0 < t < D_1T_s

transistor is on, diode is off

circuit becomes

arbitrary even "wrong"



A comment: Note: be careful to be consistent in your defined polarities of voltage and current. The same polarities must be followed during all subintervals!

Hint!

Inductor voltages and capacitor currents for this subinterval:

$$v_{L1}(t) = V_g, \quad v_{L2}(t) = v_{C1}(t), \quad i_{C1}(t) = -i_{L2}(t),$$
$$i_{C2}(t) = -v(t)/R$$

so $\sum i = 0$ @ node

so $\sum i = 0$ @ node

Second subinterval: $DT_s \le t \le T_s$

transistor is off, diode is on

Circuit becomes

Inductor voltages and capacitor currents for this subinterval:

$$v_{L1}(t) = V_g - v_{C1}(t) - v(t) \qquad \text{new } V_{L1}$$

$$v_{L2}(t) = -v(t) \qquad \text{new } V_{L2}$$

$$i_{C1}(t) = i_{L1}(t)$$

$$i_{C2}(t) = i_{L1}(t) + i_{L2}(t) - v(t)/R$$

Again, note that v_{L1}, v_{L2}, i_{C1}, and i_{C2} are expressed in terms of quantities that have small ripple (i.e., $i_{L1}(t)$, $i_{L2}(t)$, $v_{C1}(t)$, $v(t)$, and V_g) and not as functions of quantities whose ripples are not small (such as $v_{L1}(t)$, $v_{L2}(t)$, $i_{C1}(t)$, $i_{C2}(t)$, and $i_g(t)$). Use of the small ripple approximation now leads to

$$v_{L1}(t) \approx V_g - V_{C1} - V$$

$$v_{L2}(t) \approx -V$$

$$i_{C1}(t) \approx I_{L1}$$

$$i_{C2}(t) \approx I_{L1} + I_{L2} - V/R$$

Note that each inductor voltage and capacitor current has been expressed in terms of quantities that have small ripple when L_1, L_2, C_1, and C_2 are sufficiently large. We can therefore make the small ripple approximation and write

$$i_{L1}(t) \approx I_{L1}$$
$$v_{C1}(t) \approx V_{C1}$$
$$i_{L2}(t) \approx I_{L2}$$
$$v(t) \approx V$$

So we obtain

$$v_{L1}(t) = v_g$$
$$v_{L2}(t) \approx V_{C1}$$
$$i_{C1}(t) \approx -I_{L2}$$
$$i_{C2}(t) \approx -V/R$$

best choice only

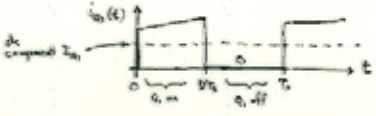
CAREFUL

A comment

We could have written the equations for subinterval 1 in other ways. For example, we could have expressed $i_{C1}(t)$ as

$$i_{C1}(t) = i_{L2}(t) - i_{g2}(t)$$

While this equation is true, it is not useful because the switching ripple in the transistor current $i_{g2}(t)$ is not small:



So we cannot write $i_{g2}(t) \approx I_{g2}$ for subinterval 1

!