ECE 562

Week 2 Lecture 2

Week 2 Lecture 2 Summary

- Section notes
  - Slides 3-7 – Converter applications
  - Slides 8-18 – Improving waveforms
  - Slides 19-21 – Commercial apps and
  - Slides 22-32 – Resonant converters
  - Slides 34-53 –Ripple characteristics and calculations
  - Slides 54-61- Circuit topology and losses

LECTURE 4

Introduction to Power Electronics Circuit Topologies: The Big Three

I. **POWER ELECTRONICS CIRCUIT TOPOLOGIES**
   - A. **OVERVIEW** last time
   - B. BUCK TOPOLOGY
   - C. BOOST CIRCUIT
   - D. BUCK - BOOST TOPOLOGY — HW 2.1
   - E. COMPARISION OF THE BIG THREE

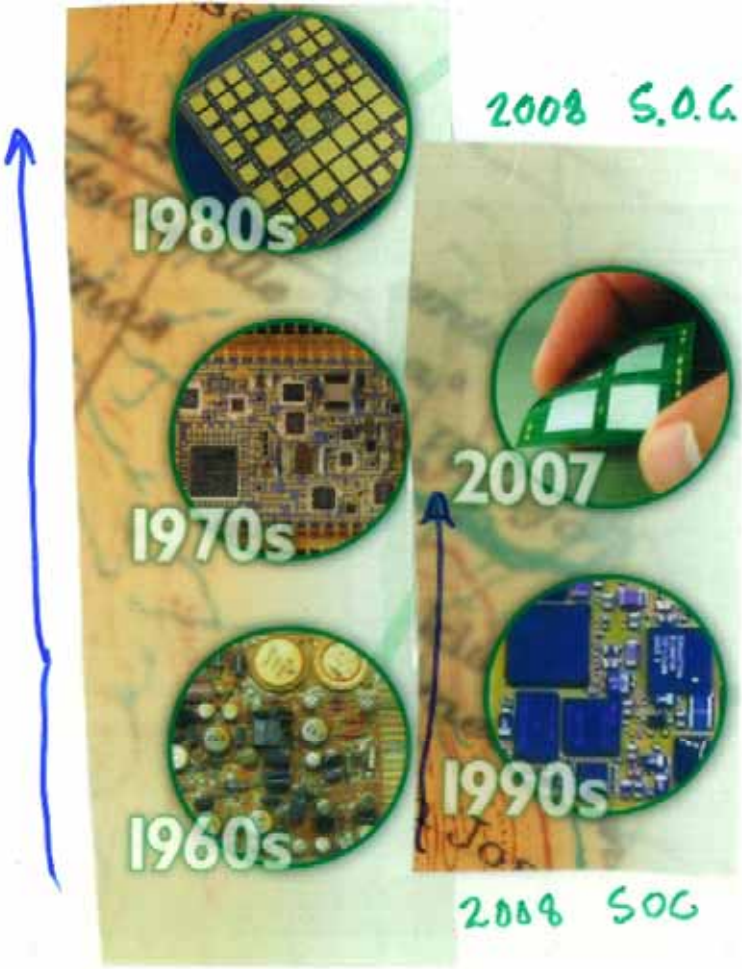
II. **TOPOLOGY OF L-C OUTPUT FILTERS**
   - A. C ALWAYS Located ACROSS V_{out}
   - B. L LOCATED BETWEEN CRUDE UNFILTERED V_{dc} AND STABILIZED V_{out}
     1. BUCK
     2. BOOST
     3. BUCK-BOOST
     4. LOW RIPPLE APPROXIMATION FOR OUTPUT SIGNALS AT f_{sw}
        a) INDUCTOR RIPPLE:

$$\Delta I = \frac{V}{L} dt(\text{switch})$$

        b) CAPACITOR RIPPLE:

$$\Delta V = \frac{I}{C} dt(\text{switch})$$

dt(switch)=(Duty cycle)*T_s(period of f_{sw})



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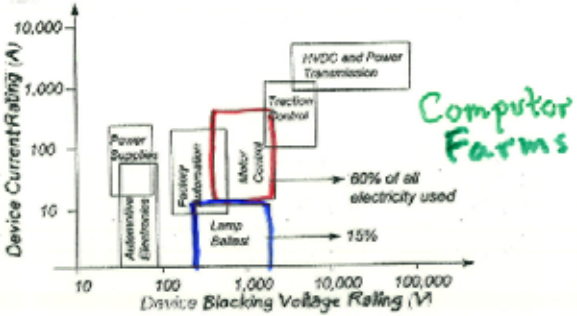
Talk #2

562 Notes on Web CSU 562

TWO MAJOR APPLICATIONS OF POWER ELECTRONICS: INDUSTRIAL ELECTRONICS

A. Overview

POWER ELECTRONICS USES NEW SWITCHING CIRCUIT TOPOLOGIES TO MAKE SMALLER, LOWER WEIGHT AND HIGHER EFFICIENCY POWER SUPPLIES. These supplies for the first time are available at variable frequencies need for applications in motor drive and in lighting which together constitute over 75% of electricity use.



Clearly, we have different applications that place specific requirements on the solid state ¬witches. Only as advances in solid state switches occurred could these new applications become cost effective. Switch technology is an enabling one for new applications. Two issues are enabling: electrical peformance and cost.

B. Improved Motor Control

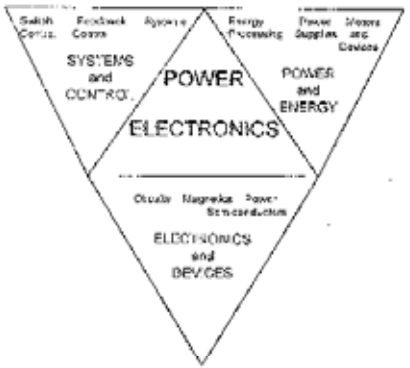
Objectives of this chapter

- Develop techniques for easily determining output voltage of an arbitrary converter circuit
- Derive the principles of *inductor volt-second balance* and *capacitor charge (amp-second) balance*
- Introduce the key *small ripple approximation*
- Develop simple methods for selecting filter element values
- Illustrate via examples

HW#1: Thinking question #2

Give some general trends for the small ripple approximation in a simple L-C output filter for increasing switch frequency f_{sw} (i.e. smaller t_s). Show that a smaller "C" is allowed for fixed I drawn at the load and chosen Δv levels. Do a similar argument for the inductor size required

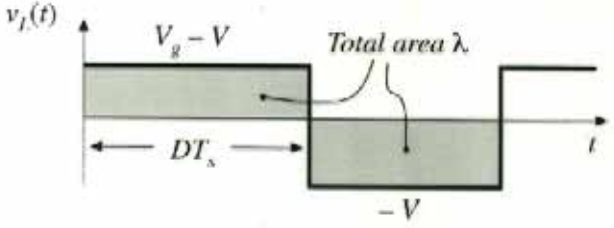
Now we can better appreciate the following chart which trys to depict all the aspects of ee that power electronics brings together to work on one topic energy conversion: controls, power, parasitic elements, and electronic devices to name a few.



Buck Circuit ?

Inductor volt-second balance: Buck converter example

Inductor voltage waveform, previously derived:



Integral of voltage waveform is area of rectangles:

$$\lambda = \int_0^{T_s} v_L(t)\,dt = (V_g - V)(DT_s) + (-V)(D'T_s)$$

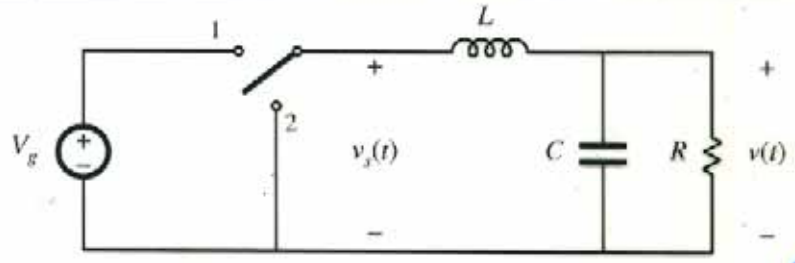
Average voltage is

$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V)$$

Equate to zero and solve for V:

$$0 = DV_g - (D + D')V = DV_g - V \quad \Rightarrow \quad V = DV_g$$

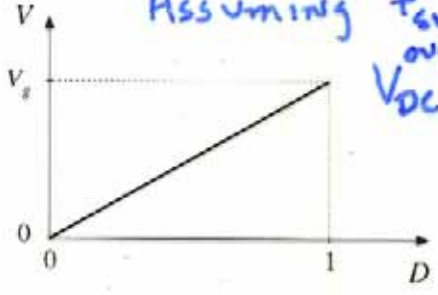
Insertion of low-pass filter to remove switching harmonics and pass only dc component



Assuming $f_{sw} \uparrow$ $T_{sw} \downarrow$

V_{DC}^{out} (eff)

$$v \approx \langle v_s \rangle = DV_g$$



The principle of inductor volt-second balance: Derivation

Inductor defining relation:

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Integrate over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L} \int_0^{T_s} v_L(t)\, dt$$

In periodic steady state, the net change in inductor current is zero:

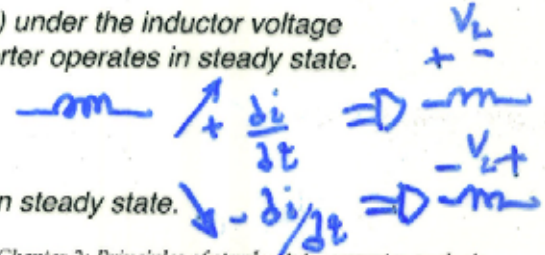
$$0 = \int_0^{T_s} v_L(t)\, dt$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state.

An equivalent form:

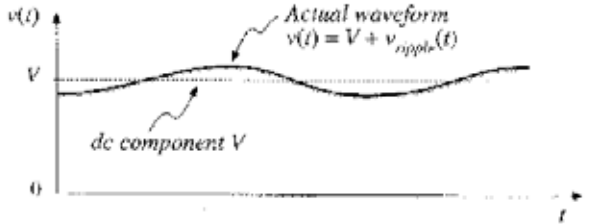
$$0 = \frac{1}{T_s} \int_0^{T_s} v_L(t)\, dt = \langle v_L \rangle$$

The average inductor voltage is zero in steady state.



The small ripple approximation

$$v(t) = V + v_{ripple}(t)$$

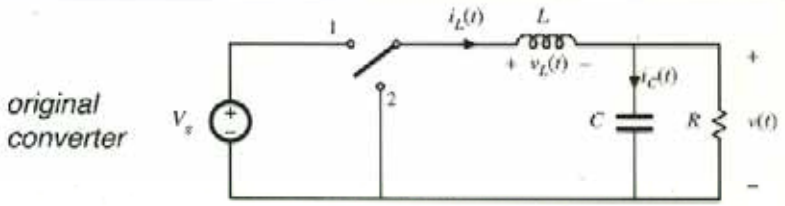


In a well-designed converter, the output voltage ripple is small. Hence, the waveforms can be easily determined by ignoring the ripple:

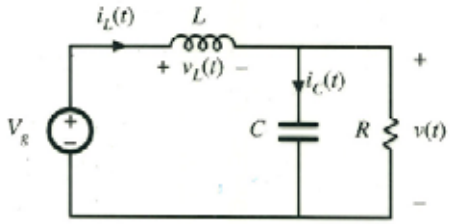
$$\left| v_{ripple} \right| \ll V$$

$$v(t) \approx V$$

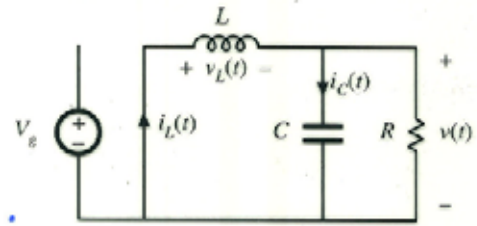
Buck converter analysis: inductor current waveform



switch in position 1



switch in position 2



$\frac{V_g - V_o}{L} DT_{sw} \rightarrow \Delta i \uparrow$ $\quad \frac{V}{L} D'T_{sw} \Rightarrow \Delta i \downarrow$

$T = \frac{1}{f_{sw}}$ $\quad (1-D)T = \frac{1}{f_{sw}}$

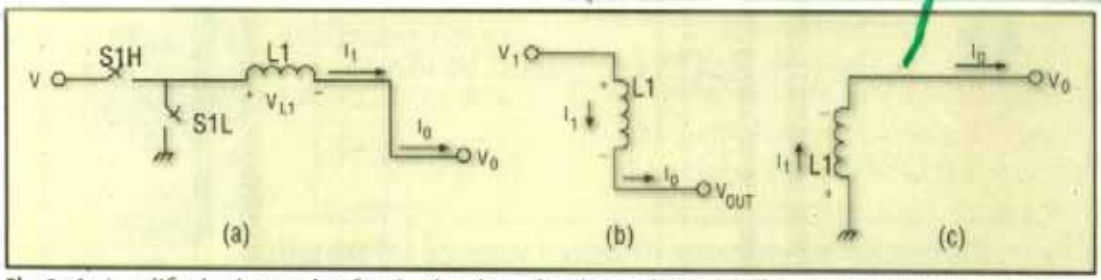
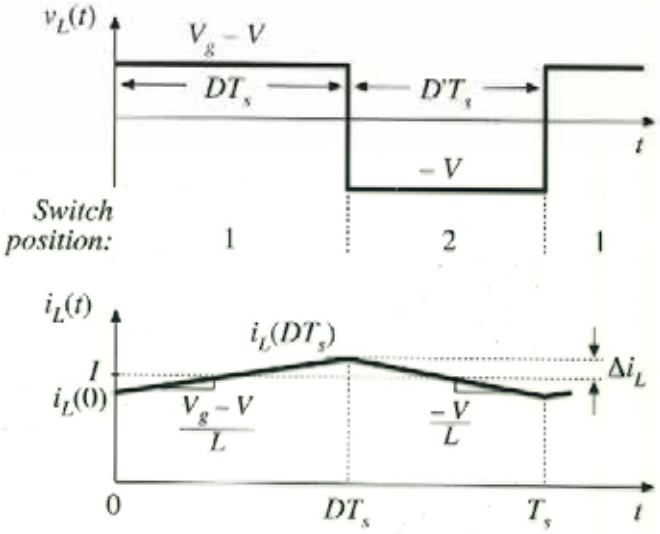


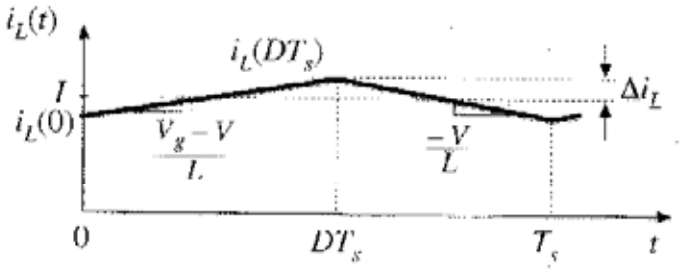
Fig. 1. *A simplified schematic of a single-phase buck regulator (a) illustrates its two states of operation. In state one, S1H is closed and S1L is open, so that the input sources energy to the output and L1 stores energy (b). In state two, S1L is closed and S1H is open, so that L1 sources energy to the load (c).*

Inductor voltage and current waveforms



$$v_L(t) = L\frac{di_L(t)}{dt}$$

Determination of inductor current ripple magnitude



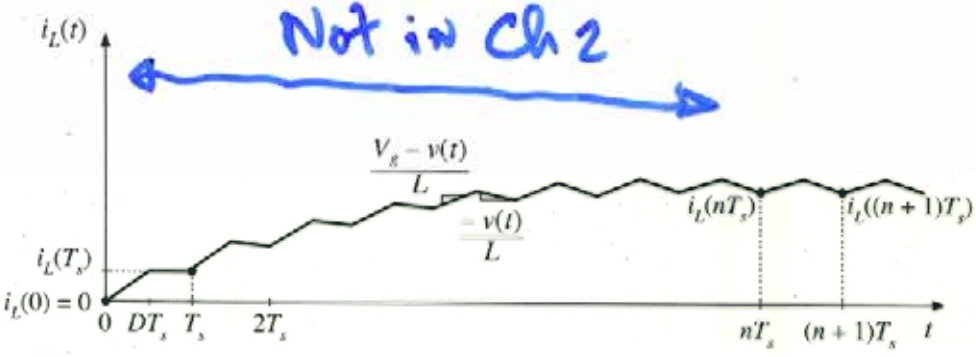
$$(\text{change in } i_L) = (\text{slope})(\text{length of subinterval})$$

$$\left(2\Delta i_L\right) = \left(\frac{V_g - V}{L}\right)\left(DT_s\right)$$

$$\Rightarrow \qquad \Delta i_L = \frac{V_g - V}{2L} DT_s \qquad\qquad L = \frac{V_g - V}{2\Delta i_L} DT_s$$

Spice HW

Inductor current waveform during turn-on transient



When the converter operates in equilibrium:

$$i_L((n+1)T_s) = i_L(nT_s)$$

fixed V_o over wide range I_{out}

Wide Range V_{IN}

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#6 Variation

fixed

How accomplished?

Complete, Quick & Ready.

Features

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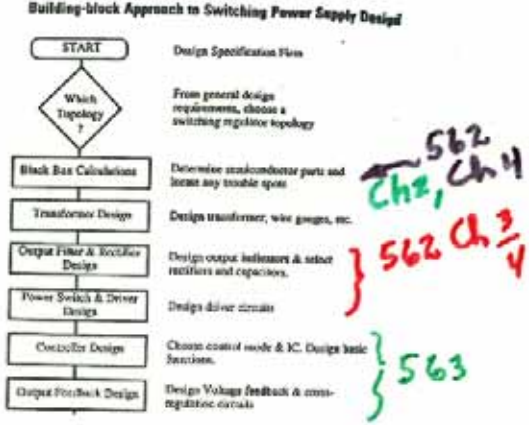
- Pb-Free (e^4), RoHS Compliant
- Only C_{BULK} Required
- Standard and High Voltage:
  LTM4600EV: $4.5V \leq V_{IN} \leq 20V$
  LTM4600HVEV: $4.5V \leq V_{IN} \leq 28V$
- $0.6V \leq V_{OUT} \leq 5V$
- I_{OUT}: 10A DC, 14A Peak
- Parallel Two µModules for 20A Output

Web notes L4



From the above approach we need to pick a starting point. We will focus next of the output filter design in the remainder of this lecture and in lectures 5 and 6.

E. BASIC TOPOLOGIES OF PASSIVE L-C FILTERS

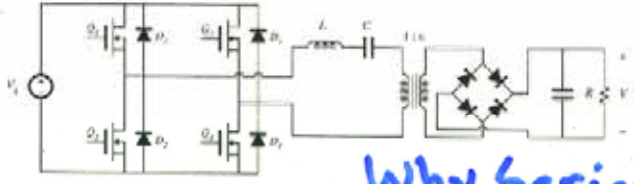
We will use L-C filters both to remove v_{ac} signals lost to conversion and to avoid kvl and kil law violations from the switching.

1. DC OUTPUT REACTIVE FILTER (L-C). This places a series L between two voltages sources v_{in} and v_{out}. It also removes or reduces the switch signal at f_s and passes only dc if designed properly. lets look at the two

Part V. Resonant converters

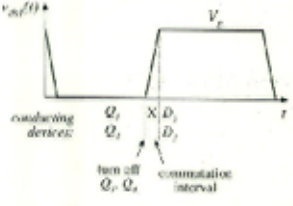
The series resonant converter

How get a Buck



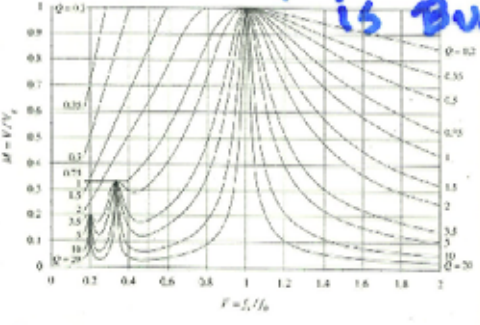
Why Series LC is Buck

Zero voltage switching



Sw loss → 0

Dc characteristics



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Talk #1, #2
HW 2.1

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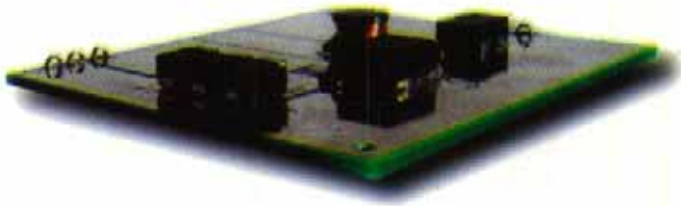
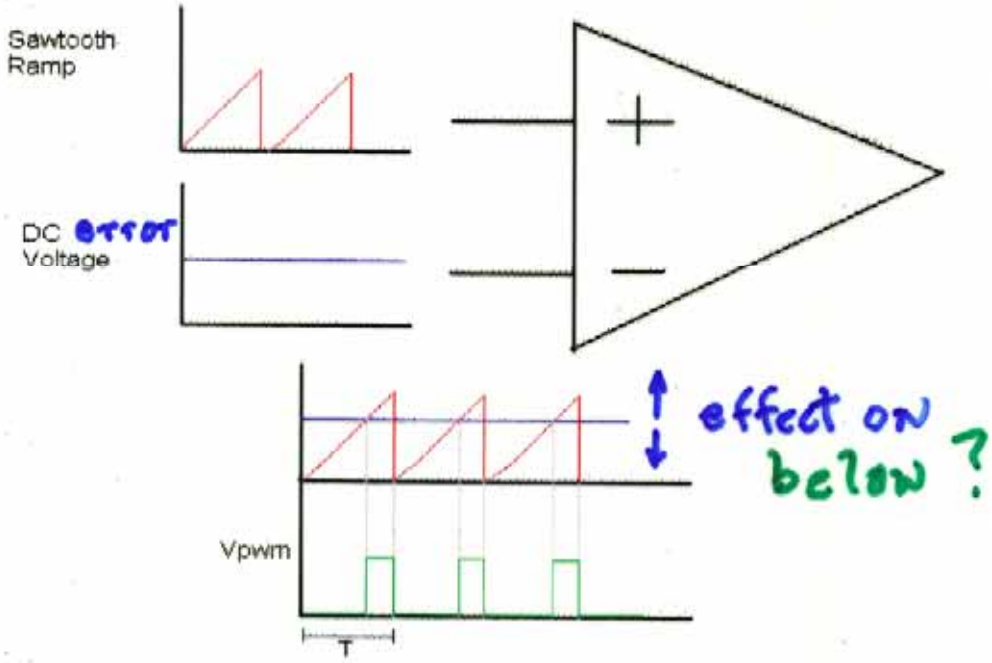


Sawtooth on (+) of D. A.

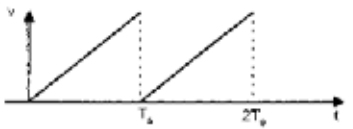


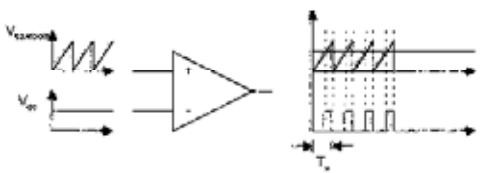
- HENCE FOR A PULSED SWITCH SIGNAL THE AVERAGE DC OUTPUT VOLTAGE MAGNITUDE WILL BE VARIED BY THE CHOICE OF D (OR D')
- how does an electrical engineer easily achieve both arbitrary switching frequency f_s and a variable d/d' ratio? that is achieve control from $0 < d < 1$?

FOR HW#1 - COME UP WITH A SIMPLE CIRCUIT TO GET f_{sw} AND D CONTROL, THEN COMPARE YOURS TO THE FOLLOWING COMPARATOR CIRCUIT SOLUTION. the comparator looks at two input signals, one dc and one ac.

THE AC WAVE SETS f_{sw} BUT THE DC LEVEL SETS THE DUTY CYCLE

- $V_{IN}(1)$: CHOSEN DC REF. VALUE SETS D/D' RATIO
- $V_{IN}(2)$: SAWTOOTH WAVE SETS f_s
- f_{sw} = SWITCHING FREQUENCY





COMPARATOR

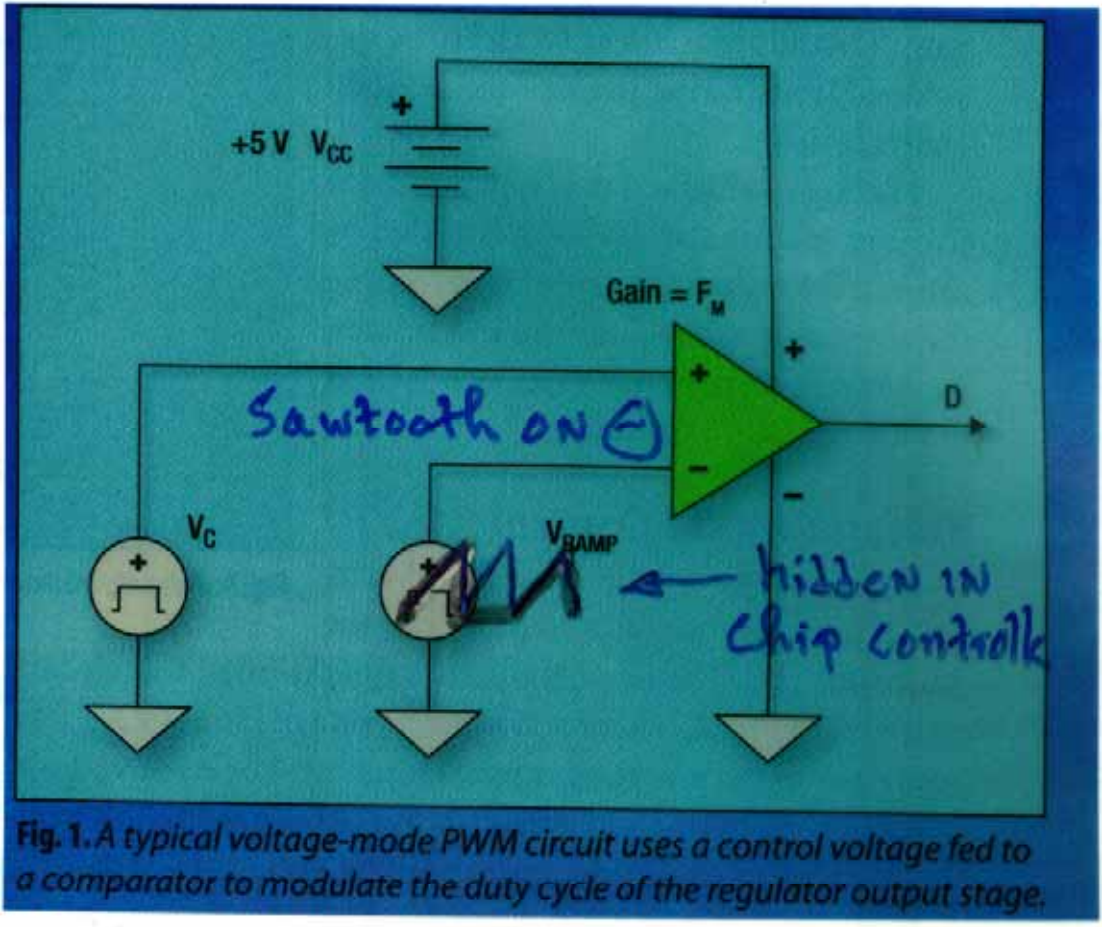


Fig. 1. *A typical voltage-mode PWM circuit uses a control voltage fed to a comparator to modulate the duty cycle of the regulator output stage.*

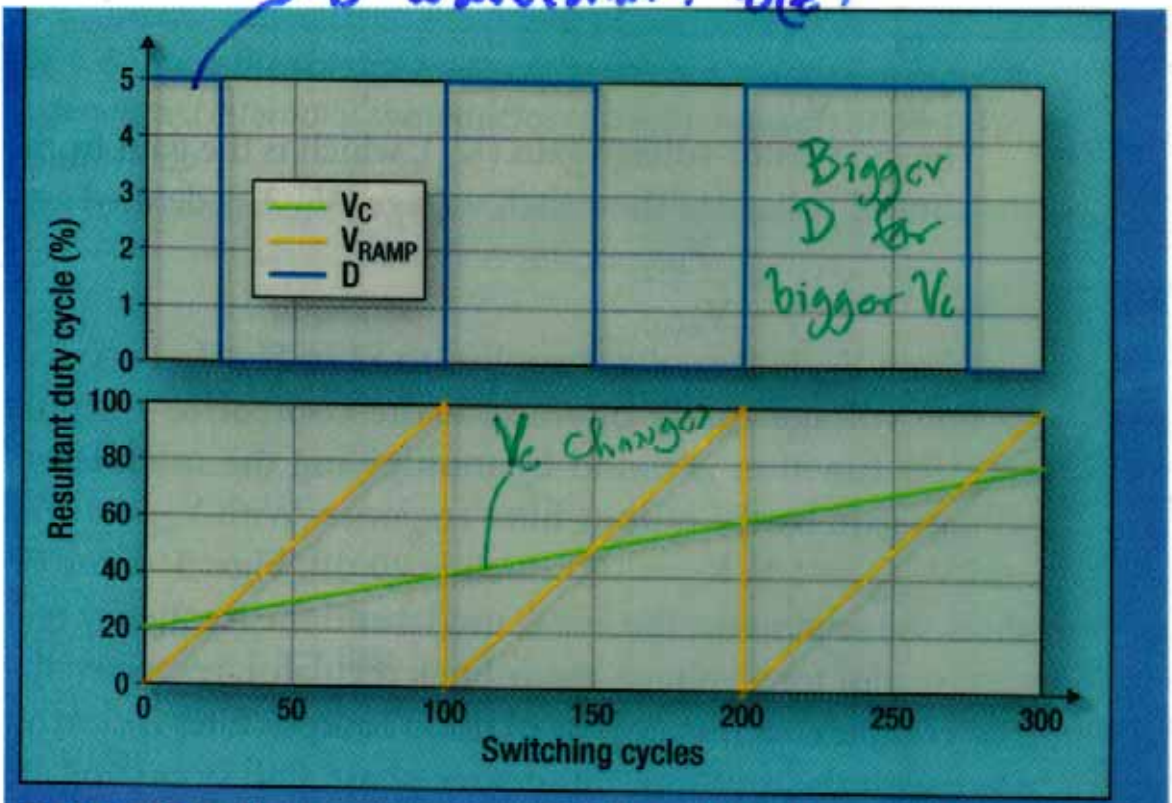


Fig. 2. *For fixed-frequency operation, an increase in the control voltage causes an increase in the duty cycle of the output of the Fig. 1 circuit.*

Picking C issues

ESR comparison	Tantalum 2.2 mF, 6.3 V	EDLC 2.2 mF, 4.5 V
ESR, 100 kHz; 25°C	35 mΩ	200 mΩ
Operating temp range	-55°C to +85°C	-20°C to +70°C
Temp range for comparison	-20°C to +70°C	-20°C to +70°C
Variation over temp range	0%	400%
Variation over time	0%	300%

Table 3. *ESR performance.*

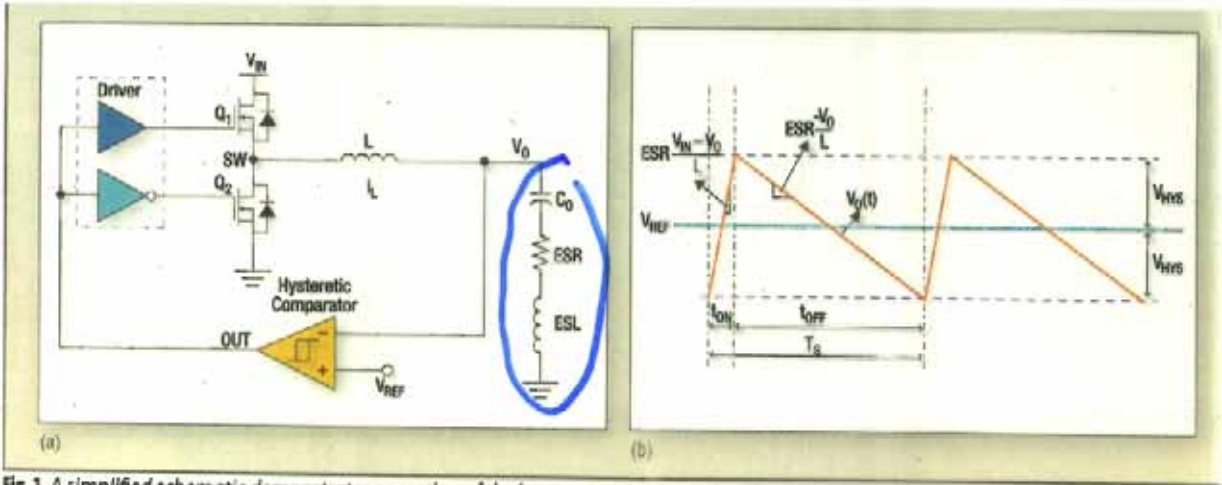


Fig. 1. *A simplified schematic demonstrates operation of the hysteretic voltage-mode voltage regulator (a) with waveforms (b) depicting ideal operation.*

Which is worse

C_O introduces $\frac{I}{C}\underbrace{\frac{D}{f_{SW}}}dt \sim \Delta V$ — Δ wave ripple

ESR introduces $\Delta i_L R$ — Δ wave ripple

ESL introduces $\underbrace{\frac{\partial i_L(t)}{\partial t}}_{\square\text{-wave}} * L$ — □-wave ripple

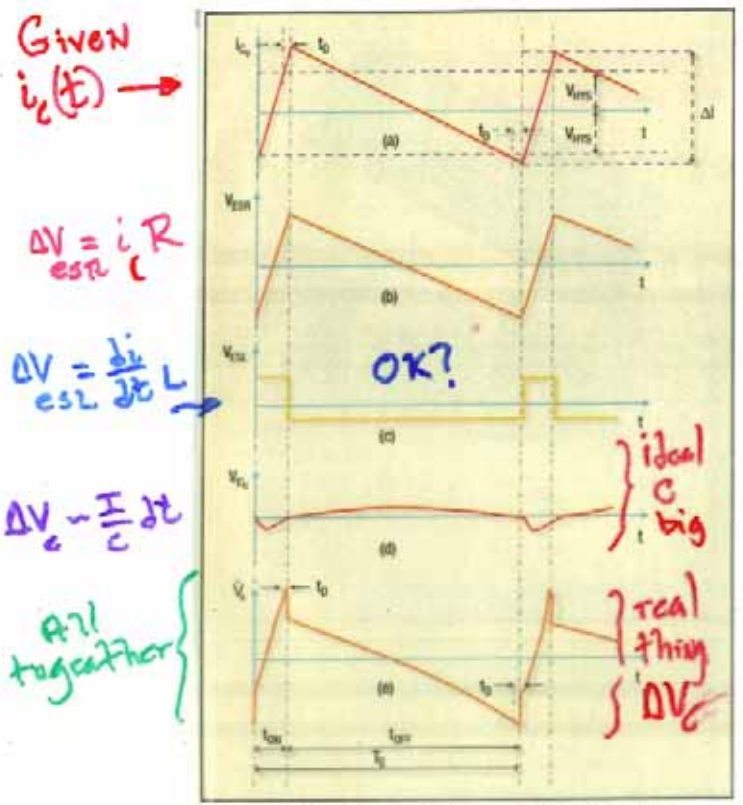


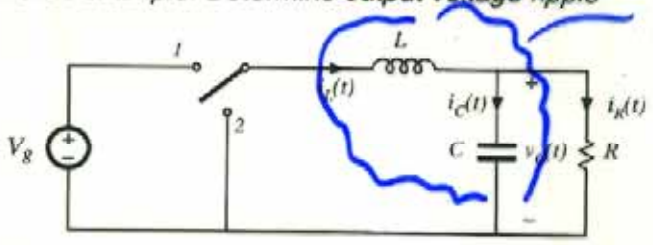
Fig. 2. *A current through the output capacitor (a) produces three separate ripple voltage waveforms—the voltage across the ESR (b), the voltage across the ESL (c) and the voltage across an ideal capacitor with an initial value at the beginning of the high-side Q1 on-time (d). The sum of these three voltages is the composite output voltage ripple (e).*


Catch
design
flaws
before
they
burn
you.

2.5 Estimating ripple in converters containing two-pole low-pass filters

Pbm 2.6 requires this

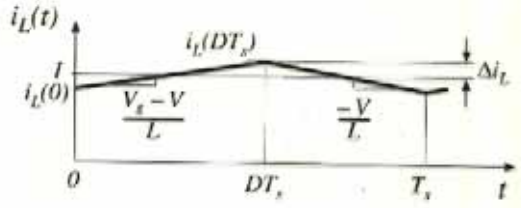
Buck converter example: Determine output voltage ripple



Linear small signal ripple? $\Delta i_L \ll I_{DC}$

Inductor current waveform.

What is the capacitor current?



"L" acts as flywheel blends I_a & I_D

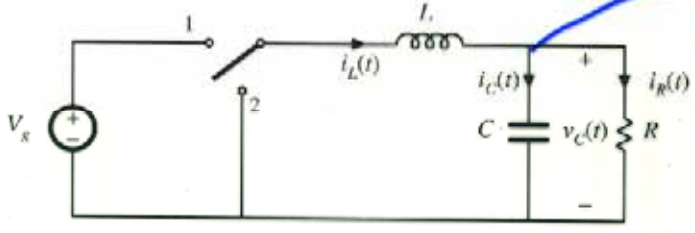
Page 32 text

Δi ~ I Case

2.5 Estimating ripple in converters containing two-pole low-pass filters

For I > Δi

Buck converter example: Determine output voltage ripple



dV/dt = ?

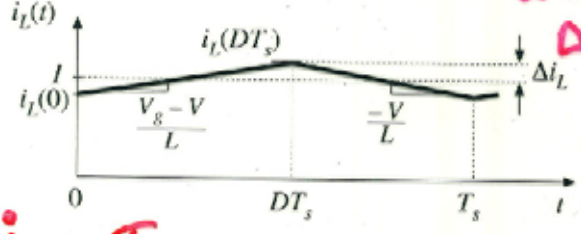
1st Approx

2nd Approx

What if Δi ≈ I_{DC} Must analyze new

Inductor current waveform.

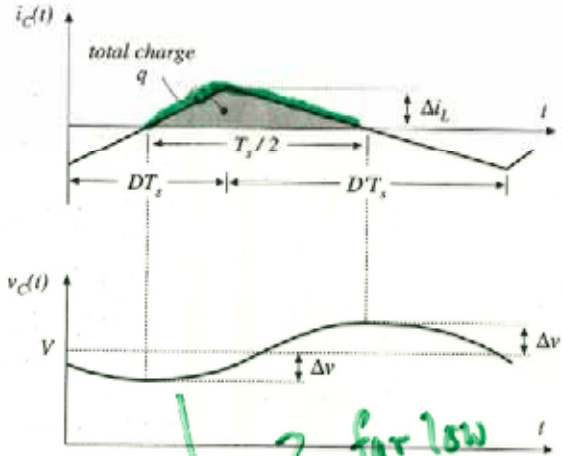
What is the capacitor current?



DCM Δi > I_{DC}

$\int i dt$ = area $\Delta = \frac{1}{2} BH$

Estimating capacitor voltage ripple Δv



Current $i_C(t)$ is positive for half of the switching period. This positive current causes the capacitor voltage $v_C(t)$ to increase between its minimum and maximum extrema. During this time, the total charge q is deposited on the capacitor plates, where

$$q = C\,(2\Delta v)$$

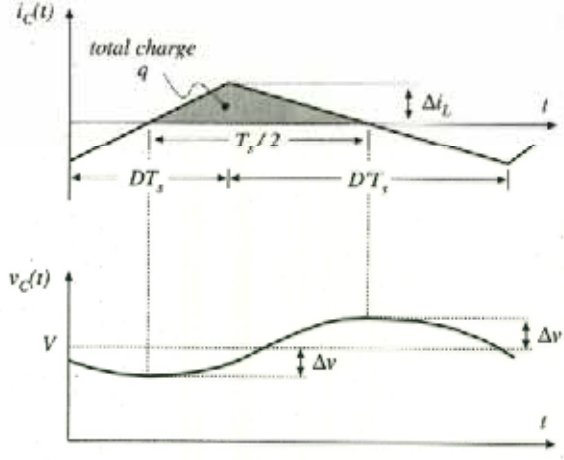
(*change in charge*) = C (*change in voltage*)

Key!

Vs. for Δi_L

? How determine

Estimating capacitor voltage ripple Δv



The total charge q is the area of the triangle, as shown:

$$q = \frac{1}{2} \Delta i_L \left(\frac{T_s}{2} \right)$$

Eliminate q and solve for Δv:

$$\Delta v = \frac{\Delta i_L T_s}{8 C}$$

Note: in practice, capacitor equivalent series resistance (esr) further increases Δv.

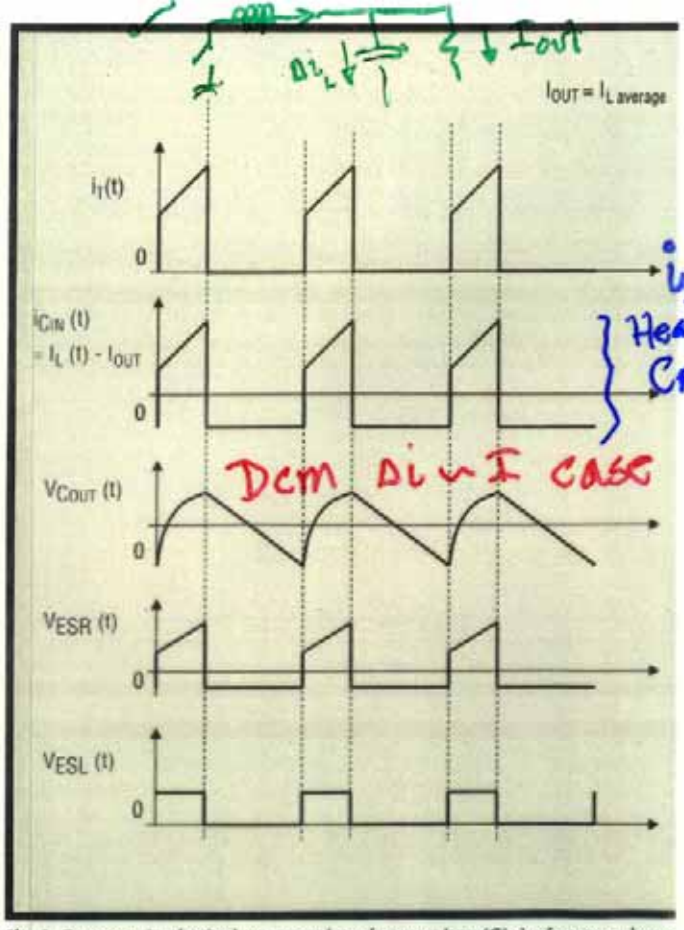
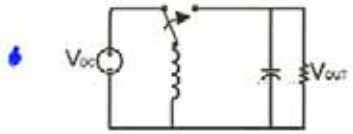


Fig. 4. *Currents in the inductor and tank capacitor (Cin) of a step-down converter*

web my notes

C. BUCK-BOOST TOPOLOGY:

Inductor is connected in parallel with C which acts as a polarity reverser. Given $+v_{dc}$ as input in we generate $-v_{dc}$ out for a switch duty cycle of ½. Many analog circuits require both + and - v_{dc} supplies and this is an easy way to do it.

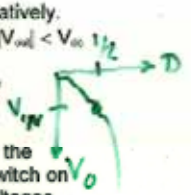


the inductor I again avoids kvl violations by acting as a current source temporarily.

- V_{out}(MINIMUM) IS NOW ZERO
- V_{out} IS OPPOSITE POLARITY TO v_{dc} due to current direction in the inductor that charges the c.
- $\int \frac{V_{dc}}{L} dt = \Delta i_L \Rightarrow i_L$ DOES NOT CHANGE

instantaneously so the capacitor charges negatively.

- FOR BUCK-BOOST EITHER $|V_{out}| > V_{dc}$ OR $|V_{out}| < V_{dc}$ IS POSSIBLE
- $V_{out} / V_{in} = -D / (1-D)$, non-linear dependence on d will be shown in lectures 5-7



On the following page we show schematically the waveforms for the buck/boost circuit for both the switch on and the switch off. Again the ability to generate voltages above the input voltage comes at the price of expensive solid state switches. With the switch on we need to pass nearly 6 times the average current. With the switch off we need to stand off across the switch V(in) + V(out).

Analysis
Design
Costing

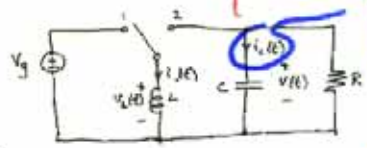
$\Sigma i_{iN} = 0$

$-i_L - i_C - i_R = 0$

?

Solution to Problem 2.1

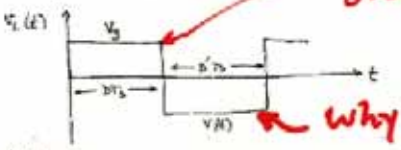
Analysis and Design of a buck-boost converter



Why choose this way?

a)

Inductor voltage waveform



why no V droop

Why negative

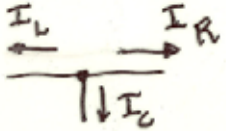
volt-second balance

$\langle v_L(t) \rangle = D(V_g) + D'(-V) \approx DV_g + D'V = 0$

small ripple approximation

solve for V:

$V = -\frac{D}{D'} V_g$



Current node

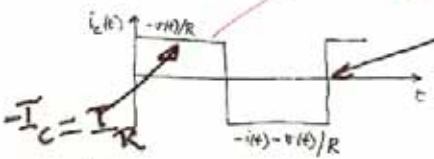
in +

out −

$-I_C - I_L - I_R \equiv 0$

Why NO i_C droop

Capacitor current waveform



$I_C = -I_L - I_R$

$-I_C = I_R$

Capacitor charge balance

I (inductor)

$$\langle i_C(t) \rangle = D\left(-\frac{v(t)}{R}\right) + D'\left(-i(t) - \frac{v(t)}{R}\right)$$

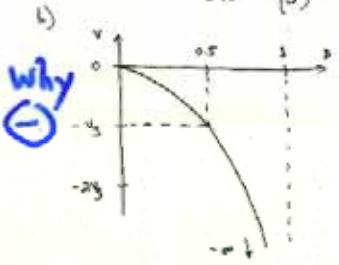
$$\approx D\left(-\frac{V}{R}\right) + D'\left(-I - \frac{V}{R}\right) = 0$$

Check $V_{IN} I_{IN} = ?$

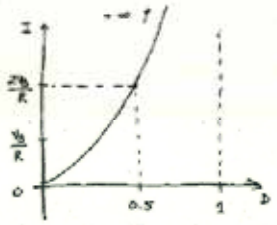
Solve for I:

$$D'I = \frac{-V}{R}\underbrace{(D+D')}_{=1}$$

$$\Rightarrow I = -\frac{V}{D'R} = \frac{D}{(D')^2}\frac{V_g}{R}$$ (inductor $i_L(DC)$)



Why (−)



$i_L(t) = ?$

$\frac{1}{2}$ → ?

$\frac{1}{4}$

c) DC design

Given $V_g = 30V$

$V = -20V$

$R = 4\Omega$

$f_s = 40kHz \Rightarrow T_s = \frac{1}{40kHz} = 25\mu sec$

(i) Find D and I

we know that $\frac{v}{v_g} = -\frac{D}{1-D}$

$\Rightarrow V(1-D) = -D V_g$

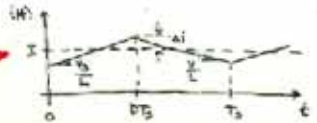
$\Rightarrow V = D(V - V_g)$

$\rightarrow D = \frac{V}{V - V_g} = \frac{-20}{-20-30} = 0.4$

equilibrium D if V_g ↓ D? baseline

$I = \frac{D}{(1-D)^2}\frac{V_g}{R} = \frac{0.4}{(0.6)^2}\frac{30V}{4\Omega} = 8.33A$

(ii) Choose L such that Δi is 10% of $I = 0.833A$



small ripple

$\frac{e\,dt}{L} = di$

$di \equiv 2\Delta i_L$

$2\Delta i = \frac{V_g}{L} D T_s \Rightarrow L = \frac{V_g D T_s}{2\Delta i}$

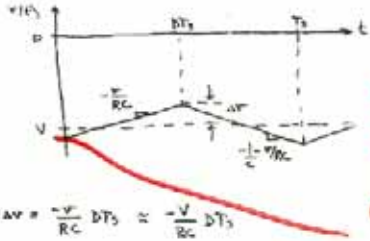
$= \frac{(30V)(0.4)(25\mu sec)}{2(0.833A)}$

$= 180\mu H$

Any problem with $|I_{DC}|$?

Could be bigger but?

(iii) Choose C such that $\Delta v = 0.1$ Volt



V_{out} ± spec

Any pbm w/ Vcl?

$$2\Delta v = \frac{-V}{RC} DT_s \simeq \frac{-V}{RC} DT_s$$

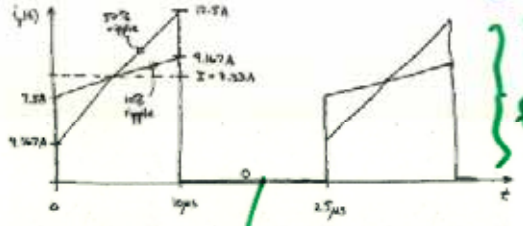
Solve for C:

$$C = \frac{-VDT_s}{2\Delta v R} = \frac{-(-20V)(0.4)(25\mu s)}{2(0.1V)(4\Omega)} = 250\mu F$$

Note: in practice, capacitor equivalent series resistance (esr) would contribute to ΔV, and would require use of a larger capacitance to achieve $\Delta v = 0.1V$.

HW Ch 3

d)



input i from V_g

$i_T = i_L$ during $0 < t < DT_s$, and $i_T = 0$ during $DT_s < t < T_s$

EMC Problem for V_g?

Why ZCTO?

Choice smaller L cheaper consequence?

Increasing a_i to 50% of T increases the peak transistor current from 9.167 A to 12.5 A.

e) Diode current $i_2(t)$

$$i_2(t) = \begin{cases} 0 & \text{during } 0 < t < DT_s \\ i_L(t) & \text{during } DT_s < t < T_s \end{cases}$$

} secondary i

Any pbm I_{peak}?

Increasing a_i also increases the peak diode current.

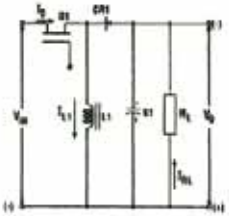
End of Problem 2.1

EMC Problem for V_{out}?

TYPE OF CONVERTER

Buck - Boost (Step Down/Up)

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = -\left(\frac{t_{on}}{T_S - t_{on}}\right) = -\left(\frac{D}{1-D}\right)$$

inverting

PEAK DRAIN CURRENT •

$$I_{DMAX} = I_{RL}\left(\frac{1}{1-D}\right) + \frac{\Delta I_{L1}}{2}$$

PEAK DRAIN VOLTAGE •

$$V_{DS} = V_{IN} + V_O + V_D$$

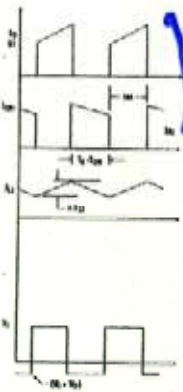
AVERAGE DIODE CURRENTS •

$$I_{CR1} = I_{RL}$$

DIODE VOLTAGES (VRM) •

$$V_{RM} = V_O + V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

Voltage inversion without using a transformer, simple, high frequency operation.

DISADVANTAGES

No isolation between input and output. Only one output is possible. Regulator loop hard to stabilize. High-side switch drive required. High output ripple. High input ripple current.

TYPICAL APPLICATIONS

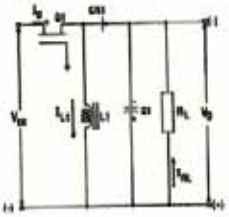
Inverse output voltages.

APPLICABLE HARRIS PRODUCTS

TYPE OF CONVERTER

Buck - Boost (Step Down/Up)

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = -\left(\frac{t_{on}}{T_S - t_{on}}\right) = -\left(\frac{D}{1-D}\right)$$

PEAK DRAIN CURRENT *

$$I_{DMAX} = I_{RL}\left(\frac{1}{1-D}\right) + \frac{\Delta I_{L1}}{2}$$

PEAK DRAIN VOLTAGE *

$$V_{DS} = V_{IN} + V_O + V_D$$

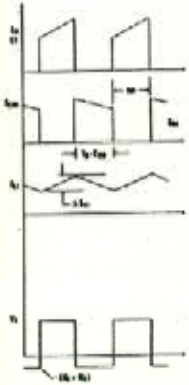
AVERAGE DIODE CURRENTS *

$$I_{CR1} = I_{RL}$$

DIODE VOLTAGES (VRM) *

$$V_{RM} = V_O + V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

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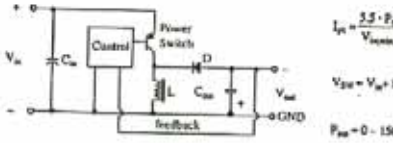
No isolation between input and output. Only one output is possible. Regulator loop hard to stabilize. High-side switch drive required. High output ripple. High input ripple current.

TYPICAL APPLICATIONS

Inverse output voltages.

APPLICABLE HARRIS PRODUCTS

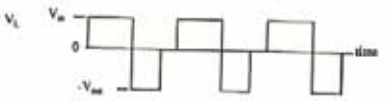
SPICE Large Δi_L ripple



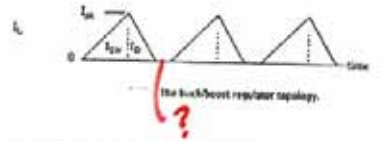
$I_{pk} = \frac{2.5 \cdot P_{out}}{V_{inmin}}$

$V_{SW} = V_{in} + |V_{out}|$

$P_{out} = 0 - 150\ W$



DCM
$i_L \to 0$



?

In preparation for your midterm exam, look at the attached schematic on pg. 8 of a flyback converter slowly - don't panic. try to find only the essential power electronics portions.

(1) identify the crude dc generation in the upper left driven by 120 ac mains. this CRUDE DC IS DRIVEN BY THE SWITCH #1 INTO THE TRANSFORMER PRIMARY.

(2) On the right side of the schematic notice the three secondaries of the transformers with the three dc outputs: 5, 12, and 30 v.

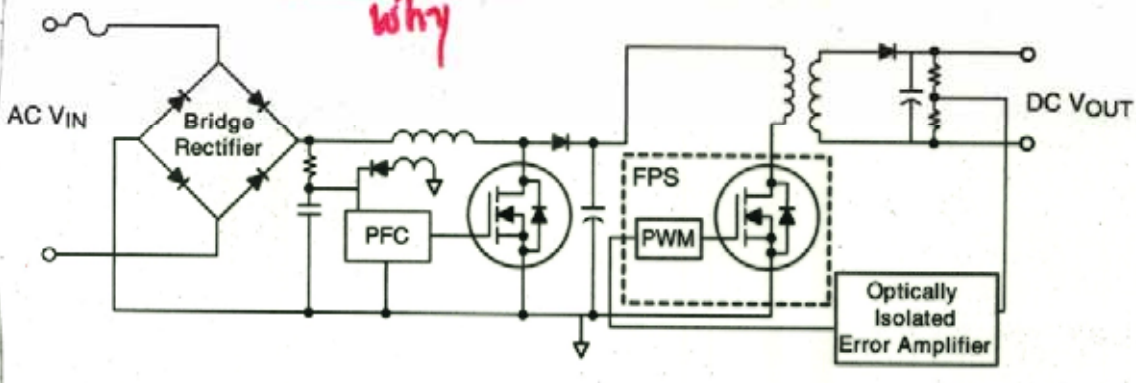
(3) Find the cmos transistor Q1 (middle) which is the switching transistor. From the gate of this cmos switch the gate control circuitry may also be found.

We will spend the rest of the semester detailing how such circuits work.

Talk #1
#2

Green FPS for quasi-resonant switching converter

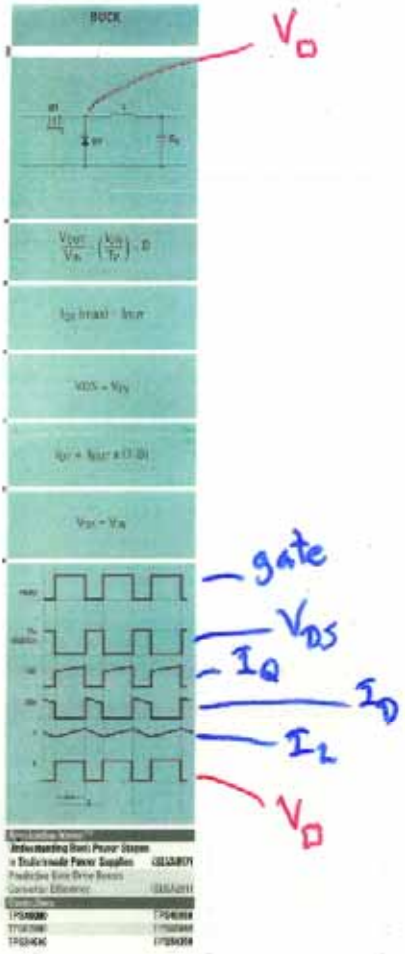
why



Only Fairchild offers complete SMPS solutions—including optically isolated error amps, PFC controllers, SuperFET™ MOSFETs, bridge rectifiers, diodes, online tools—even Global Power Resource Design Centers to accelerate your AC/DC designs.

Part V. Resonant converters

19. Resonant conversion
20. Soft switching


BUCK
V_D
gate
V_{DS}
I_Q
I_D
I_L
V_D

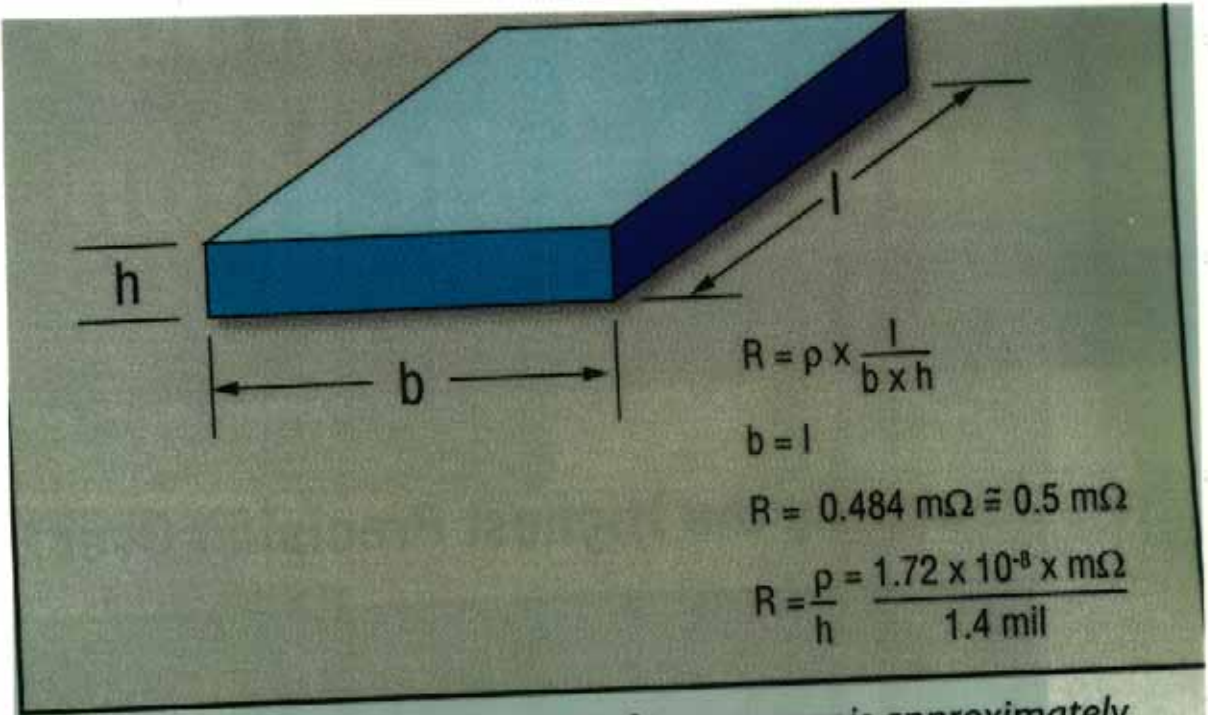
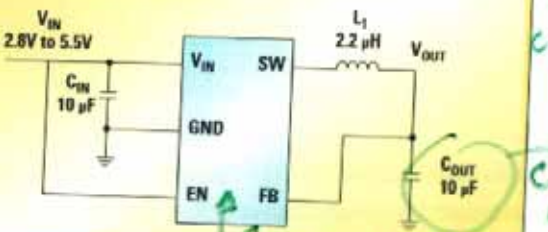


Fig. 5. *The resistance of one square of 1-oz copper is approximately 0.5 mΩ.*

LM3671 Typical application circuit

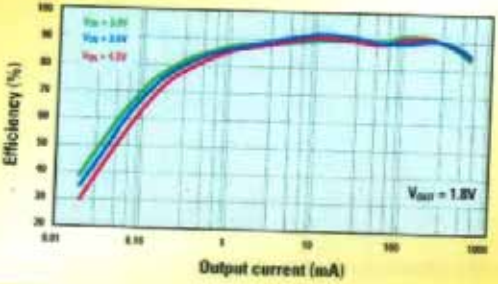


3 ex compon

high f Ceramic caps

$f_{SW} \leq 2$ MHz

LM3671 Efficiency vs. load current



Ch3

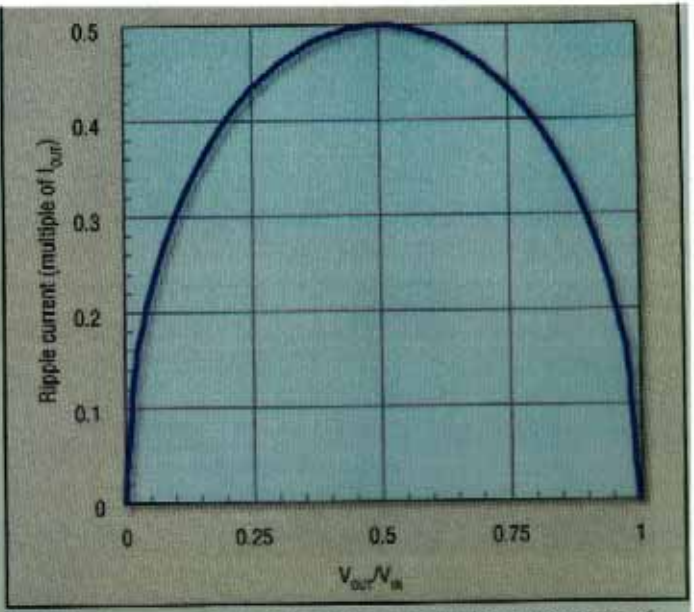
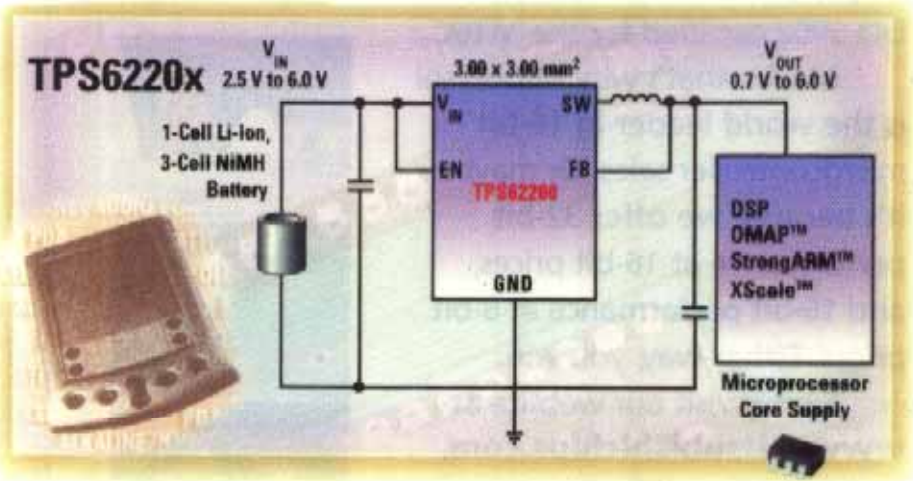


Fig. 4. *Ripple current for the input capacitors reaches a worst case of $I_{OUT}/2 = 0.5$ when the variable input voltage equals twice the fixed output voltage.*



▶ 97% efficient, 300-mA step-down converter in SOT-23

Applications

- *All 1-cell Li-Ion, 3-cell alkaline/NiMH operated products*
  - *Cell phone, PDA, pocket PC*
  - *Portable media player, digital camera*
  - *OMAP™ processor and DSP power supply*

Features

- *Efficiency: up to 97%*
- *Output current: 300 mA (max)*
- *Quiescent current: 15 µA (typ)*
- *Input voltage: 2.5 V to 6.0 V*
- *Package: 5-lead SOT-23*
- *Pricing starts at $1.50 in quantities of 1,000*

The principle of capacitor charge balance: Derivation

Capacitor defining relation:

$$i_C(t) = C \frac{dv_C(t)}{dt}$$

Integrate over one complete switching period:

$$v_C(T_s) - v_C(0) = \frac{1}{C} \int_0^{T_s} i_C(t)\, dt$$

In periodic steady state, the net change in capacitor voltage is zero:

$$0 = \frac{1}{T_s} \int_0^{T_s} i_C(t)\, dt = \langle i_C \rangle$$

Hence, the total area (or charge) under the capacitor current waveform is zero whenever the converter operates in steady state. The average capacitor current is then zero.

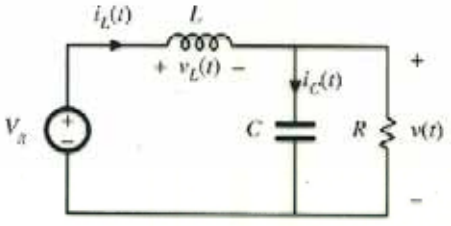
Inductor voltage and current
Subinterval 1: switch in position 1

Inductor voltage

$$v_L = V_g - v(t)$$

Small ripple approximation:

$$v_l \approx V_g - V$$



Knowing the inductor voltage, we can now find the inductor current via

$$v_l(t) = L \frac{di_l(t)}{dt}$$

Solve for the slope:

$$\frac{di_l(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L}$$

⇒ *The inductor current changes with an essentially constant slope*

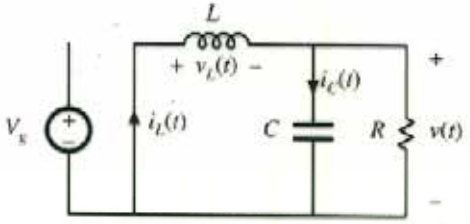
Inductor voltage and current
Subinterval 2: switch in position 2

Inductor voltage

$$v_L(t) = -v(t)$$

Small ripple approximation:

$$v_L(t) \approx -V$$



Knowing the inductor voltage, we can again find the inductor current via

$$v_L(t) = L\frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L}$$

⇒ *The inductor current changes with an essentially constant slope*

We will cover output filters in lecture 4 and pulse width control in lectures 5-7 for the three circuit topologies:buck, boost and buck- boost.

Before we venture into details we can learn a lot by a black box overview. Specifically, from the output power requirements we can work backwards to the input power required. This input power will be driven by the nominal input voltage allowing us to ascertain:

- Average input current regardless of circuit topology which has 10- 25 possibilities
- After the circuit topology is chosen we can then determine the peak currents in the input of the switch mode. These peak currents will vary by factors of 1.5 to 6 as shown below on the next page.

Diode loss dominates

In the circuit topology we have two general methods.

1. Pulsewidth modulated(PWM) converters

Employed in portable equipment or where high power flows demands the highest efficiency power conversion of about 90 %

562

2.Resonant switched converters

Utilized to achieve smaller size supplies and still avoid the electronic noise generated by PWM converters.

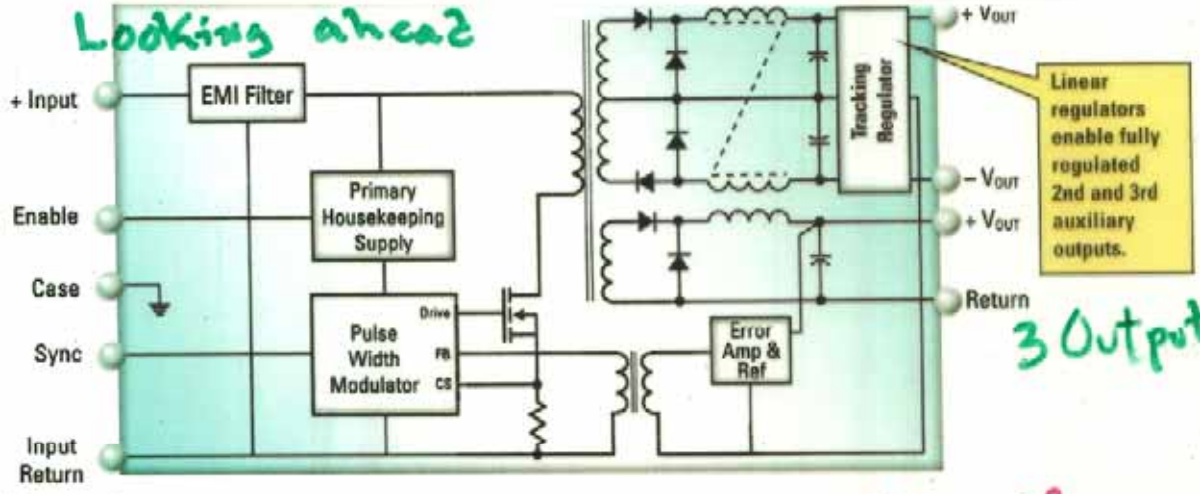
563
564

High Power no Diode loss Highest ôô loss dominates

SWITCHES Driven between cutoff and saturation lose only 1% of the transmitted power.. To better appreciate the whole of power electronics design before we begin the detailed study of each individual subtopic we show on the next page a functional block diagram including:

- Input rectifiers and RFI filters as well as output and input filters
- Power switches and Controller Chip with associated feedback
- Specialized circuits for start-up of a PWM supply
- Protection circuits for the switches and the loads
- Note the use of an isolation transformer operating at the switch frequency and not the mains frequency

Looking ahead



3 Outputs

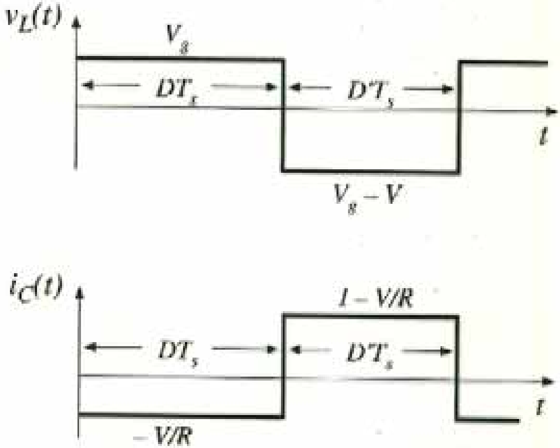
Talk #1 Chip Choices

Talk #2 Details

Vol(avl) = const   Equil Ah const

Inductor voltage and capacitor current waveforms

Fig 2.15
Pg 23



Key to V-sec balance is?

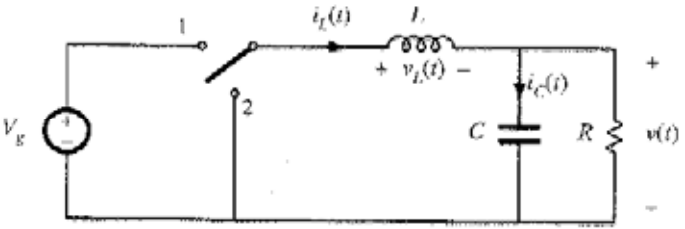
Key to i-sec balance is?

Buck $V_o = D V_g$

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

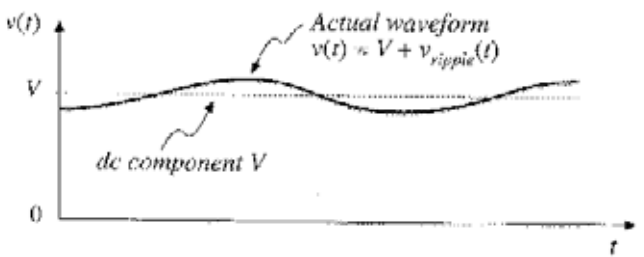
Actual output voltage waveform, buck converter

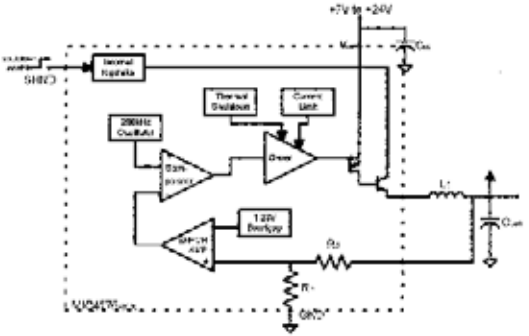
Buck converter containing practical low-pass filter



Actual output voltage waveform

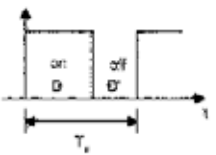
$v(t) = V + v_{ripple}(t)$





D. DUTY CYCLE CONTROL ON SWITCHING SIGNAL TO VARY V(OUT)

Although we fix f_{sw} and hence the cycle duration T_s, the on/off durations of the switch within the cycle are fully controllable form zero on time to a maximum of T_s. Variation of D will vary V(out)



assuming that only the control circuitry contains the switch we divide t_1 into 2 periods that vary in a complementary fashion

$$\tau_{on} = DT_s,\ \tau_{off} = D'T_s \text{ and } (D + D')T_s = T_s$$

That is $D + D' = 1$ when there are no dead periods.