

ECE 562

Week 1 Lecture 2

Week 1 Lecture 2

Summary

- Section 2
 - Slides 3-8 – Power conversion tasks
 - Slides 9-17 – Efficiency characteristics
 - Slides 18-40 – Buck converters and filtering
 - Slides 41-45 – Circuit elements
 - Slides 46-48 – PSpice setup
 - Slides 49-67 – Commercial power supply characteristics



1972:

Odyssey [above], the first home video game, and *Pong*, the first commercial video game, are released.

1979:
Sony debuts
the Walkman.



1981:
IBM
introduces its
first personal
computer—
the IBM PC.



1982:
The Commodore 64,
the best-selling single
personal computer
model of all time, debuts,
featuring 64-bit graphics.

CONSUMER



1971:
Intel invents
the first
microprocessor.

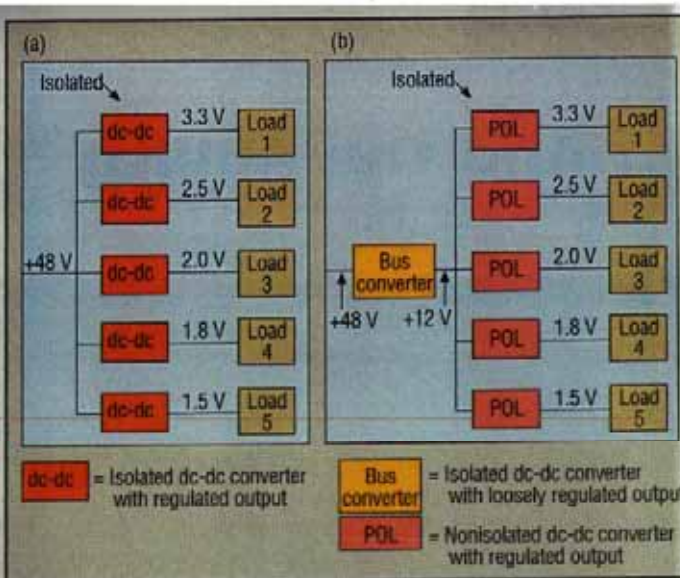
1973:
Xerox
introduces the
Alto—the first
computer with
a graphical user
interface.

1978:
Philips announces
the first CD.



1982:
Silicon Graphics
Inc. (SGI) is
launched,
sparking an era
of high-end
3-D graphics
workstations.

1988:
Deep Thought
becomes the
first computer
to beat a
human chess
master. It is
later defeated
by Garry
Kasparov.



By moving from a single-stage of on-board power conversion (a) to two-stage power conversion (b), distributed power applications have reduced system costs by paying for isolation just once. The latter approach is commonly known as the intermediate bus architecture. Voltage levels shown are merely popular values.

48V Telecom
42V ?

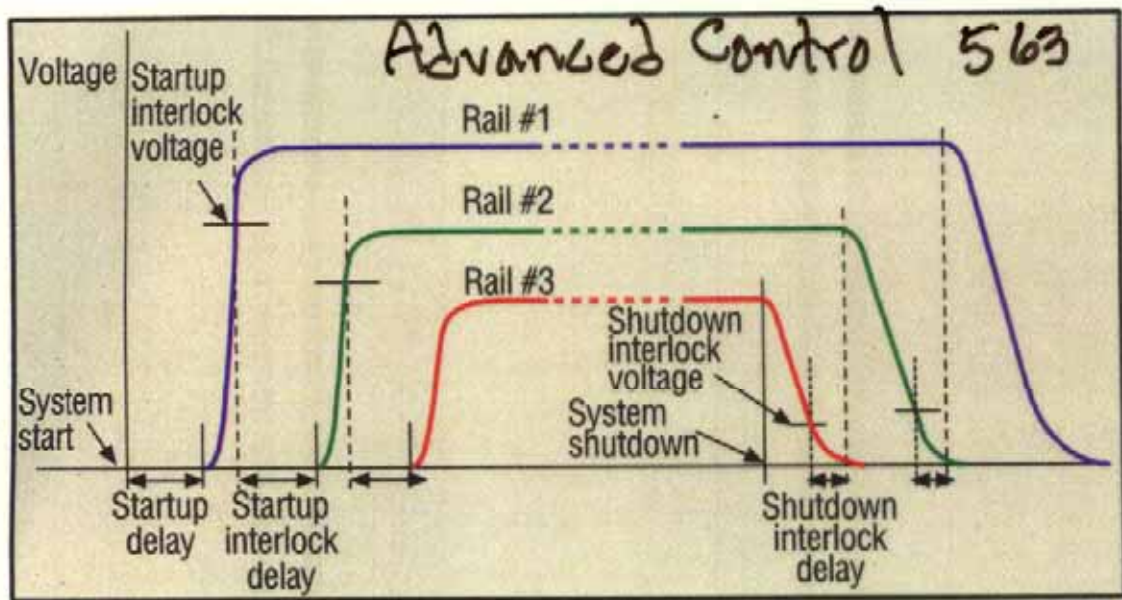


Fig. 3. Sequencing using interlocks.

Sequencing

old voltages and ti

1997:
The BlackBerry device is released by Research in Motion.



1999:
Napster brings peer-to-peer file sharing to the masses.



2001:
Apple introduces the iPod.

You Tube

2005:
YouTube is launched.

2007:
Apple releases the iPhone.

1990:
Tim Berners-Lee introduces the World Wide Web to the public on 25 December.



1997:
IEEE releases 802.11 (Wi-Fi) standard.

1998:
Google fires up its first server.

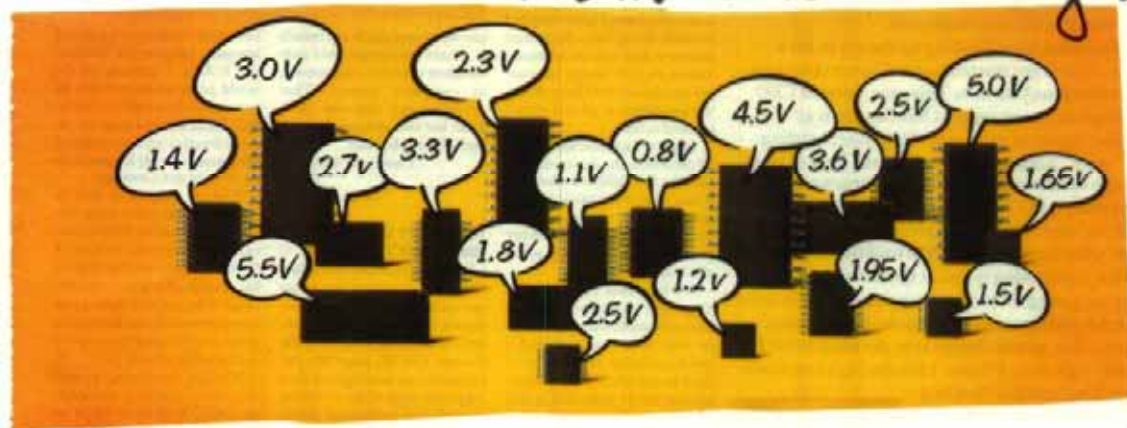


2004:
On 4 January, the NASA rover *Spirit* lands on Mars; *Opportunity* joins it on 25 January.

2005:
MareNostrum, a supercomputer with 20 terabytes of RAM, is installed in Spain.



How to get myriad of V's
from one battery?



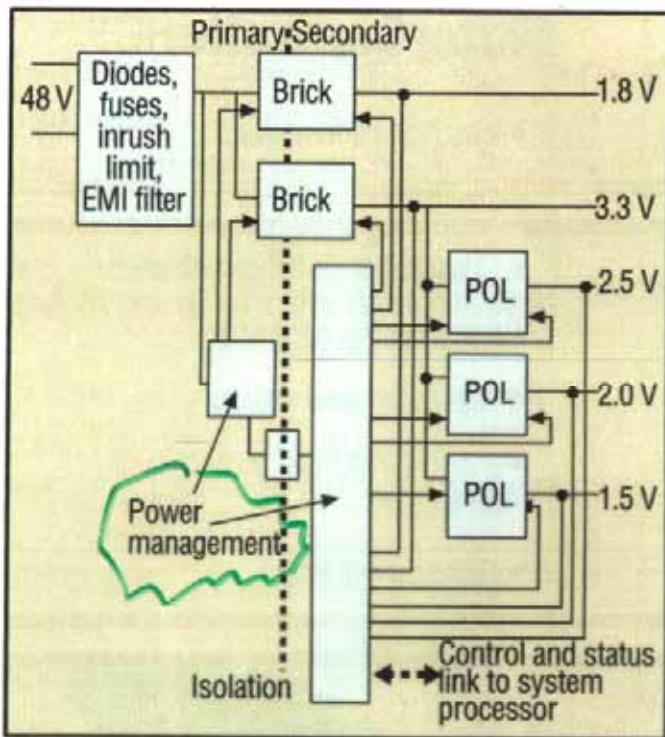
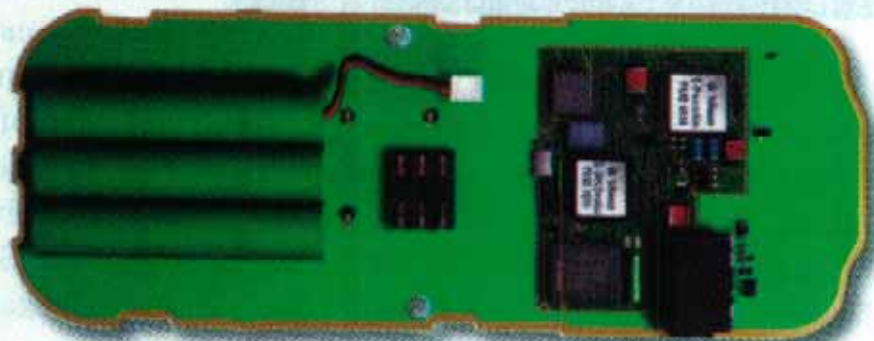
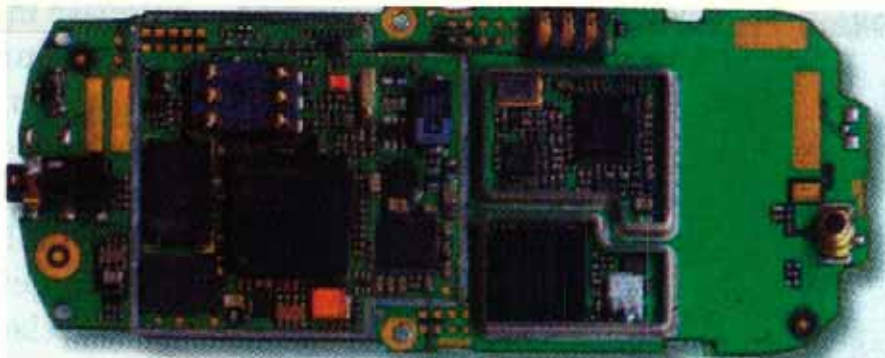


Fig. 1. 48-V card power block diagram.

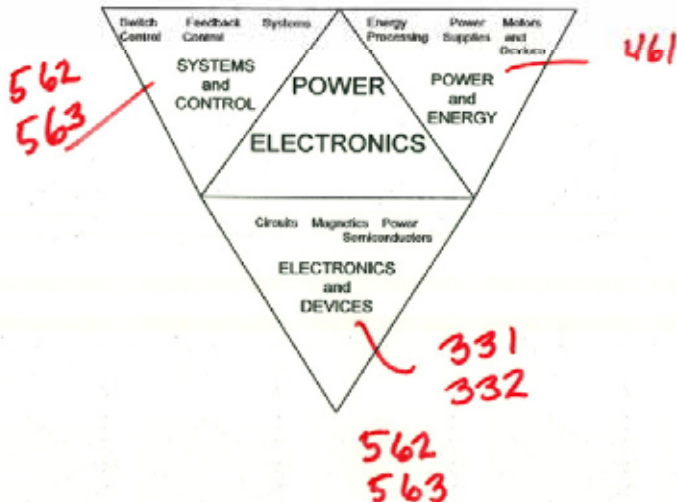


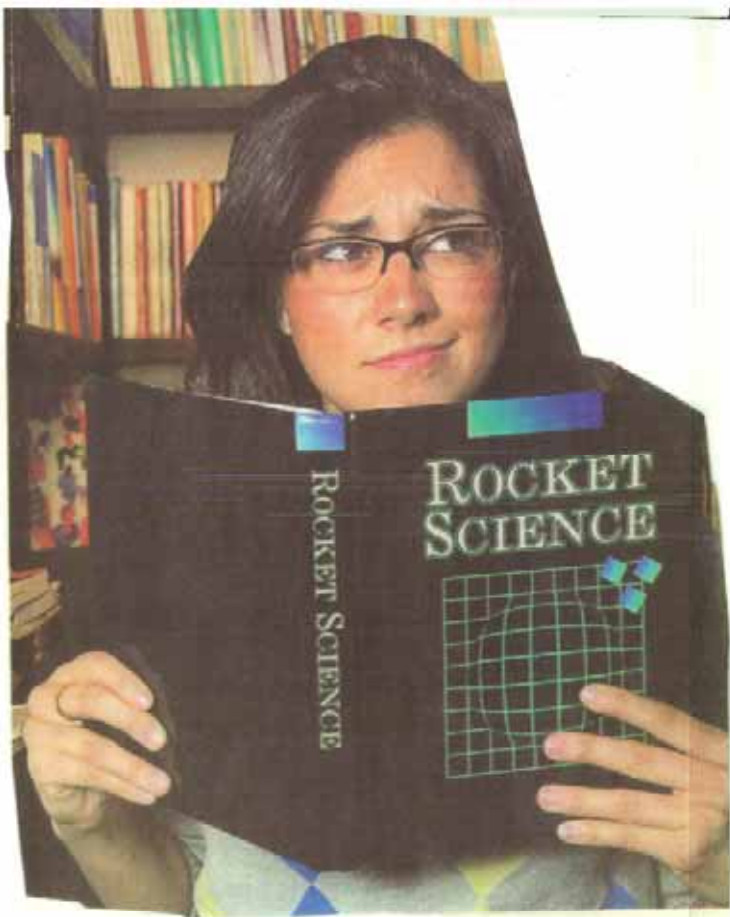
BEFORE AND AFTER: A new mobile phone prototype from Infineon [bottom] has half the number of components of a typical handset [top]. Integrating several ICs into one chip was the key.

In reality actual efficiency values are 85% to 90% due to losses in the parasitics.

The switching regulator generates very high transients of the electric and magnetic fields at 200 kHz. This generates both conducted and radiated electromagnetic noise. This noise can be easily higher than the 5% tolerance window of the supply voltage 3.1 V for the Pentium. To avoid malfunction of the processor it is necessary to filter this noise for all conditions. Moreover, this noise must not pollute the ac mains.

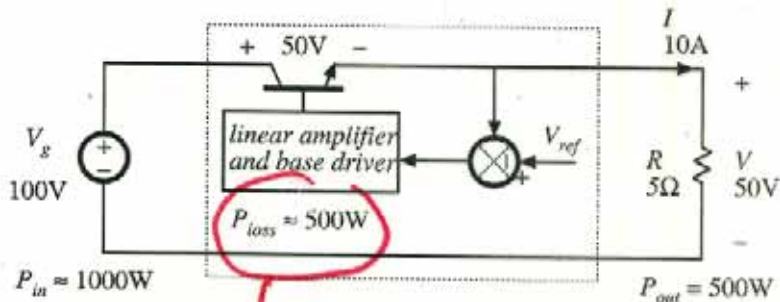
Which regulator, Example 1 or 2 is a best choice for a laptop computer?





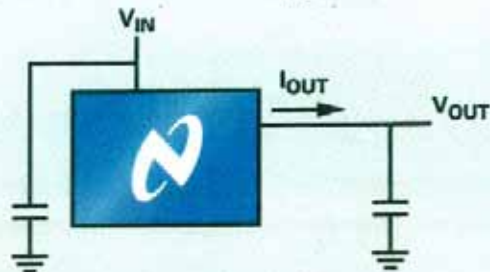
Dissipative realization

Series pass regulator: transistor operates in active region



Can we drop voltage?
w/o power loss?

old standard Linear regulator



Function: Step-down ($V_{OUT} < V_{IN}$)

When to use: Typically when $I_{OUT} < 1A$, ultra low-dropout, and low-noise applications

Characteristics: Excellent option where fixed output, low current, and low voltage drops are required. Easy to implement

Devices to use: Any low-dropout, linear regulator

Comments: Great for micropower applications

Paper #1 Topic

#2 Lab
Make a new
SPICE lab

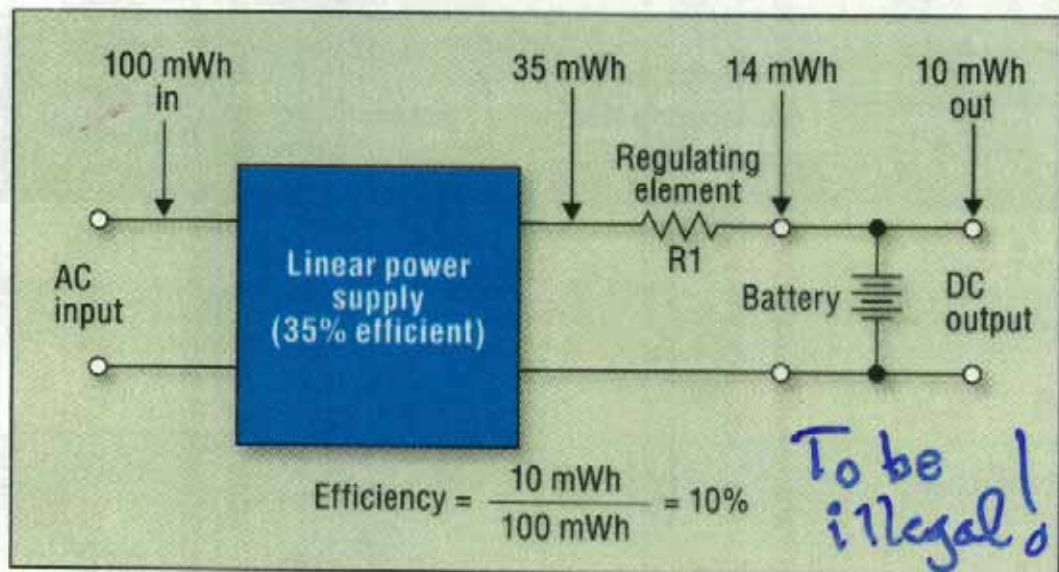


Fig. 4. In a two-piece battery charger composed of a linear power supply and a resistive linear regulator, overall efficiency is typically around 10%.

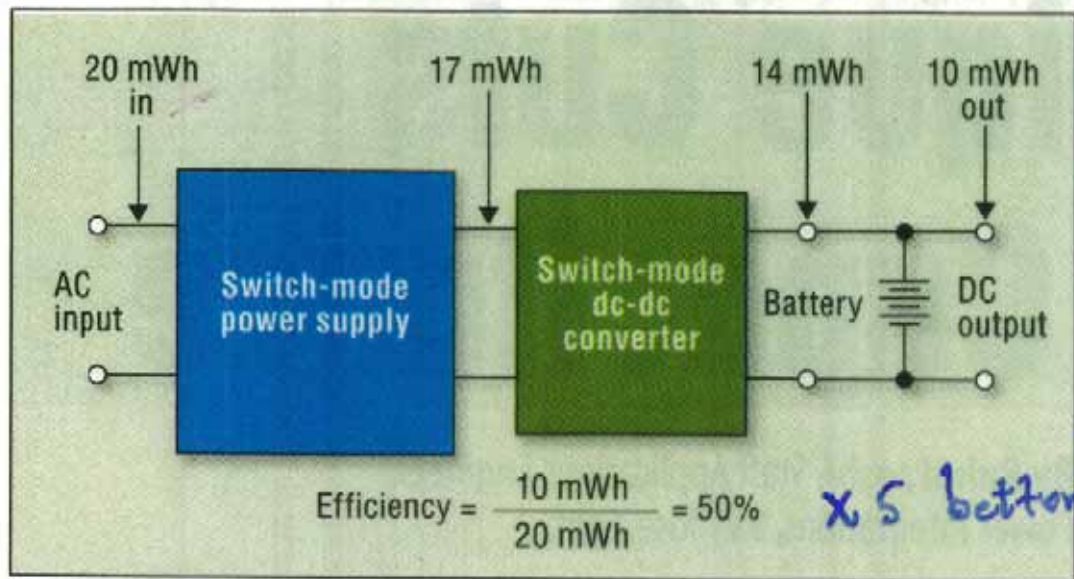
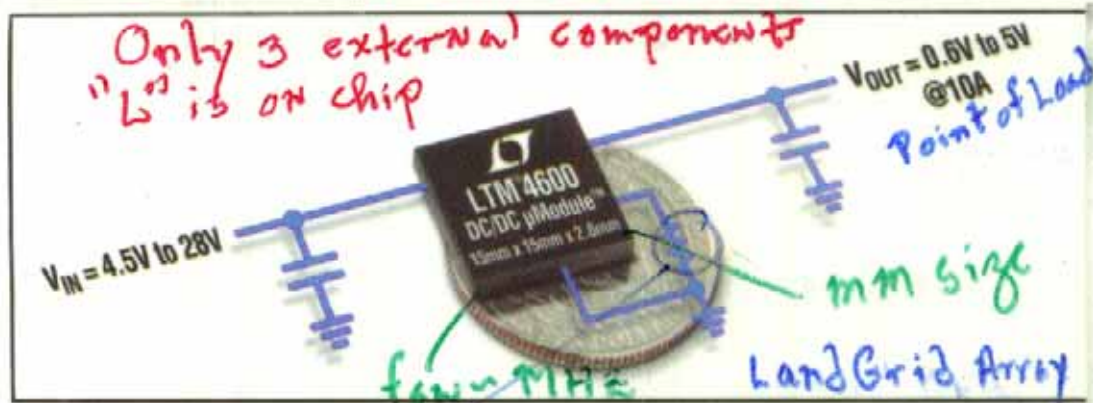


Fig. 5. A two-piece charger with two-switch mode components improves efficiency over the linear charger significantly.



Linear Technology's LTM4600 provides an instant 10-A power supply.

Power Electronics Technology | November 2005

R sets V_{out}

Two in parallel $I_{out} = ?$

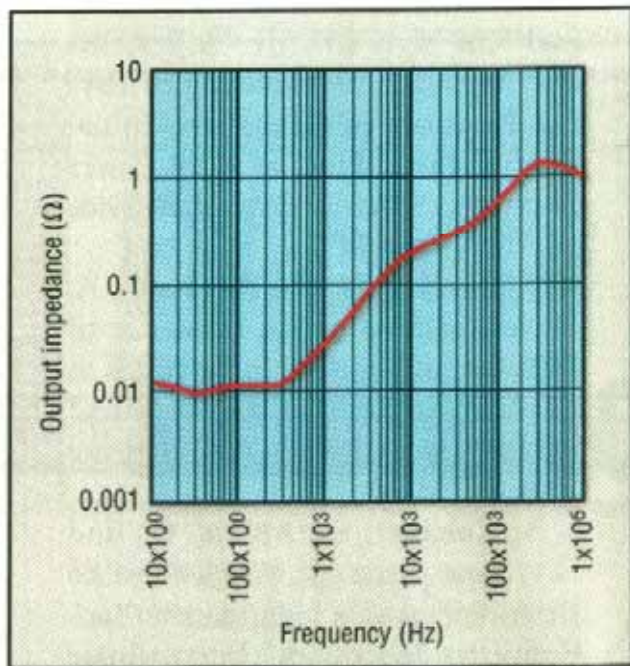
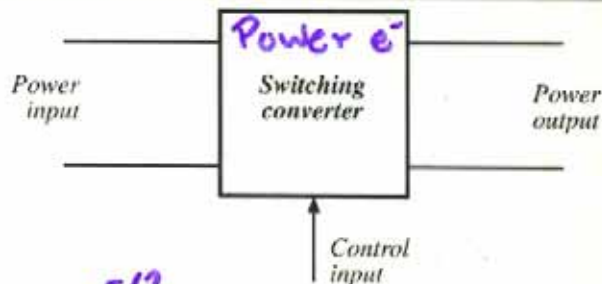
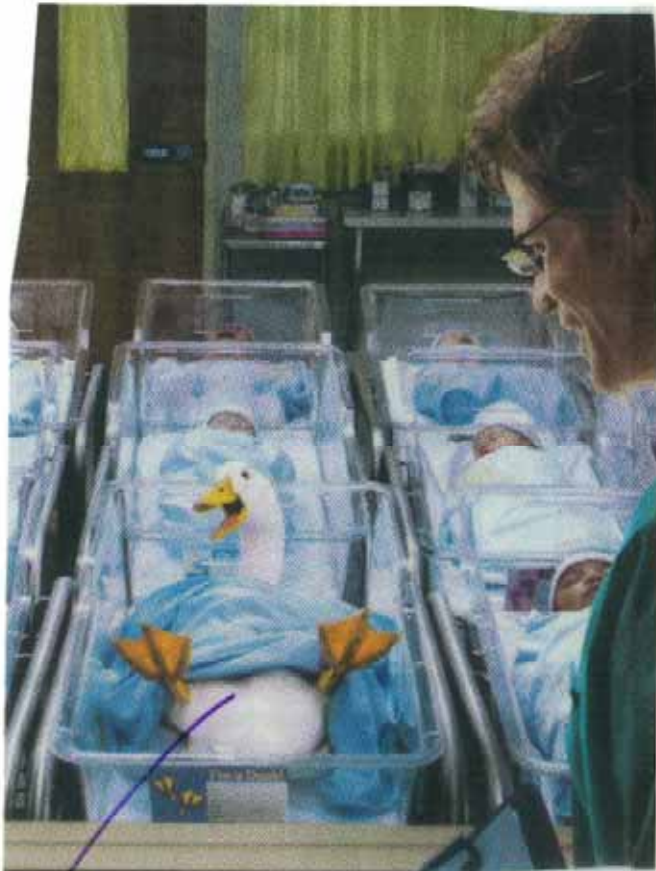


Fig.1. Output impedance characteristics of a linear regulator.

1.1 Introduction to Power Processing



- ① *Dc-dc conversion:* 562 Change and control voltage magnitude
- ② *Ac-dc rectification:* Possibly control dc voltage, ac current
- ③ *Dc-ac inversion:* 461 Produce sinusoid of controllable magnitude and frequency
- ④ *Ac-ac cycloconversion:* 461 Change and control voltage magnitude and frequency



Pe⁻ Uses L, C, switches
ALL "low loss"

Overview prior to reading text

Chapter 2

Principles of Steady-State Converter Analysis

Assume Lossless L, C, switch

- 2.1. Introduction
- 2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation
- 2.3. Boost converter example
- 2.4. Cuk converter example
- 2.5. Estimating the ripple in converters containing two-pole low-pass filters
- 2.6. Summary of key points

) Today

) read for next class

Ch 3 add L, C losses / Sw losses!

Ch2

Objectives of this chapter

- Develop techniques for easily determining output voltage of an arbitrary converter circuit
- Derive the principles of inductor volt-second balance and capacitor charge (amp-second) balance
- Introduce the key small ripple approximation
- Develop simple methods for selecting filter element values
- Illustrate via examples

Choose L_{opt}

Choose C_{opt}

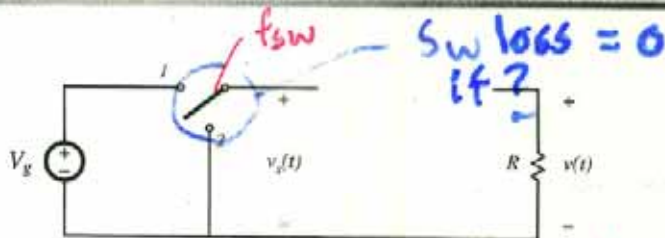
$$\frac{e}{L} = \frac{di}{dt} \Rightarrow \int \frac{e}{L} dt \rightarrow i \quad \begin{matrix} \text{same} \\ @ t=0 \\ @ t=T_{sw} \end{matrix}$$

Balance \Rightarrow no i drift

2.1 Introduction Buck converter

Fig 2.1
pg 13

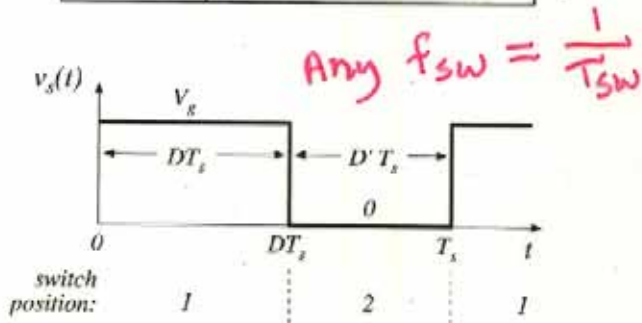
SPDT switch changes dc component



Switch output voltage waveform

Duty cycle D :
 $0 \leq D \leq 1$

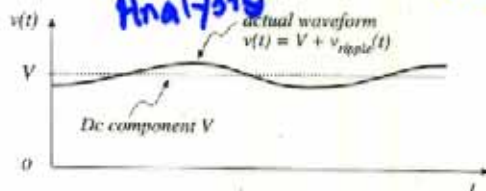
complement D' :
 $D' = 1 - D$



The small ripple approximation

Avoids ① Spice Transient Analysis ② Complex Analysis

$$v(t) = V + v_{\text{ripple}}(t)$$



In a well-designed converter, the output voltage ripple is small. Hence, the waveforms can be easily determined by ignoring the ripple:

$$|v_{\text{ripple}}| \ll V$$

$$v(t) = V$$

Dc component of switch output voltage

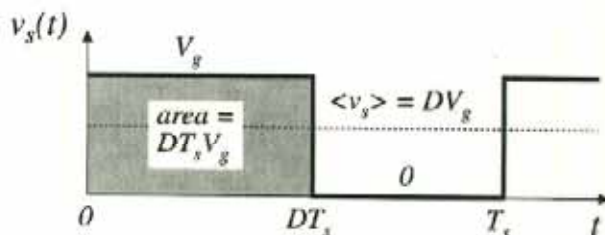


Fig 2.2
pg 124

Fourier analysis: Dc component = average value

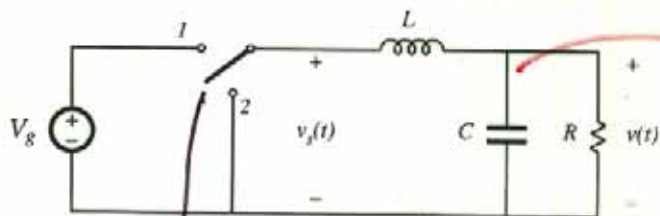
$$\langle v_s \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt$$

$$\langle v_s \rangle = \frac{1}{T_s} (DT_s V_g) = DV_g$$

Very choppy DC
without filter

Insertion of low-pass filter to remove switching harmonics and pass only dc component

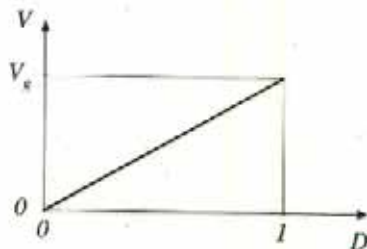
f_{sw}
noise
ripple



$\tau = \frac{L}{R}$

$\tau = RC$

$v = \langle v_L \rangle = DV_g$
 f_{sw}
 T_{sw}



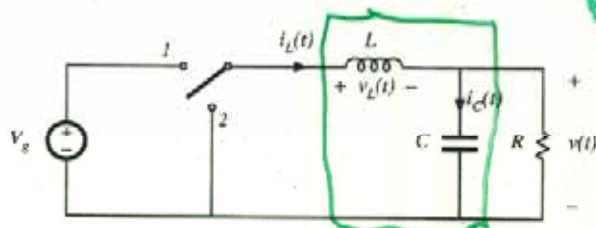
For filtering

$T_{sw} \ll \tau_{RC}$ or τ_{LC}

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

Actual output voltage waveform, buck converter

Buck converter containing practical low-pass filter



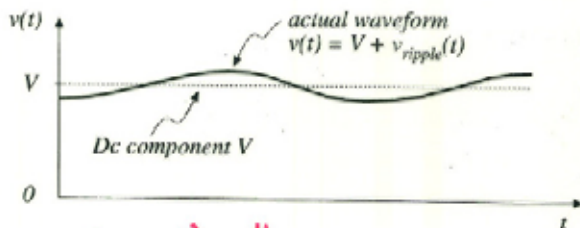
Both L & C are "big"

Actual output voltage waveform

$$v(t) = V + v_{\text{ripple}}(t)$$



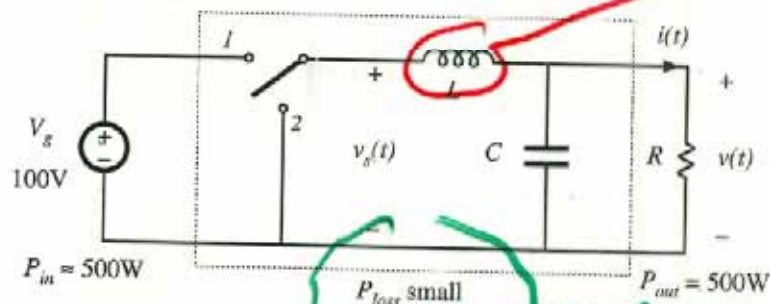
How to drive to "0"



Addition of low pass filter

Roll-off

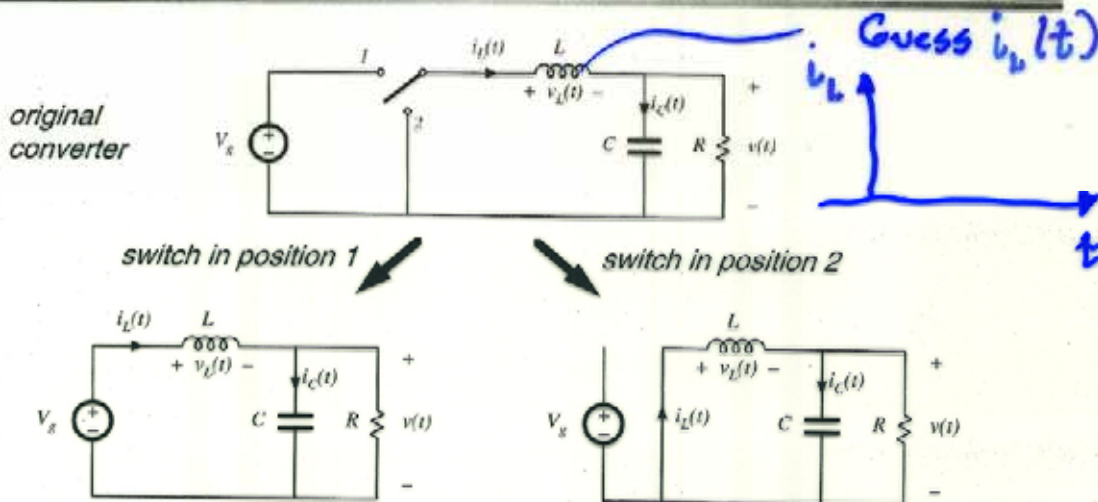
Addition of (ideally lossless) L-C low-pass filter, for removal of switching harmonics



- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s
- This circuit is known as the "buck converter"

Buck converter analysis: inductor current waveform

Fig 2.8
P17



Inductor voltage and current

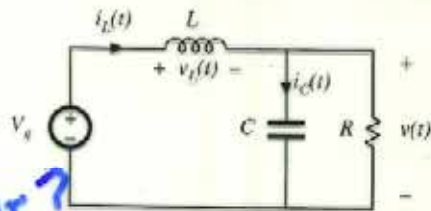
Subinterval 1: switch in position 1

Inductor voltage

$$v_L = V_g - v(t)$$

Small ripple approximation:

$$v_L \approx V_g - V \approx \text{constant over?}$$



Knowing the inductor voltage, we can now find the inductor current via

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L}$$

⇒ The inductor current changes with an essentially constant slope



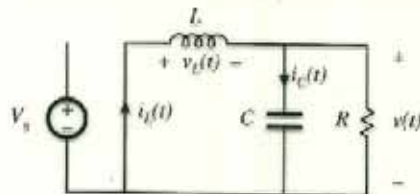
Inductor voltage and current Subinterval 2: switch in position 2

Inductor voltage

$$v_L(t) = -v(t)$$

Small ripple approximation:

$$v_L(t) = -V \text{ Constant}$$



Knowing the inductor voltage, we can again find the inductor current via

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} = -\frac{V}{L}$$

→ *The inductor current changes with an essentially constant slope*



Assumes $T_{sw} \ll RC, \frac{L}{R}$

Inductor voltage and current waveforms

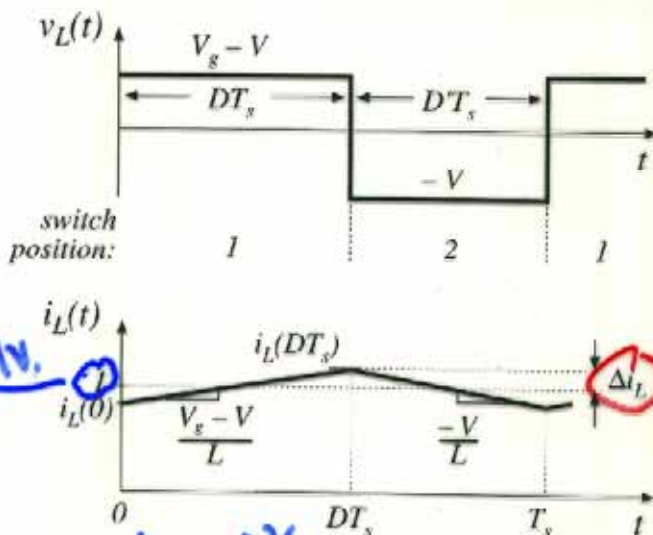


Fig 2.9
2.10
p. 18

$$v_L(t) = L \frac{di_L(t)}{dt}$$

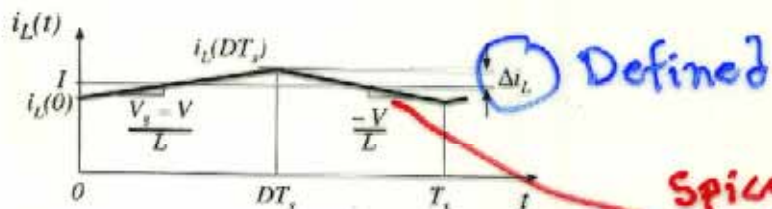
Goal is Big Av. current

Small goal

$$\Delta i = \frac{\Delta V}{L} \Delta t$$

Δi small \Rightarrow ?

Determination of inductor current ripple magnitude



(change in i_L) = (slope)(length of subinterval)

$$(2\Delta i_L) = \left(\frac{V_s - V}{L}\right)(DT_s)$$

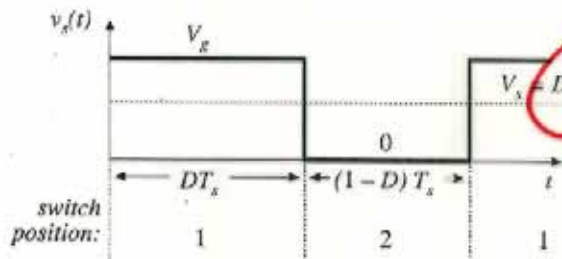
$$\Rightarrow \Delta i_L = \frac{V_s - V}{2L} DT_s$$

$$L = \frac{V_s - V}{2\Delta i_L} DT_s$$

t_{on} SW1

Spice
Simulation
DUE
Set Δi
ripple by?

The switch changes the dc voltage level



$D =$ switch duty cycle
 $0 \leq D \leq 1$

$T_s =$ switching period

$f_s =$ switching frequency
 $= 1 / T_s$

DC component of $v_s(t) =$ average value:

$$V_s = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = DV_g$$

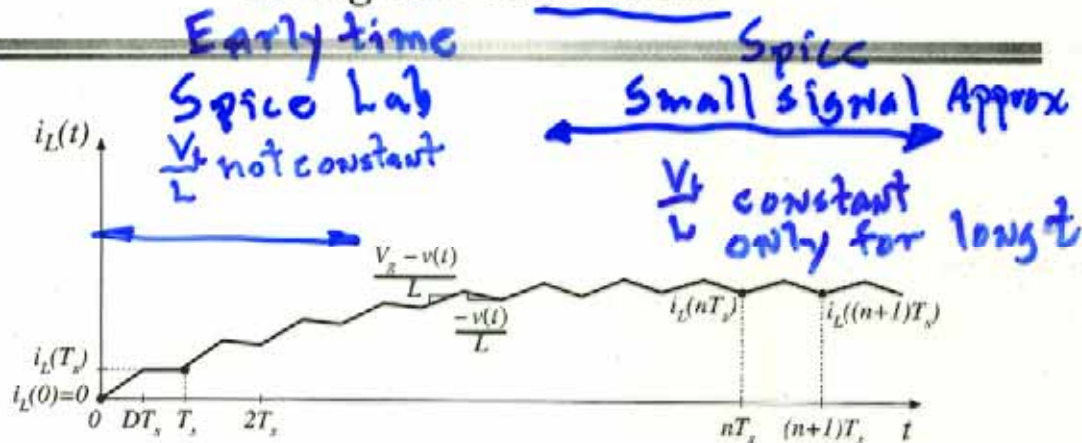
$\neq f(t_{SW})$ why

$f_s \uparrow$ good why?

Σ effects
 Σ

Trt effects
 Trend?

Inductor current waveform during turn-on transient

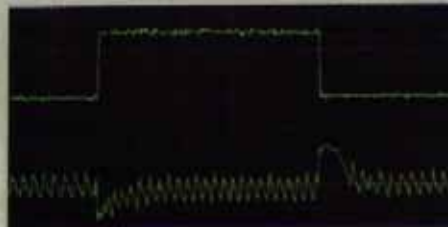


When the converter operates in equilibrium:

$$i_L((n+1)T_s) = i_L(nT_s)$$

563

Fast Transient Response



I_{OUT}
10A/DIV

V_{OUT}
100mV/DIV

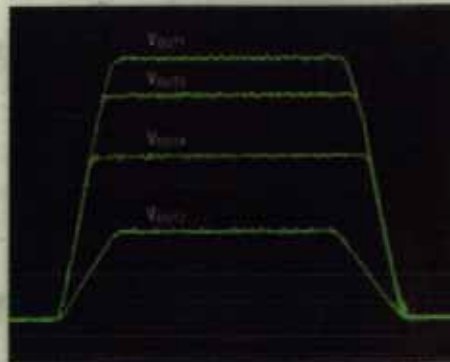
$V_{IN} = 15V$

20 μ s/DIV

$V_{OUT} = 2.5V$

$C_{OUT} = 2 \times 330\mu F$

Coincident or Ratiometric Tracking

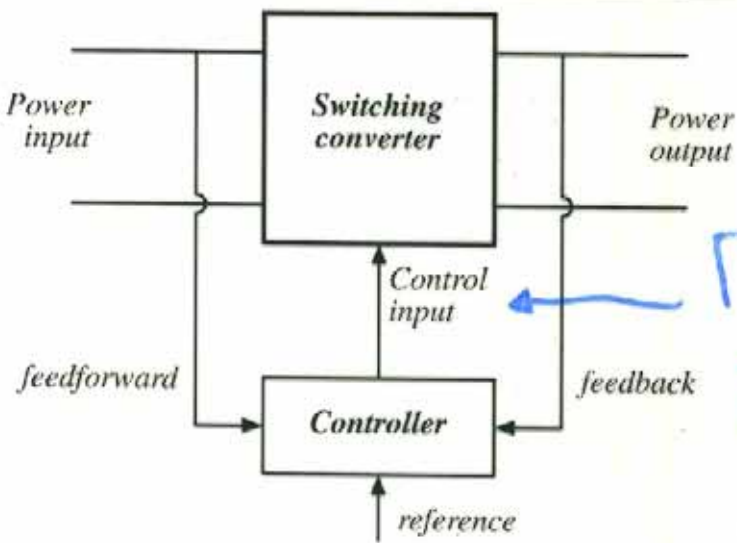


2ms/DIV


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V_{out} } Const
 V_{in} } Const
during T_{sw}

Control is invariably required



ON duty cycle "D"



The principle of inductor volt-second balance: Derivation

Inductor defining relation:

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Integrate over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L} \int_0^{T_s} v_L(t) dt$$

In periodic steady state, the net change in inductor current is zero:

$$0 = \int_0^{T_s} v_L(t) dt$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state.

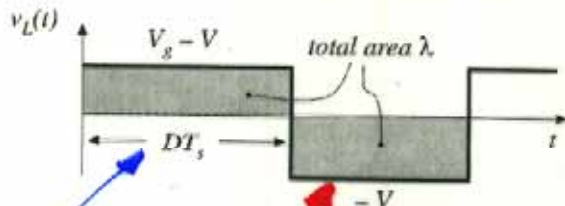
An equivalent form:

$$0 = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = \langle v_L \rangle$$

The average inductor voltage is zero in steady state.

Inductor volt-second balance: Buck converter example

Inductor voltage waveform,
previously derived:



Integral of voltage waveform is area of rectangles:

$$\lambda = \int_0^{T_s} v_L(t) dt = (V_g - V)(DT_s) + (-V)(D'T_s)$$

Average voltage is **SW1 ON** **SW2 ON**

$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V)$$

Equate to zero and solve for V :

$$0 = DV_g - (D + D')V = DV_g - V \quad \Rightarrow \quad V = DV_g$$

The principle of capacitor charge balance: Derivation

Capacitor defining relation:

$$i_c(t) = C \frac{dv_c(t)}{dt}$$

Integrate over one complete switching period:

$$v_c(T_s) - v_c(0) = \frac{1}{C} \int_0^{T_s} i_c(t) dt$$

In periodic steady state, the net change in capacitor voltage is zero:

$$0 = \frac{1}{T_s} \int_0^{T_s} i_c(t) dt = \langle i_c \rangle$$

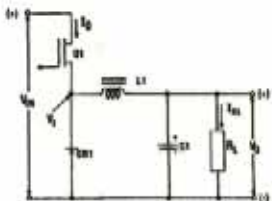
Hence, the total area (or charge) under the capacitor current waveform is zero whenever the converter operates in steady state. The average capacitor current is then zero.



TYPE OF CONVERTER

Buck (Step Down)

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = \frac{t_{on}}{T_S} = D$$

PEAK DRAIN CURRENT

$$I_{D\text{MAX}} = I_{RL} + \frac{\Delta I_L}{2}$$

CAN make
→ 0

PEAK DRAIN VOLTAGE

$$V_{D1} = V_{IN} + V_D$$

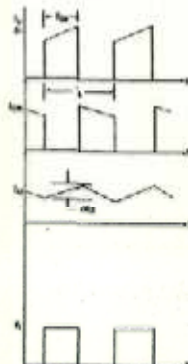
AVERAGE DIODE CURRENTS

$$I_{CR1} = I_{RL} (1-D)$$

DIODE VOLTAGES (VRM)

$$V_{1M} = V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

High efficiency, simple, no transformer, low switch stress. Small output filter, low ripple.

DISADVANTAGES

No isolation between input and output. Potential over-voltage if D1 shorts. Only one output possible. High-side switch (fsw) required. High input ripple current.

TYPICAL APPLICATIONS

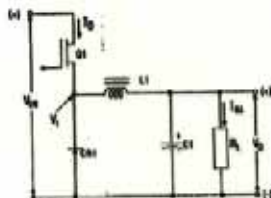
Small size, imbedded systems.

APPLICABLE HARRIS PRODUCTS

HP2660 w/P IGBT For all the CKTS.

TYPE OF CONVERTER

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = \frac{t_{ON}}{T_S} = D$$

PEAK DRAIN CURRENT

$$I_{D\text{MAX}} = I_{RL} + \frac{\Delta I_L}{2}$$

PEAK DRAIN VOLTAGE

$$V_{D1} = V_{IN} + V_D$$

AVERAGE DIODE CURRENTS

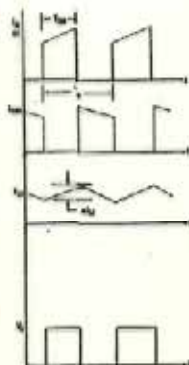
$$I_{CR1} = I_{RL} (1-D)$$

DIODE VOLTAGES (VRM)

$$V_{RM} = V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS

Pspice
Simulation
Lab #1



ADVANTAGES

High efficiency, simple, no transformer, low switch stress. Small output filter, low ripple.

DISADVANTAGES

No isolation between input and output. Potential over-voltage if Q1 fails. Only one output possible. High-side switch drive required. High input ripple current.

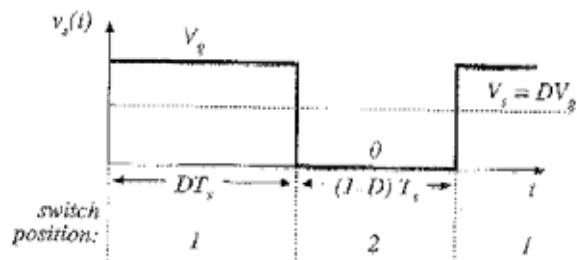
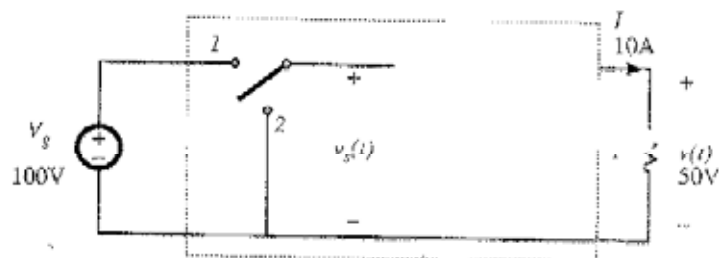
TYPICAL APPLICATIONS

Small size, inhealed systems.

APPLICABLE HARRIS PRODUCTS

HP1500 uP-IGBT For off line CKTS.

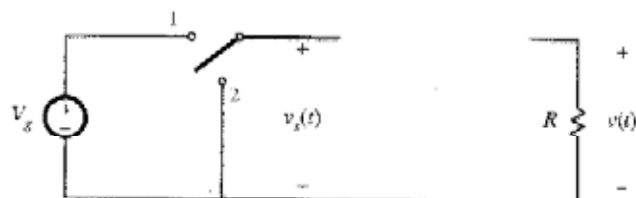
Use of a SPDT switch



2.1 Introduction

Buck converter

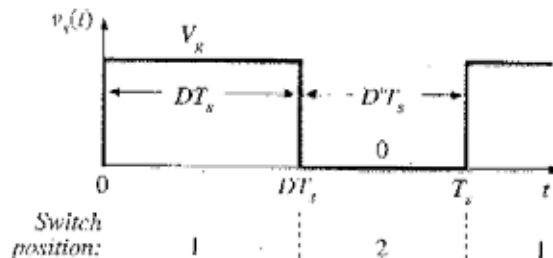
SPDT switch changes dc component



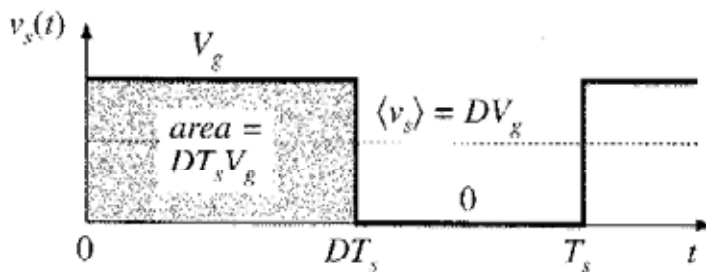
Switch output voltage waveform

Duty cycle D :
 $0 \leq D \leq 1$

complement D' :
 $D' = 1 - D$



Dc component of switch output voltage



Fourier analysis: Dc component = average value

$$\langle v_s \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt$$

$$\langle v_s \rangle = \frac{1}{T_s} (DT_s V_g) = DV_g$$

How to Set up Pspice at CSU

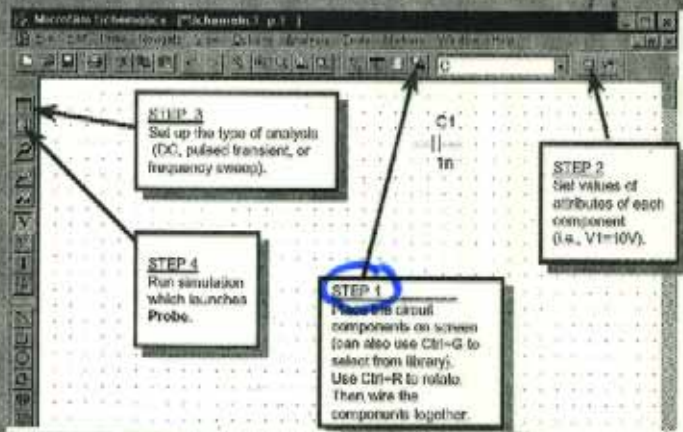
- Using Window NT explorer
 - s: Application Pspice SV_91 CSU_setup Pspice
 - T drive -> Classes -> EE562 -> Pspice folder (Pspice SV and Pspice(LV).lnb)



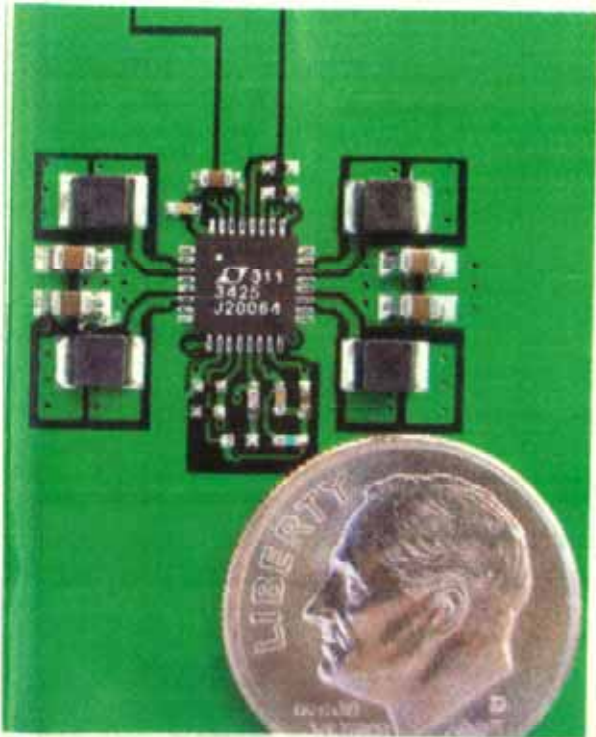
Copy the Pspice folder and its sub files into your D drive, using right mouse button to drag and drop.

Steps of create a circuit

- ❖ Open the schematic
 - To start, double click on the Pspice SV icon
 - And Pspice schematic will open
 - Use it to create your circuit diagram (a process called schematic capture)
- ❖ Major steps



... process are spay



Demonstration board LTC3425

$V_{IN} = 3.3\text{ V}, 5\text{ V}, \text{ or } 12\text{ V}$

15 A



Track

$V_{O1} = 3.3\text{ V}$

20 A



Track

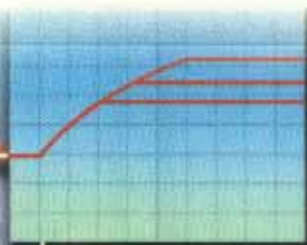
$V_{O2} = 2.5\text{ V}$

30 A



Track

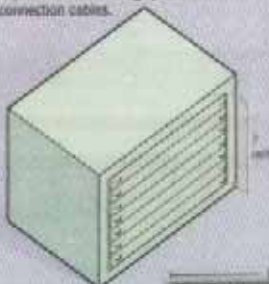
$V_{O3} = 1.8\text{ V}$



$\frac{100 \text{ A}}{\text{Processor}} * 10^2 \text{ processors}$
 $\Rightarrow ? \text{ KA}$

Making the Most of Server Real Estate

Traditional rack servers stack computers horizontally in standard racks. Each machine requires its own cooling system and connection cables.

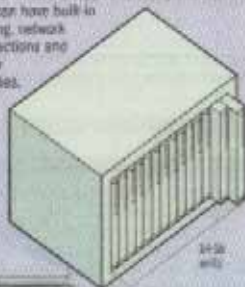


Rack view of a rack

The extra components are redundant and make for a complicated set-up of wires in the back.

Source: IBM, 1997

Blade servers save space by leaving only computing essentials on each machine. The smaller units are slipped vertically into racks that can have built-in cooling, network connections and power supplies.



More machines fit in the same space and individual units are easy to plug in, due to the stacking structure in the back.

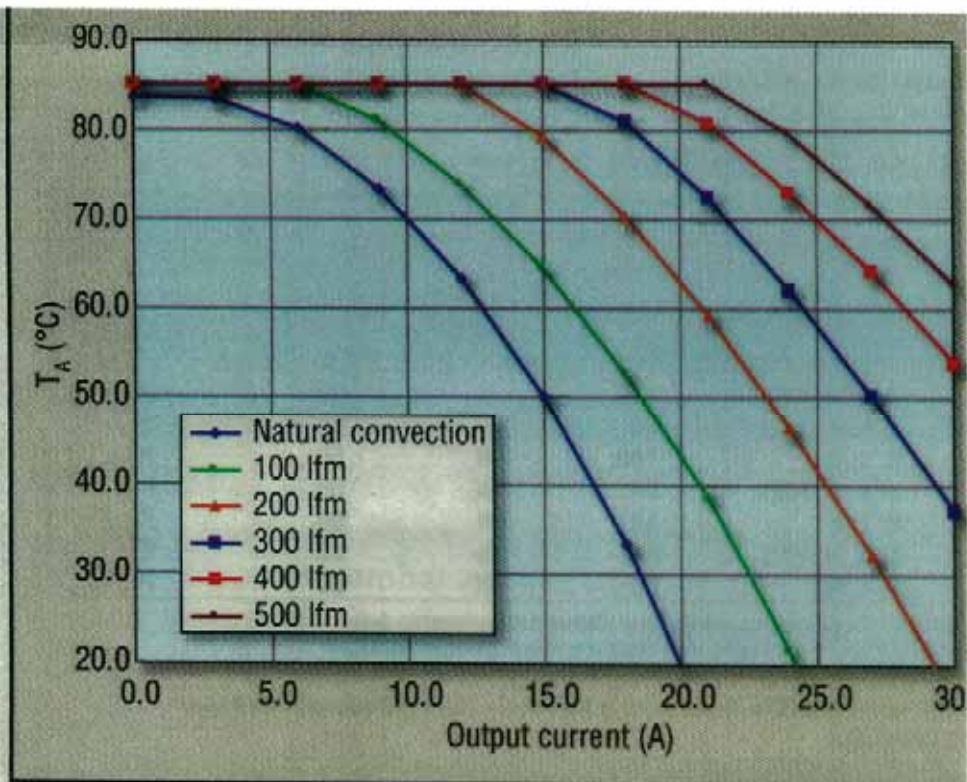
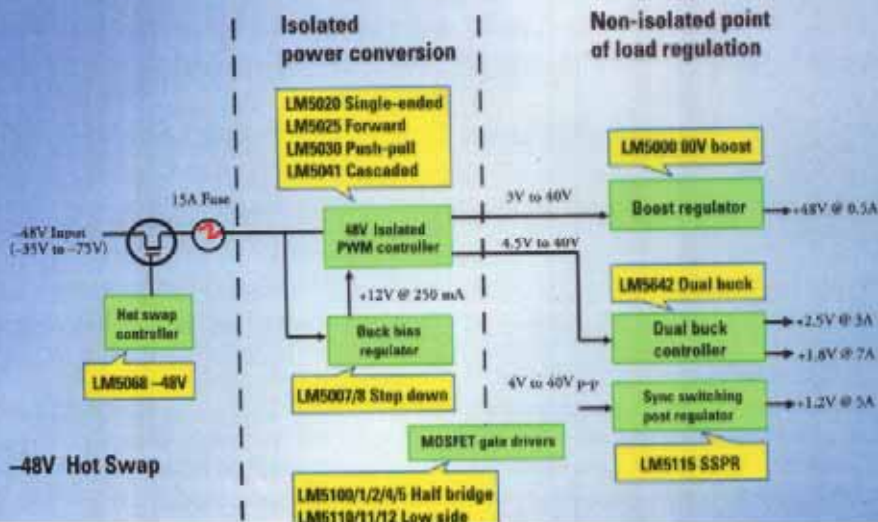


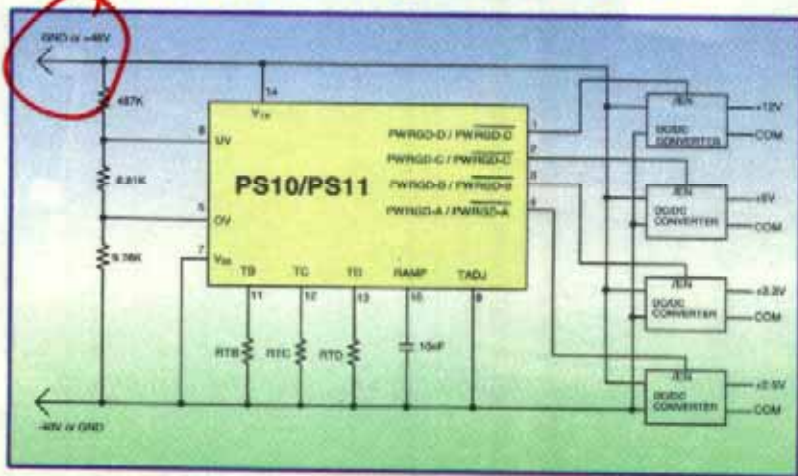
Fig. 1. Thermal-derating curves specify the maximum current a dc-dc converter can deliver at different airflow speeds and ambient temperatures.

LM5000 family, the complete solution for distributed power architectures



Tel Com Why?

PS10/PS11 Quad Power Sequencing Controller



- ✓ Turns on up to 4 DC-DC converters sequentially
- ✓ Eliminates the need for optocouplers
- ✓ Timing can be programmed using external resistors
- ✓ Programmable UV and OV

asserting a fault condition.

running, without interrupting the

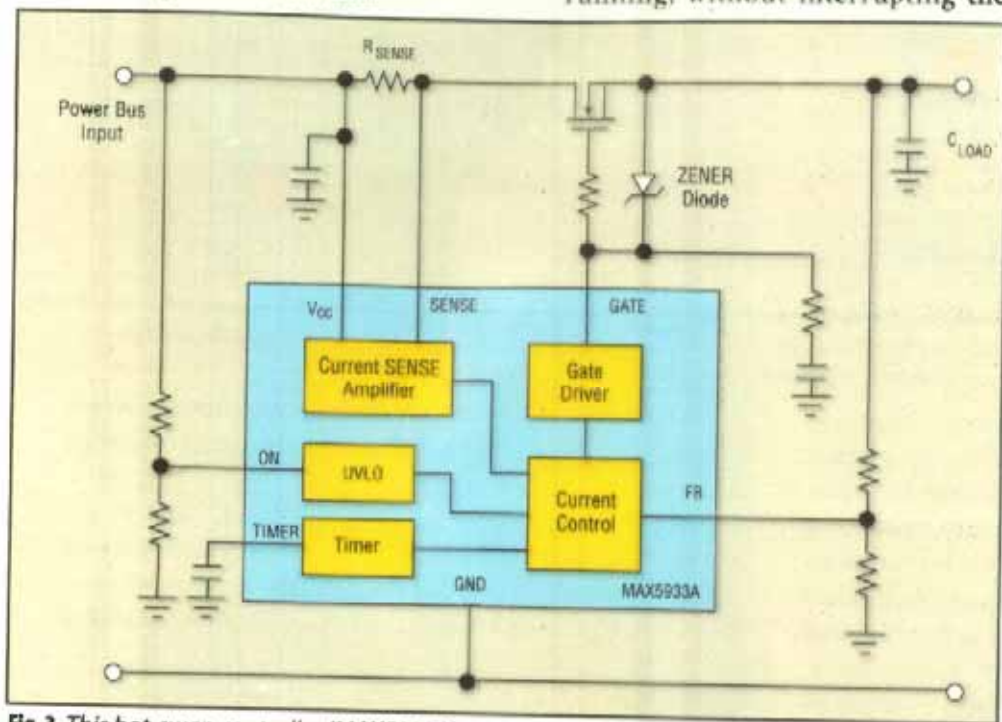
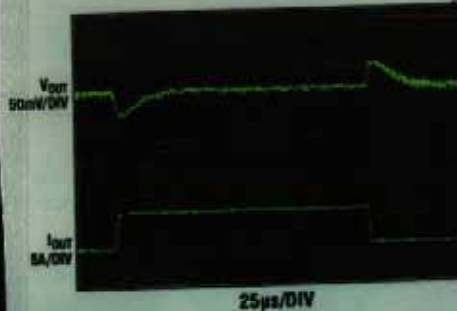


Fig. 3. This hot-swap controller (MAX933A) protects the power bus against inrush current spikes and short-circuit faults.

▼ Features

- 15mm x 15mm x 2.8mm LGA with $15^{\circ}\text{C}/\text{W } \theta_{JA}$
- Pb-Free (e^4), RoHS Compliant
- Only C_{BULK} Required
- Standard and High Voltage:
LTM4600EV: $4.5\text{V} \leq V_{IN} \leq 20\text{V}$
LTM4600HVEV: $4.5\text{V} \leq V_{IN} \leq 28\text{V}$
- $0.6\text{V} \leq V_{OUT} \leq 5\text{V}$
- I_{OUT} : 10A DC, 14A Peak
- Parallel Two μ Modules for 20A Output

Ultrafast Transient Response $2\% \Delta V_{OUT}$ with a 5A Step

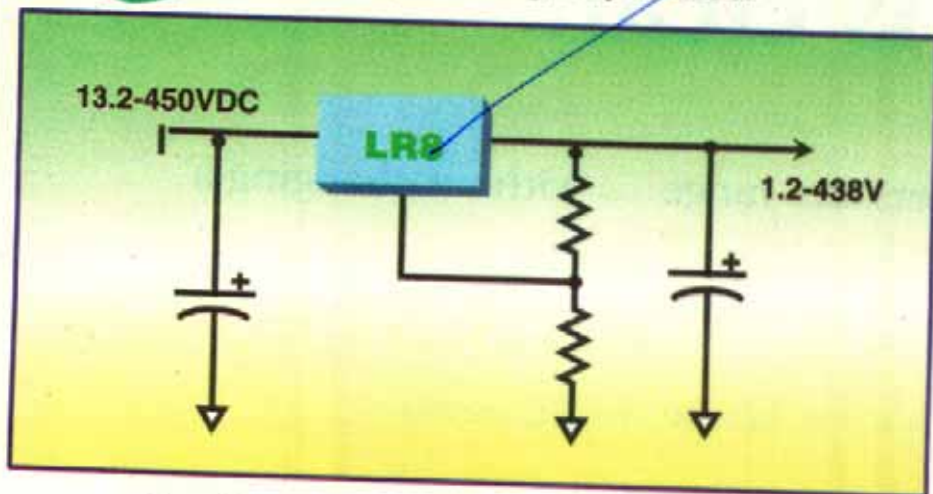


$V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$, 0A to 5A Load Step
($C_{BULK} = 3 \times 22\mu\text{F CERAMICS}$, 470 $\mu\text{F POS CAP}$)

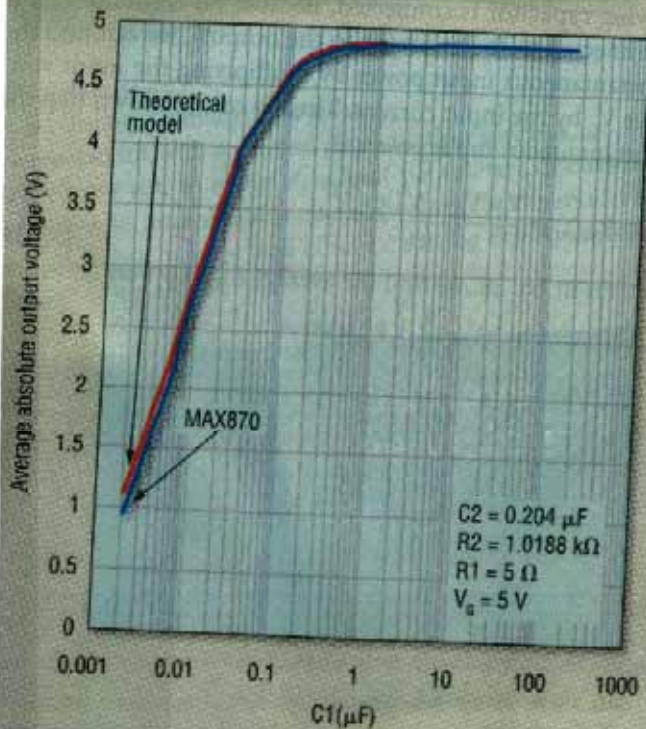
LR8: HV Adjustable Linear Regulator

The LR8 is a 3-terminal adjustable linear regulator just like an LM317 capable of input voltages up to 450V.

V_{LR8} & η



The LR8 can be used as a stand-alone linear regulator or as a PWM start-up circuit



5. Values of average output voltage versus flying capacitance (C_1) calculated using the theoretical model are close to the actual results obtained with the MAX870.

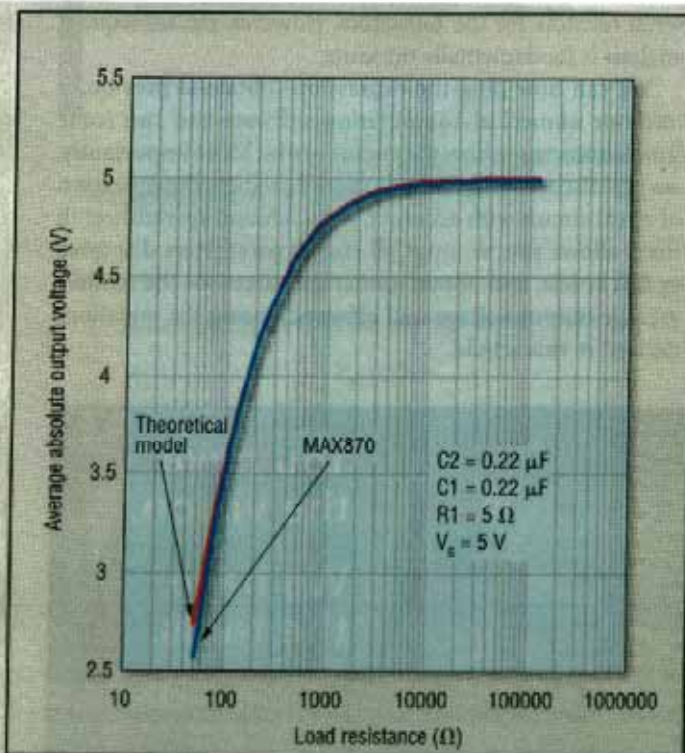


Fig. 4. A plot of the average output voltage versus load resistance ($R2$) for the theoretical model agrees closely with the actual results obtained with a switched-capacitor voltage inverter (MAX870).

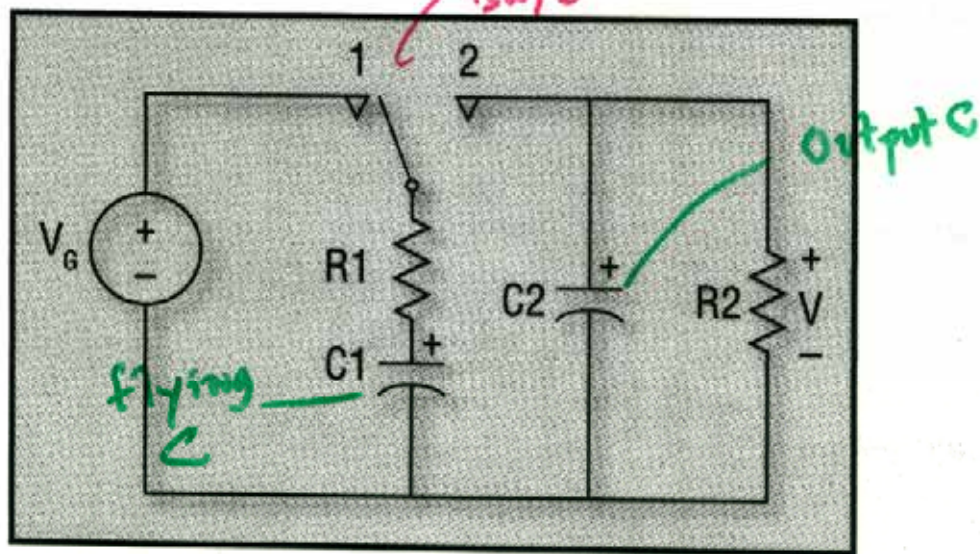


Fig. 1. The basic charge-pump circuit can be used for regulated stepdown charge pumps, inverting regulated charge pumps and inverting unregulated charge pumps.

The radio frequency spectrum and how it's allocated

All bandwidth is not created equal. The section to be auctioned is in the heart of prime frequencies for communications.

Mobile and terrestrial networks



200 MHz to 3 GHz



30 MHz



1.710 MHz to 1.755 MHz



30 GHz

30 GHz

communications

Use of air communications way



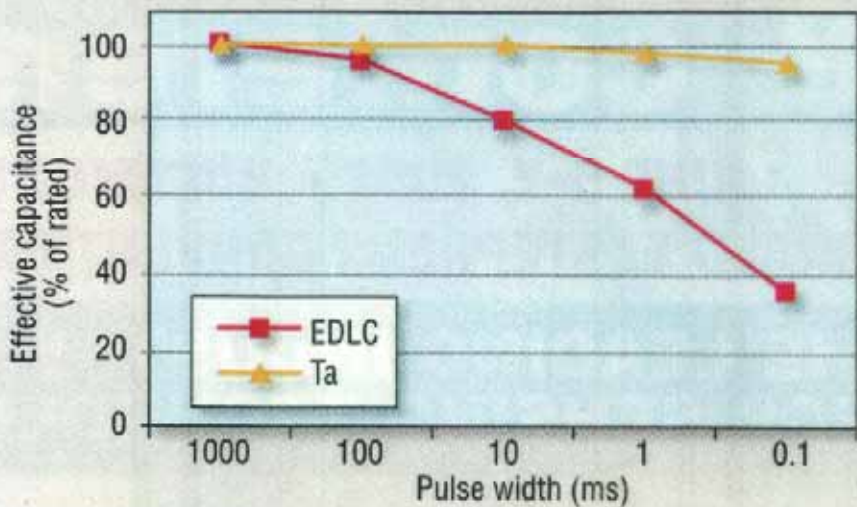


fig.3. The effective capacitance of different capacitor technologies varies as a function of pulse width.

| Design parameters | Capacitor options (Fig. 2) | | | |
|-------------------------------------|---|---|---|---|
| | Option 1 3 x 2200- μ F, 6.3-V tantalums | Option 2 2 x 2200- μ F, 6.3-V tantalums | Option 3 1 x 22,000- μ F, 4.5-V EDLCs | Option 4 1 x 35,000- μ F, 5.5-V EDLCs |
| Rated capacitance (mF) | 6.6 | 4.4 | 22 | 35 |
| Effective capacitance (mF) | 6.6 | 4.4 | 11 | 17 |
| Effective ESR (m Ω) at 20°C | 12 | 18 | 200 | 150 |
| Overall size L x W x H (mm) | 14.5 x 22.5 x 2 | 14.5 x 15 x 2 | 26 x 15 x 2.1 | 28 x 15 x 4.8 |
| Printed circuit board mounting | SMD | SMD | Hand soldered | Hand soldered |
| Voltage drop (V), GSM pulse | 0.19 | 0.30 | 0.50 | 0.37 |

Table 2. Four potential solutions to the design problem.

| Design parameter | Value |
|-----------------------|-----------------|
| PCMCIA voltage | 3.3 V max |
| PCMCIA current | 1.0 A max |
| PA input voltage | 3.0 V min |
| PA peak input current | 2.0 A max |
| GSM pulse width | 577 μ s min |

Table 1. *Design problem summary.*

PCMCIA

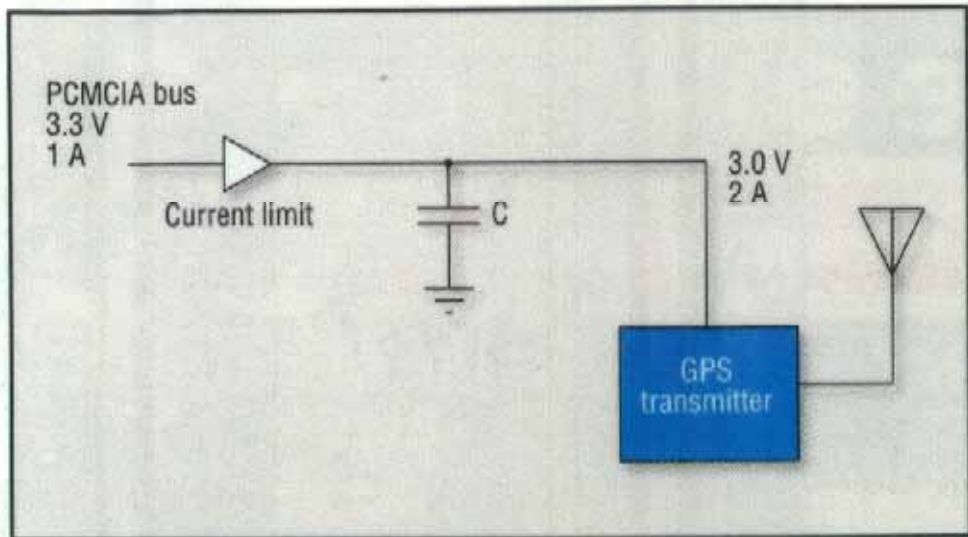


Fig. 2. The capacitor in this simplified circuit diagram must deliver the required current to the GSM transmitter while limiting the voltage drop to 0.3 V or less.

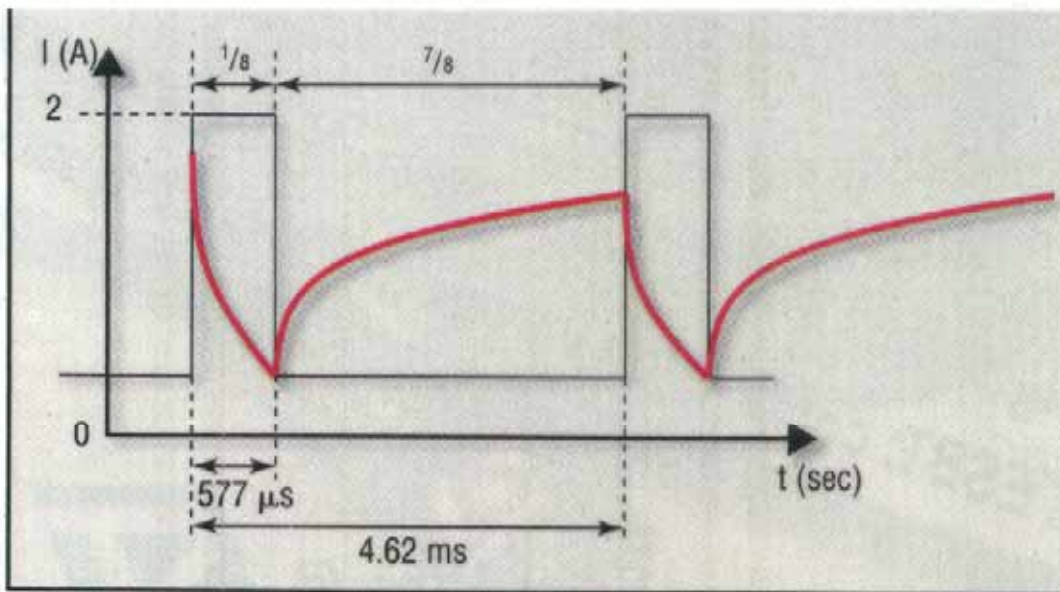


Fig. 1. During GSM transmissions, the power amplifier transmits a pulse lasting $577 \mu\text{s}$. The capacitor supplying this current must charge during the remaining portion of the cycle.

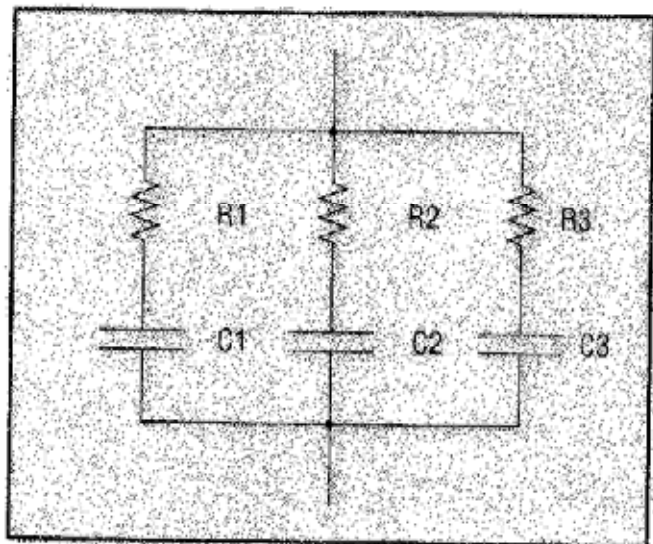


Fig. 4. Paralleling three tantalum capacitors provides 6.6 mF of capacitance with an effective ESR of 12 m Ω .