ECE 562

Week 10 Lecture 2

Fall 2008

Week 10 Lecture 2
Summary

Slides	Topic
3-12	Transistor types, switch losses, and packaging
13-18	Capacitor and inductor selection
19-26	Flyback converter examples
27-31	Transformer losses
32-53	Forward converter
54-66	Roles of diodes
67-80	Forward converter and diode reset
81-104	Active clamping of transformer

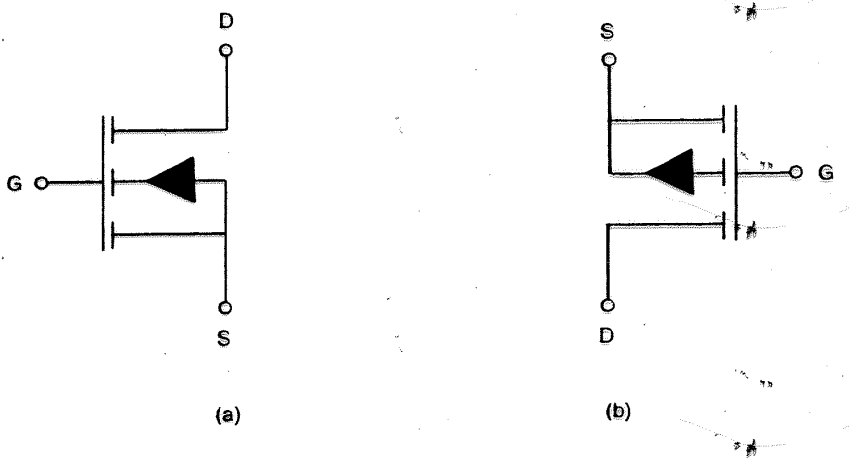


Figure 3–4 (a) N-channel MOS transistor and (b) P-channel MOS transistor complete of "bulk" terminal.

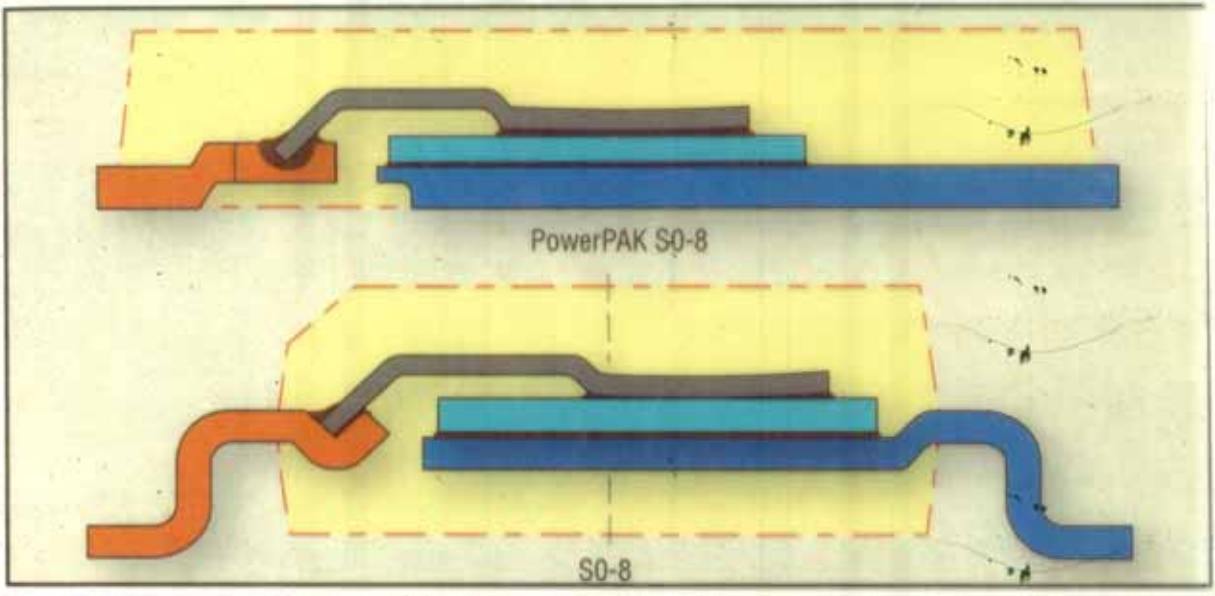


Fig. 2. *Cross-sectional views of the PowerPAK SO-8 and standard SO-8 packages reveal differences in lead-frame construction that impact package height and inductance.*

Get On The High Side With Micrel

High-side load switches offer the lowest $R_{DS(ON)}$, high efficiency and smalle

Switch and I^2 R Losses in Q1

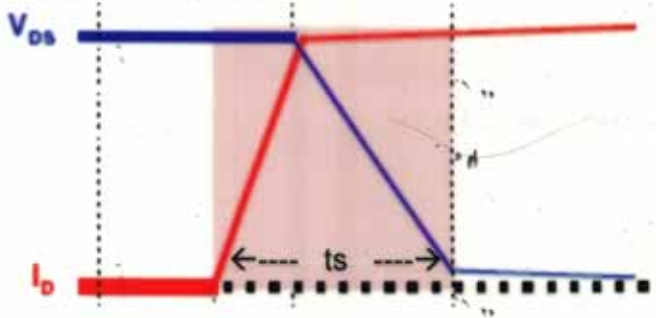
- Gate charge Q_G (given on MOSFET spec sheet) is needed at gate to switch the FET

$$P_{upper} = P_{sw} + P_{cond} \rightarrow$$

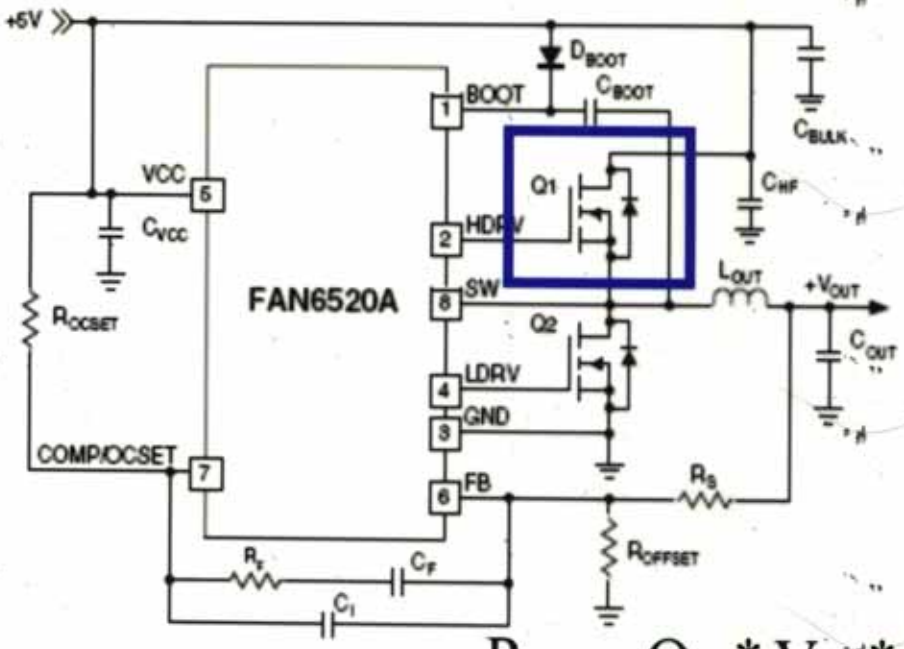
$$\left(\frac{V_{ds} * I_1}{2} * 2 * t_s\right) * F_{sw} + \left(\frac{V_{out}}{V_{in}} * I_{out}^2 * R_{ds(on)}\right)$$

*Rds(on) is taken at max. junction temp. (125° C for 6520A)

$$t_s \approx \frac{Q_{g(sw)}}{I_{driver}}$$



FETS Gate Losses:~ $C_G V^2 F_{SW}$



$$P_{gate} = Q_g * V_{cc} * F_{sw}$$

Four FET's
Program as buck boost

$V_{in} > V_{out}$
Q_1 and Q_2 synch
$V_{in} < V_{out}$
Q_3 and Q_4 synch

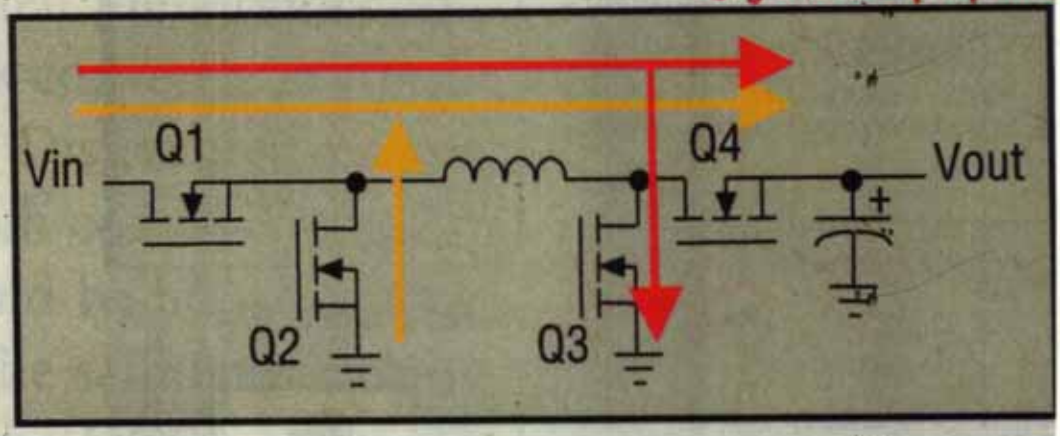


Fig. 1. *Buck-boost configuration. Yellow arrows show the direction of current flow as a buck. Red arrows show the direction of current flow when acting as a flyback.*

The New Juice Box

Methanol, butane and other gase

Associated Press

Toshiba's direct methanol fuel cell was certified as the smallest in the world

may help solve the age-old battery problem.

Inside Lilliputian Systems' fuel cell chip

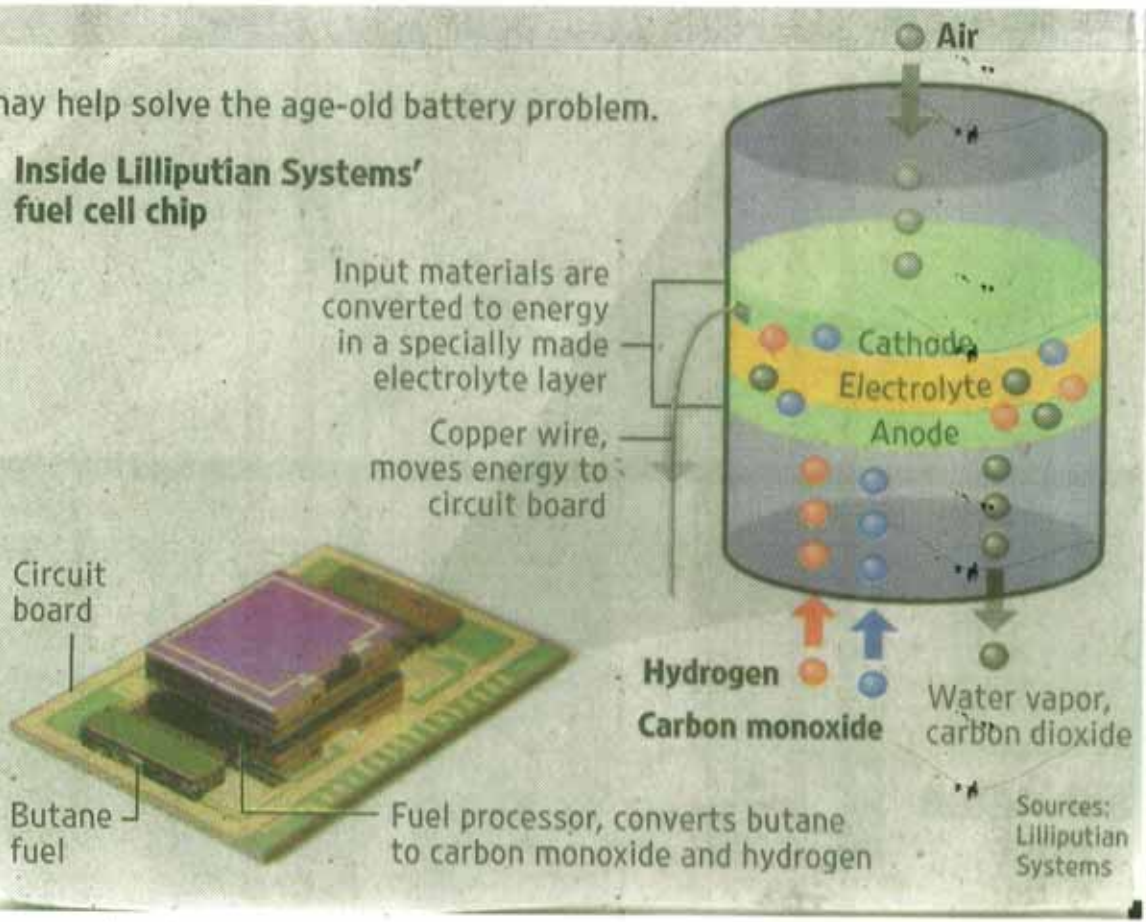


Fig. 2. *Chip-scale packaging has enabled the miniaturization of linear battery-charger circuits.*

Capacitor Selection

•Parallel Output Capacitors

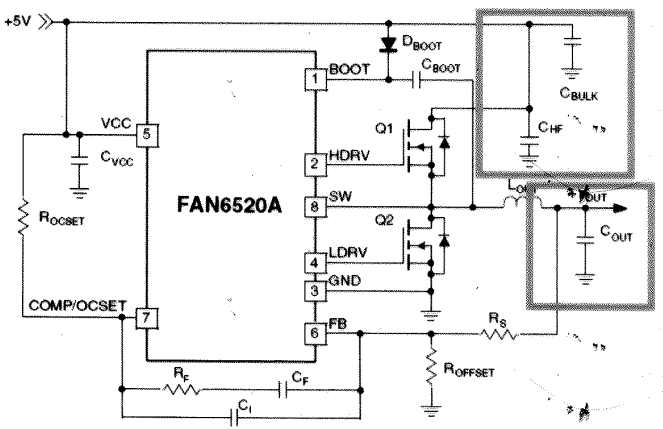
- Bulk Capacitor Considerations

  ESR

  Voltage Rating

- High Frequency Capacitor Considerations

  ESL

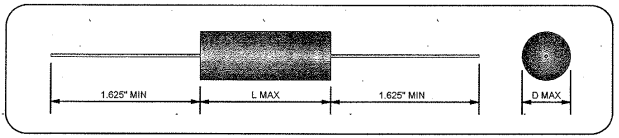


For 5kV Application

ASC CAPACITORS

METALLIZED POLYESTER TAPE WRAP AND EPOXY FILL CASE

X675



2000VDC				
CAP (µF)	D MAX	L MAX	LEAD AWG	I_{PEAK} (A)
0.0010	0.250" (6.4mm)	1.284" (32.6mm)	22	0.1
0.0015	0.250" (6.4mm)	1.284" (32.6mm)	22	0.2
0.0022	0.250" (6.4mm)	1.284" (32.6mm)	22	0.2
0.0033	0.290" (7.4mm)	1.284" (32.6mm)	22	0.4
0.0047	0.310" (7.9mm)	1.284" (32.6mm)	22	0.5
0.0068	0.350" (8.9mm)	1.284" (32.6mm)	22	0.7
0.010	0.380" (9.7mm)	1.284" (32.6mm)	22	1.1
0.015	0.460" (11.7mm)	1.284" (32.6mm)	20	1.7
0.022	0.520" (13.2mm)	1.284" (32.6mm)	20	2.4
0.033	0.590" (15.0mm)	1.284" (32.6mm)	20	3.6
0.047	0.730" (18.5mm)	1.284" (32.6mm)	20	5.2
0.068	0.570" (14.5mm)	1.914" (48.6mm)	20	2.3
0.10	0.630" (16.0mm)	1.914" (48.6mm)	20	3.4
0.15	0.780" (19.8mm)	1.914" (48.6mm)	20	5.1
0.22	0.890" (22.6mm)	1.914" (48.6mm)	20	7.5
0.33	1.000" (25.4mm)	1.914" (48.6mm)	20	11.2
0.47	1.250" (31.8mm)	1.914" (48.6mm)	20	16.0
0.68	1.500" (38.1mm)	1.914" (48.6mm)	20	23.1
1.0	1.800" (45.7mm)	1.914" (48.6mm)	20	34.0

4000VDC				
CAP (µF)	D MAX	L MAX	LEAD AWG	I_{PEAK} (A)
0.0010	0.275" (7.0mm)	1.284" (32.6mm)	22	0.2
0.0015	0.300" (7.6mm)	1.284" (32.6mm)	22	0.3
0.0022	0.325" (8.3mm)	1.284" (32.6mm)	22	0.5
0.0033	0.350" (8.9mm)	1.284" (32.6mm)	22	0.7
0.0047	0.400" (10.2mm)	1.284" (32.6mm)	22	1.0
0.0068	0.450" (11.4mm)	1.284" (32.6mm)	20	1.5
0.010	0.500" (12.7mm)	1.284" (32.6mm)	20	2.2
0.015	0.600" (15.2mm)	1.284" (32.6mm)	20	3.3
0.022	0.475" (12.1mm)	1.914" (48.6mm)	20	1.5
0.033	0.560" (14.2mm)	1.914" (48.6mm)	20	2.2
0.047	0.660" (16.8mm)	1.914" (48.6mm)	20	3.1
0.068	0.775" (19.7mm)	1.914" (48.6mm)	20	4.5
0.10	0.950" (24.1mm)	1.914" (48.6mm)	20	6.6
0.15	1.100" (27.9mm)	1.914" (48.6mm)	20	9.9
0.22	1.300" (33.0mm)	1.914" (48.6mm)	20	14.5
0.33	1.500" (38.1mm)	1.914" (48.6mm)	20	21.8

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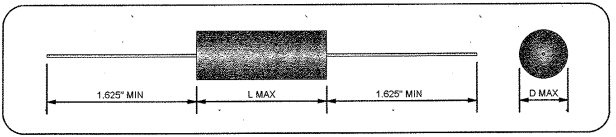

6000VDC				
CAP (µF)	D MAX	L MAX	LEAD AWG	I_{PEAK} (A)
0.0010	0.320" (8.1mm)	1.664" (42.3mm)	22	0.2
0.0015	0.330" (8.4mm)	1.664" (42.3mm)	22	0.3
0.0022	0.350" (8.9mm)	1.664" (42.3mm)	22	0.4
0.0033	0.400" (10.2mm)	1.664" (42.3mm)	22	0.6
0.0047	0.430" (10.9mm)	1.664" (42.3mm)	20	0.8
0.0068	0.500" (12.7mm)	1.664" (42.3mm)	20	1.2
0.010	0.580" (14.7mm)	1.664" (42.3mm)	20	1.7
0.015	0.680" (17.3mm)	1.664" (42.3mm)	20	2.6
0.022	0.800" (20.3mm)	1.664" (42.3mm)	20	3.8
0.033	0.650" (16.5mm)	2.664" (67.7mm)	20	3.4
0.047	0.740" (18.8mm)	2.664" (67.7mm)	20	4.8
0.068	0.880" (22.4mm)	2.664" (67.7mm)	20	6.9
0.10	1.060" (26.9mm)	2.664" (67.7mm)	20	10.2
0.15	1.200" (30.5mm)	2.664" (67.7mm)	20	15.3

8000VDC				
CAP (µF)	D MAX	L MAX	LEAD AWG	I_{PEAK} (A)
0.0010	0.320" (8.1mm)	2.034" (51.7mm)	22	0.2
0.0015	0.350" (8.9mm)	2.034" (51.7mm)	22	0.3
0.0022	0.380" (9.7mm)	2.034" (51.7mm)	22	0.5
0.0033	0.430" (10.9mm)	2.034" (51.7mm)	20	0.7
0.0047	0.480" (12.2mm)	2.034" (51.7mm)	20	1.1
0.0068	0.560" (14.2mm)	2.034" (51.7mm)	20	1.5
0.010	0.660" (16.8mm)	2.034" (51.7mm)	20	2.3
0.015	0.780" (19.8mm)	2.034" (51.7mm)	20	3.4
0.022	0.940" (23.9mm)	2.034" (51.7mm)	20	5.0
0.033	1.110" (28.2mm)	2.034" (51.7mm)	20	7.5
0.047	0.830" (21.1mm)	3.344" (84.9mm)	20	6.2
0.068	1.025" (26.0mm)	3.344" (84.9mm)	20	9.0
0.10	1.250" (31.8mm)	3.344" (84.9mm)	20	13.2

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Inductor Selection

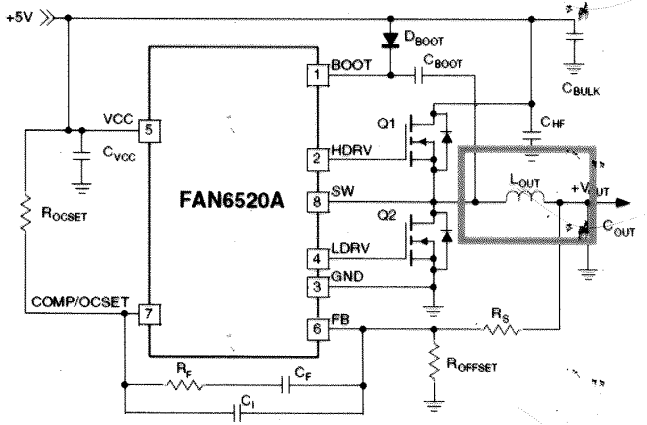
•Output Inductors

- Designed to:

  Meet output voltage ripple requirements

  Minimize response time to load transient

  Avoid saturation of the inductor core



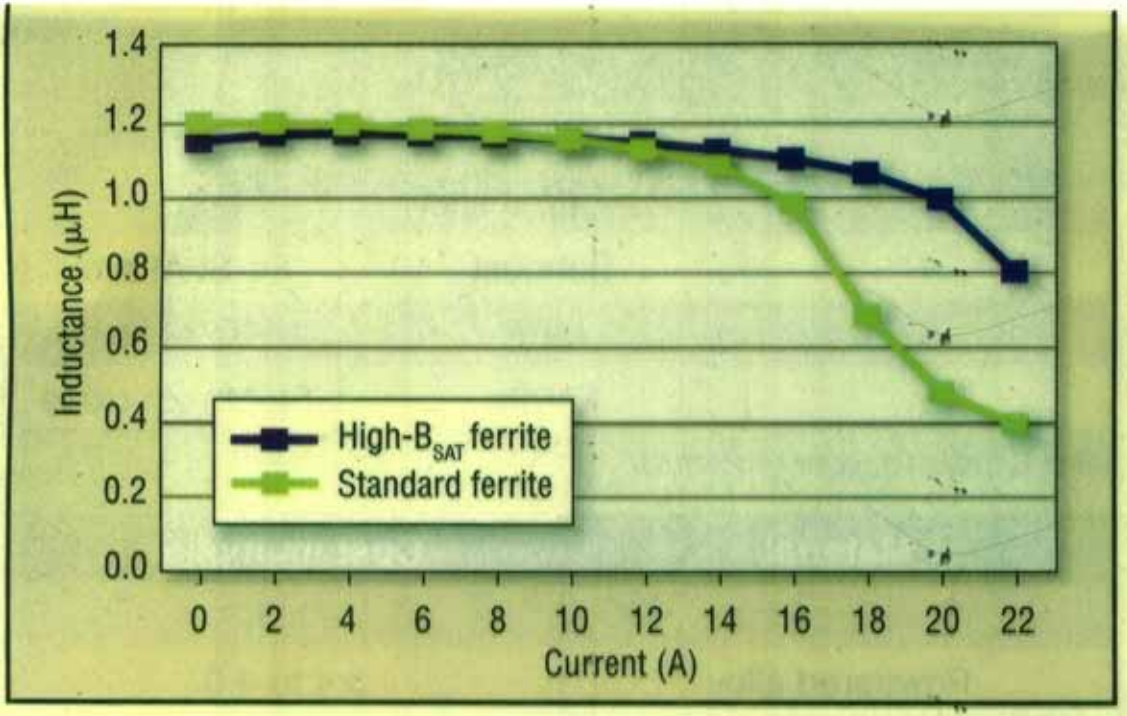


Fig. 1. *The effect of saturation in an inductor using a high-B_{SAT} material is significantly lower than that in an identical conductor using standard ferrite-powder material.*

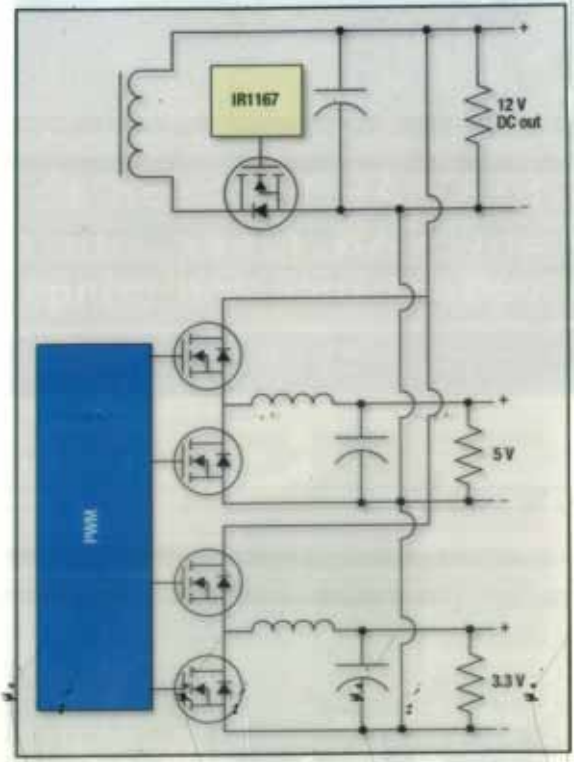


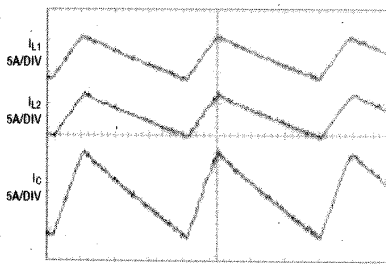
Fig. 7. *A multi-output secondary stage can be implemented using buck converters fed from a single secondary-side winding regulated with a SmartRectifier IC, assuming a flyback converter primary winding.*

Multiple Phases are Interleaved

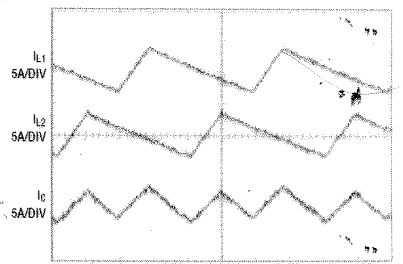
- Operation From **One to Twelve Phases**
- Current up to 200A total current divided between FETS

OUTPUT CURRENT	<35A	35A TO 70A	70A TO 105A	105A TO 140A	140A TO 200A
No. of LTC1629s	1	2	3	4	6
Buck Stages	2	4	6	8	12

- Phases Operate **Interleaved to reduce current ripple**
  - ☐ Effectively Multiplies Frequency by Number of Phases
  - ☐ Reduces Output Ripple



(a) Single-Phase



(b) Dual-Phase

Active Care of Trf saturation

Transformer reset

$i_m \leq i_{critical}$ Prevents Core Saturation

return i_m to zero

- "Transformer reset" is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance

+ V-sec = -V-sec

Downside of transformers

timing cost but law!

Key

Lecture 15
The Forward PWM Converter Circuit Topology and Illustrative Examples

quantative example "last" lecture

I. Erickson Problem 6.4 A DCM Two Transistor Flyback Converter

II. Forward Converter

Key

A. Overview

B. Forward Converter with a Three Winding Transformer Drive: Two Case Studies

done → 1. One Transistor Implementation

NEXT → 2. Two Transistor Implementation

} V_{max} solve issues ON Q lower P.I.V.

C. Forward Converter Transformer

D. External Reset of a Transformer: Erickson Problem 6.9

You make sure it occurs properly as engineer

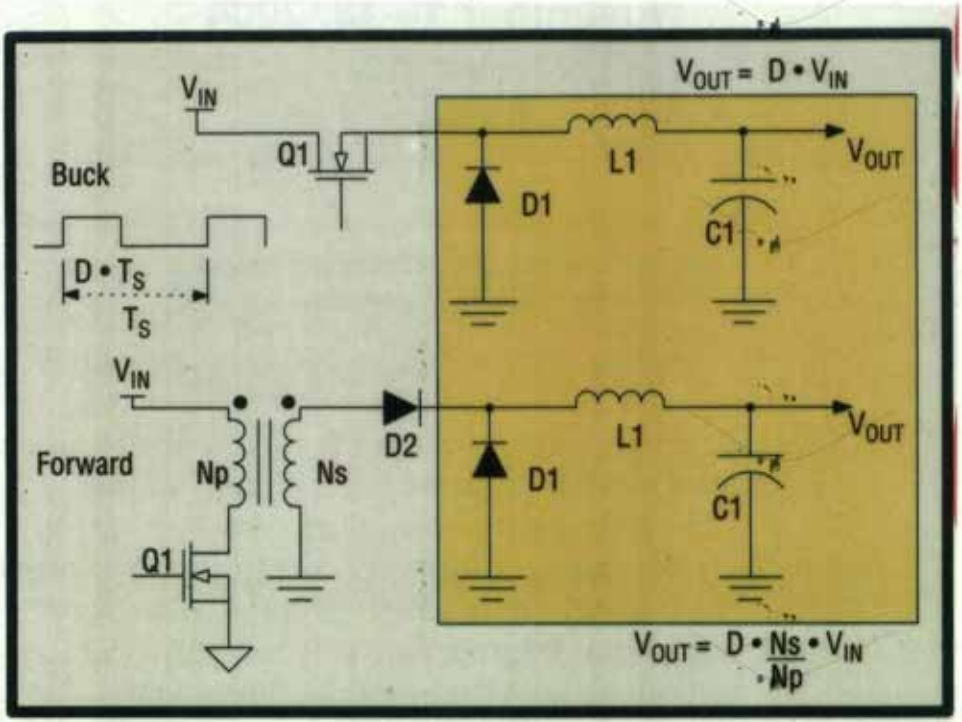


Fig. 1. *Buck and forward topology.*

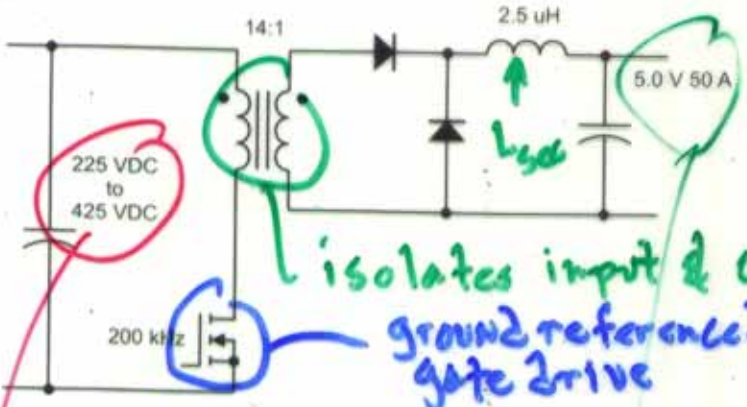


Figure 1 : Forward converter designed for rugged operation.

V_g (rail) very high for? Server with 10^3 µP

V_{out} low eg < 1.0 V

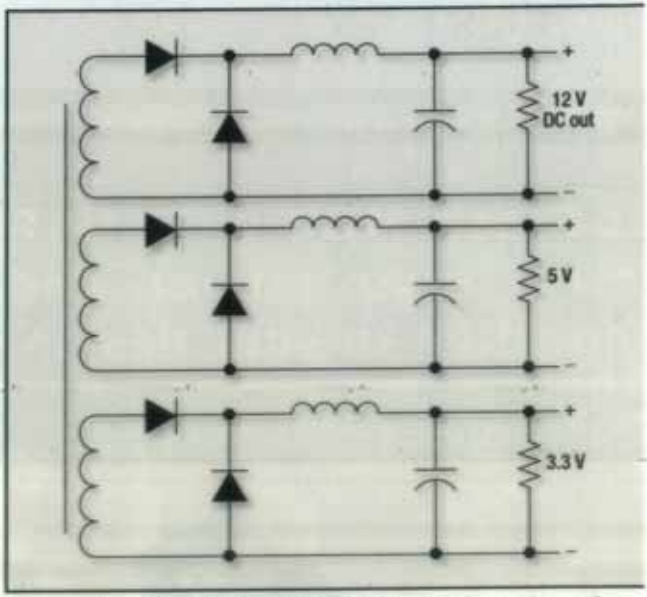


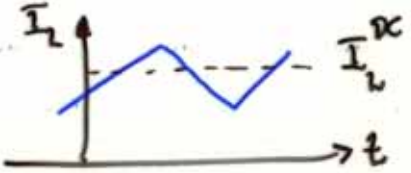
Fig. 6. *Traditionally, Schottky diodes provide secondary-side rectification in multi-output power supplies.*

1. Buck
No Trf $V_o = D V_{IN}$

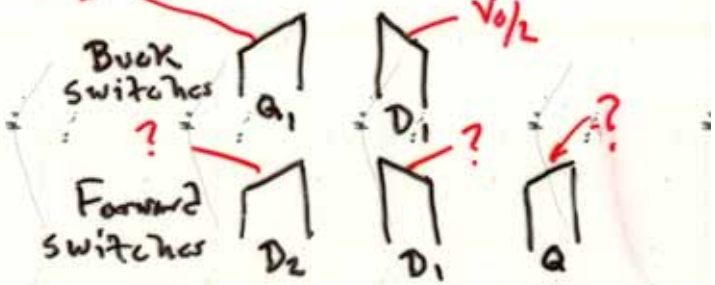
2. Buck with Trf
big V_{max} on D_1
$V_o = \left(\frac{N_s}{N_p}\right) V_{IN}$ D
big $\frac{1}{T}$
step down
fine tune

Forward
Floating gate drive eliminated
Small V_{max} on L_1 by $\frac{N_s}{N_p}$
Need extra diode D_2

Both cases



$\frac{V_{IN}-V_o}{L}$



Adv of Trf

① Isolation: seperate grounds V_p & V_{sec} and multiple N_s coils for multiple V_{out}

② Q_1 will have lower I_{max} in primary of a step down trf

V_{GS} w.r.t ground!

$\frac{V_s}{V_p}$ step down

③ $V_o = D V_{IN} \left(\frac{N_s}{N_p} \right)$

Buck step down

Trf

$D \cdot \frac{N_s}{N_p}$

④ L_m for Forward Trf big ? small ?

⑤ Which and Why CCM vs DCM goals

Effect choice of $L_{(buck)}$ IN secondary

reset trf

reset circuits

IN sec

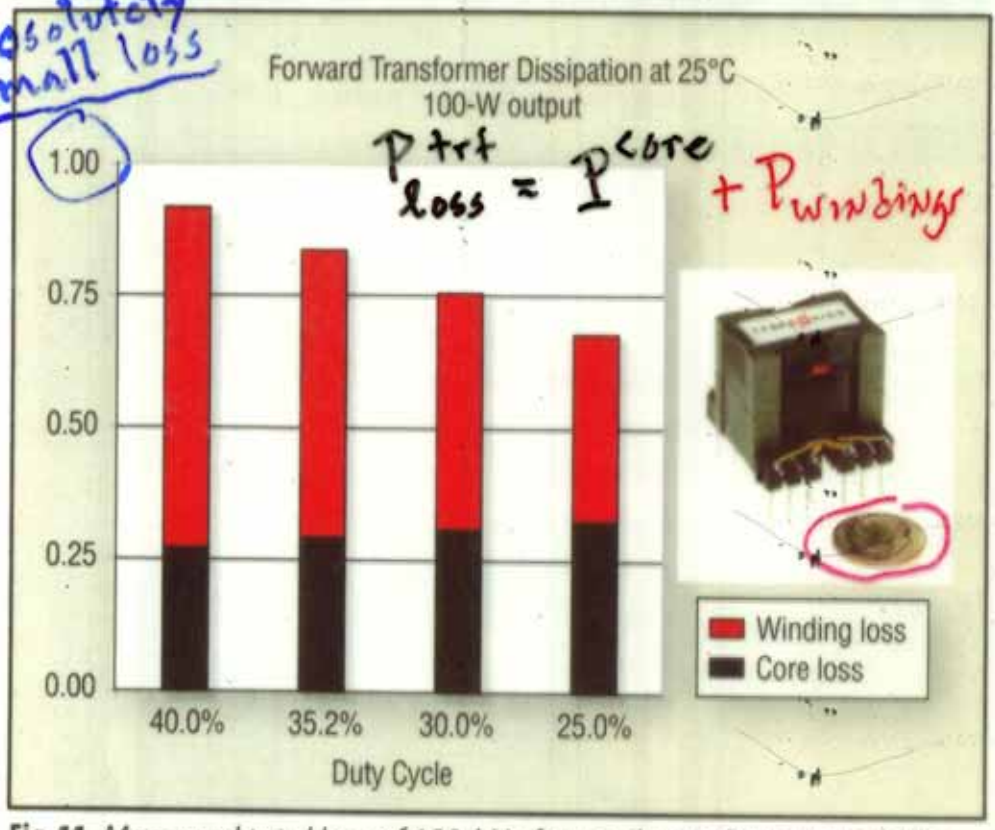


Fig. 11. *Measured total loss of 100-kHz forward transformer providing 20 V at 5 A.*

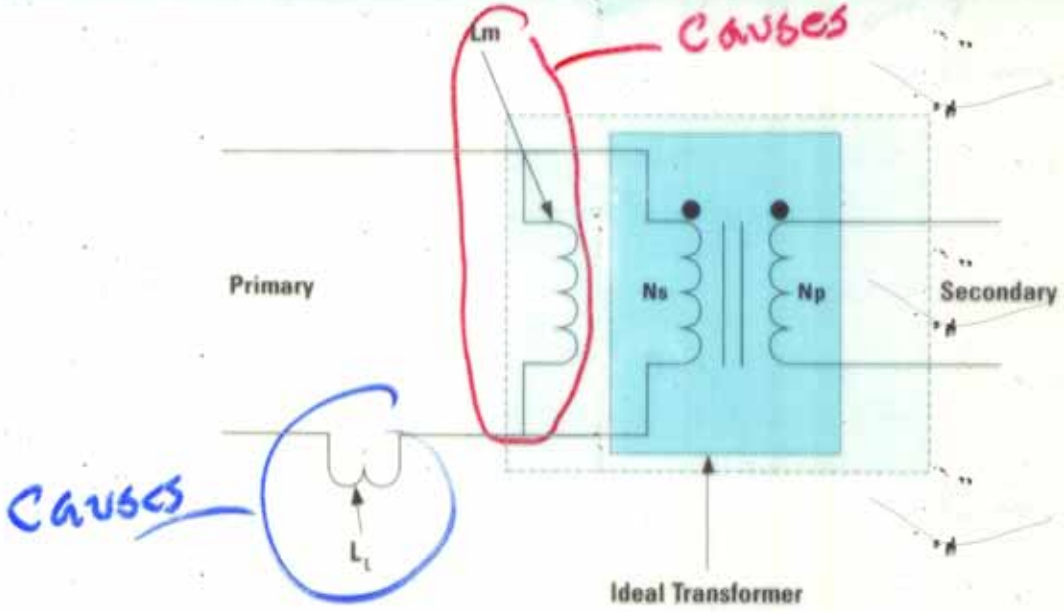


Figure 2. Transformer Model

Disadvantage of Trf

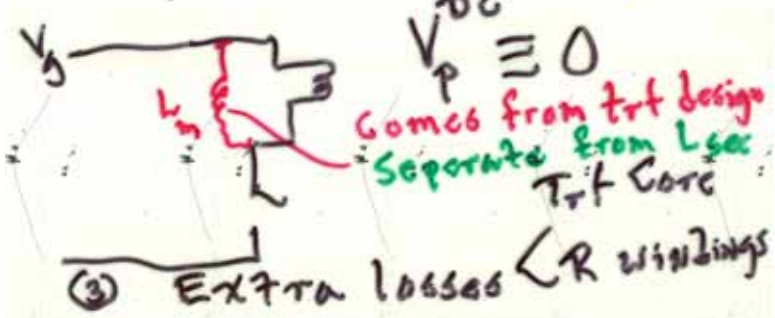
Worst case

(1) Saturation of L_m by V-sec from big V_{IN}

⇒ (1) desire large L_m value to avoid saturation

⇒ (2) Will need active trf reset as well - how achieved?

(2) No residual V_{DC} on input to Trf allowed ☹



Ways to insure L_m does not saturate

① Make sure i_{L_m} always returns to "0" over a switch cycle — Operate DCM

⇒ small L (sec) only will cause Buck $\Pi i > I_{oc}$

② Insure equal & opposite V-sec on L_m over a CCM switch cycle — add a third winding and a clamp diode

tive cost, complexity and efficiency tradeoffs. The forward converter is derived from the buck topology family,

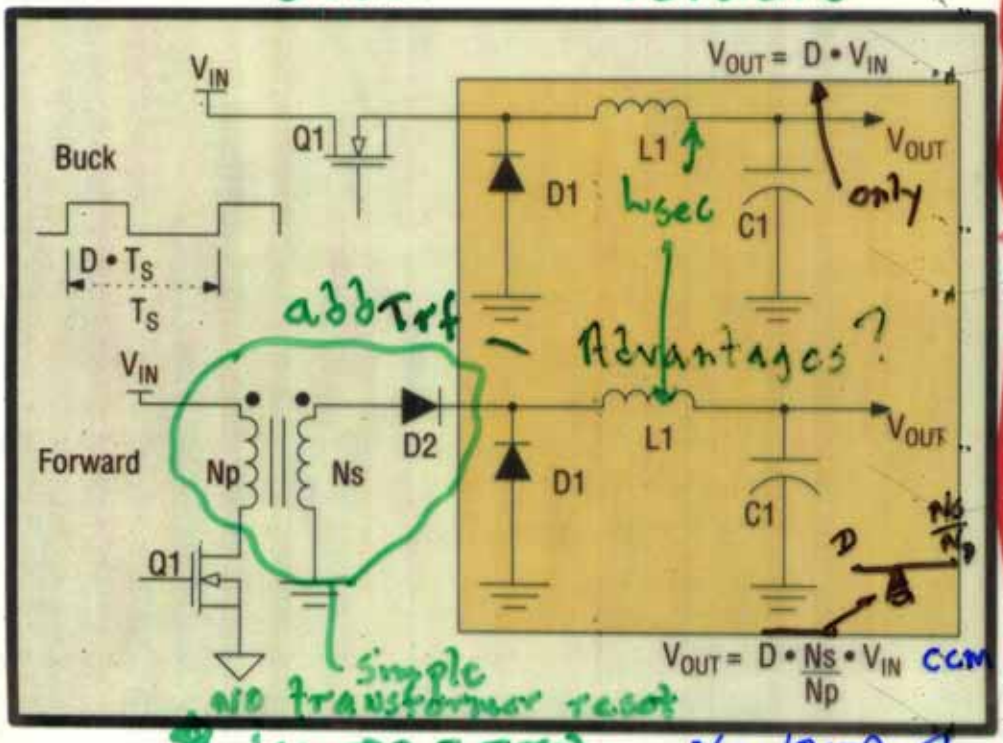
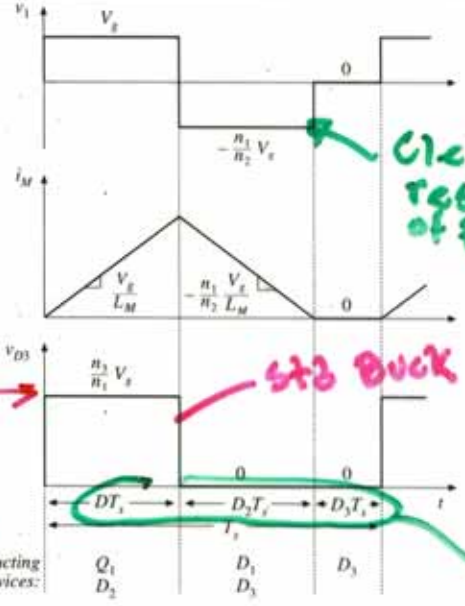


Fig. 1. *Buck and forward topology.*

Forward converter: waveforms

DCM



- Magnetizing current, in conjunction with diode D_1, operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode D_3, may operate in either CCM or DCM

Clever reset of flux

back bias D_3 forward bias D_2

stb Buck

$V_0 = D \frac{n_3}{n_1} V_g$

Next Details !

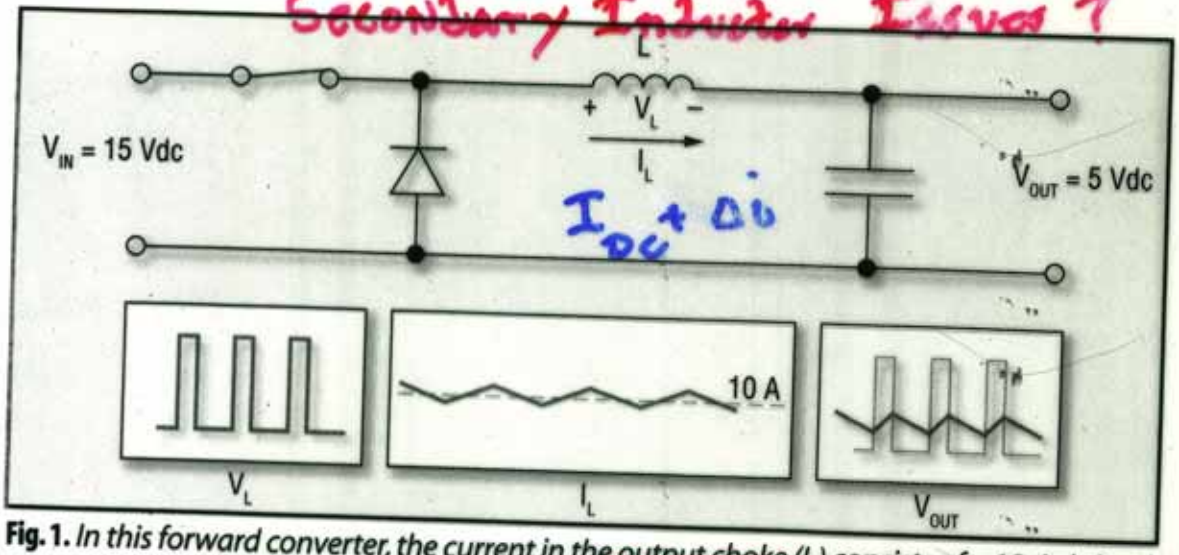


Fig. 1. *In this forward converter, the current in the output choke (I_L) consists of a 10-A dc load current and a saw-tooth current that is determined by the voltage across L and the value of its inductance.*

Inductor core saturation
Same considerations..
as in Buck inductor
Air Gap for L_{sec} coil!

Δi small
CCM
can push I^2_{DC} ↑

Δi big DCM
must limit
I^2_{DC} ≤ $I^{core}_{critical}$

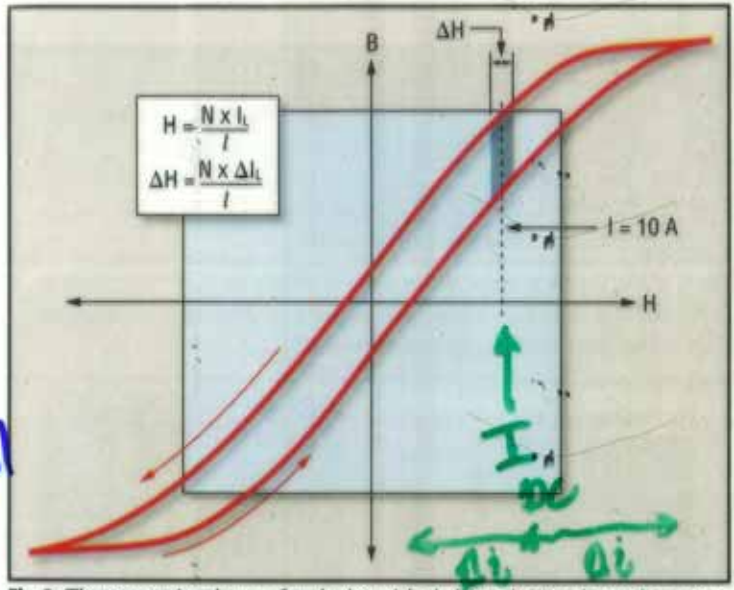


Fig. 2. *The operating loop of a choke with dc bias depicts how the magnetic flux density (B) is also shifted from its normal loop around zero.*

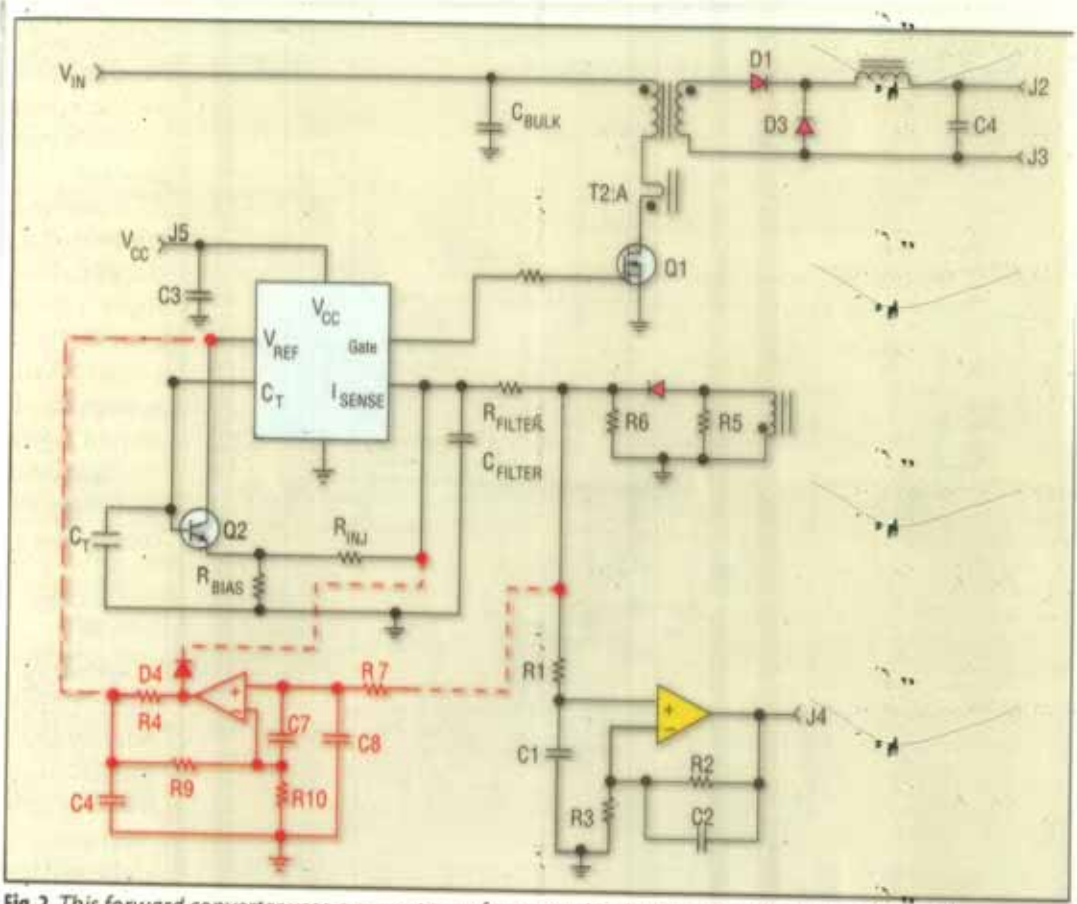


Fig. 2. *This forward converter uses a current transformer and includes overcurrent protection (red).*

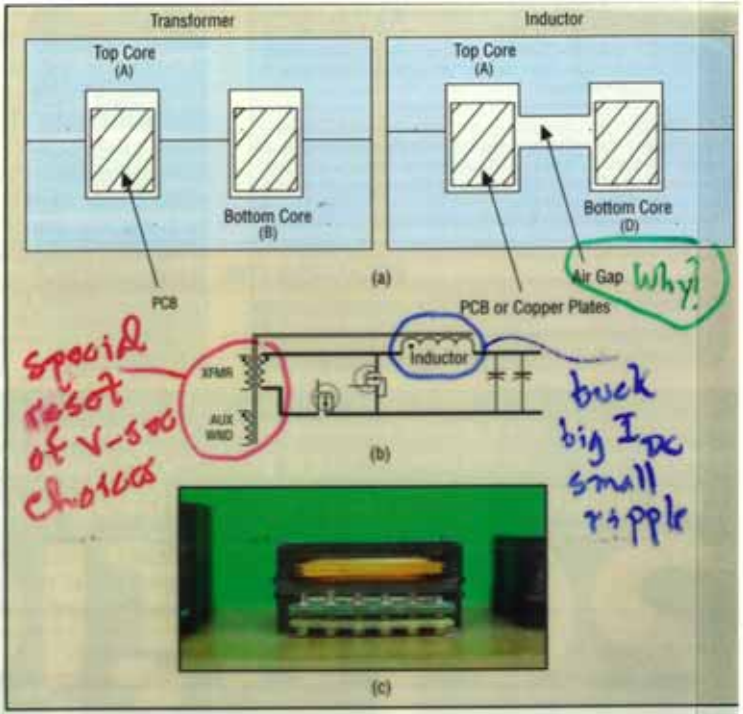


Fig. 1. *Forward converter with integrated magnetics. Shown here are the cross-sectional diagrams of the transformer and inductor when constructed separately (a), the forward converter schematic when magnetics are integrated (b) and a photo of the integrated planar magnetic device (c).*

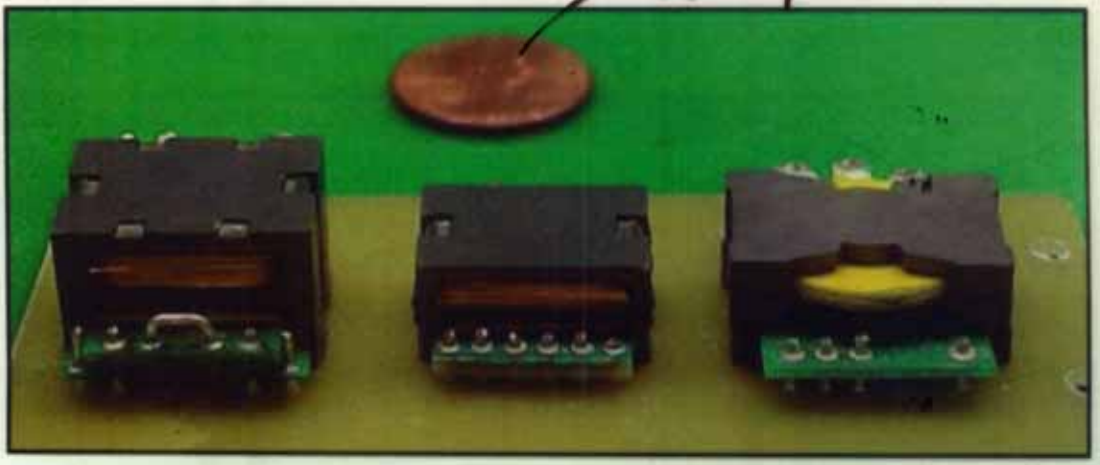
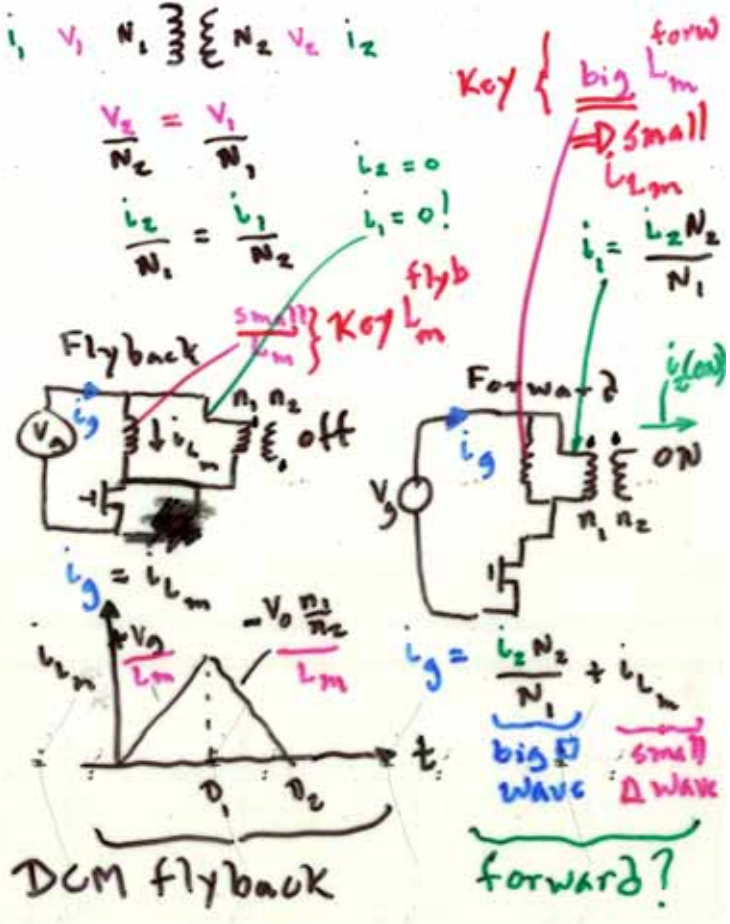


Fig. 7. *Inductors on top and transformers on bottom are integrated into one structure of different shapes and sizes*

Flyback vs Forward Trf



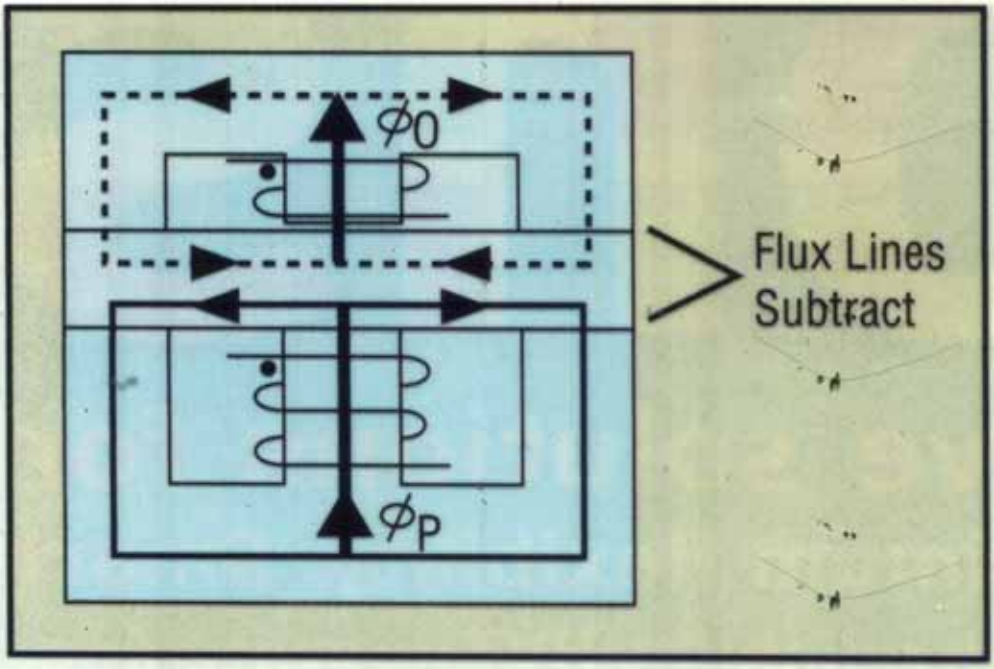


Fig. 2. *Placing a high reluctance path (air gap) minimizes the magnetic interaction between transformer and inductor.*

Summarize $V_{Lm}(t)$ $I_{Lm}(t)$

$D_1 T_{sw}$ V_g I_{Lm} and increasing V_g/L_m L_m Q_1 ON

and decreasing

$D_2 T_{sw}$ L_m D_1 ON

$-\frac{N_1}{N_2}\frac{V_g}{L_m}$

$\frac{-V_g}{N_2} \approx \frac{V_{Lm}}{N_1}$

N_2 coil N_1 coil

$\frac{N_1}{N_2} > 1$ forces DCM

I_{Lm} $\frac{V_g}{L}$ $\frac{V_g}{L}\frac{N_1}{N_2}$ t

$D_1 \rightarrow \leftarrow D_2 \leftarrow D_3 \rightarrow$

Quantative Conditions for Transformer reset

D_1 choice & ratio $\frac{N_2}{N_1}$ >1 $=1$ <1 ?

From magnetizing current volt-second balance:

$$\langle v_1 \rangle = D(V_g) + D_2(-V_g n_1/n_2) + D_3(0) = 0$$

To insure No L_m saturation

Solve for D_2:

$$D_2 = \frac{n_2}{n_1} D$$

D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

$$D_3 = 1 - D - D_2 \geq 0$$

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0$$

Solve for D

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

for $n_1 = n_2$: $D \leq \frac{1}{2}$

$\pm V_g$ on V_p

(1) Reset for CCM Forward

(2) To achieve DCM

limited D_{ON} in Forward

$D_3 T_{sw}$

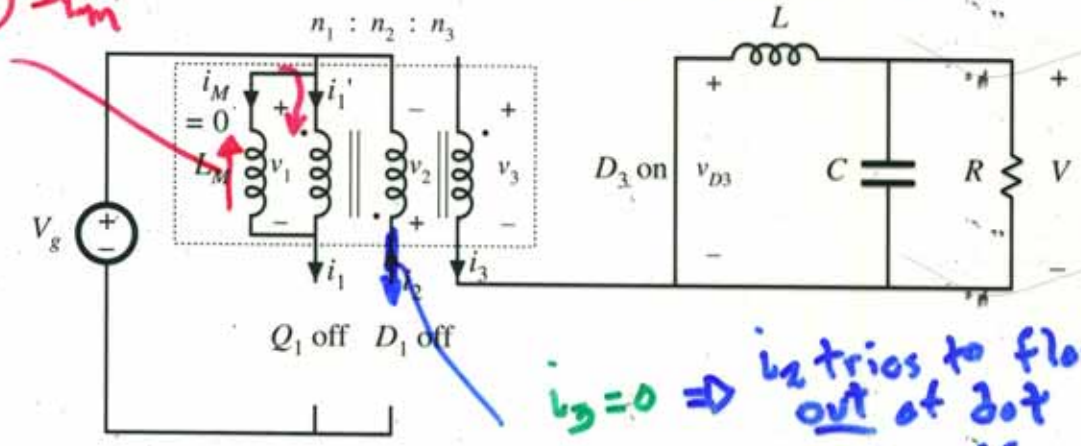
Subinterval 3

DCM condition

$i_{L_m} \to 0$

if proper conditions

$-I_{Lm}$



$i_3 = 0 \Rightarrow$ i_2 tries to flow out of dot

D_1 off

interval

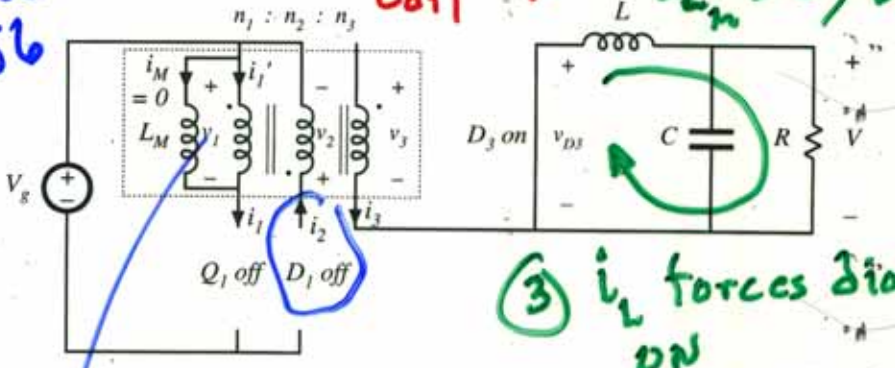
If D_1 short enough $i_{Lm}(max)$ is low

(2) Interval 3 Caused by i_{Lm} going → 0

All coils $i_{coil} = ?$

$i_{Lm} \to 0$, D_1 off

Fig 6.25c
Pg 256

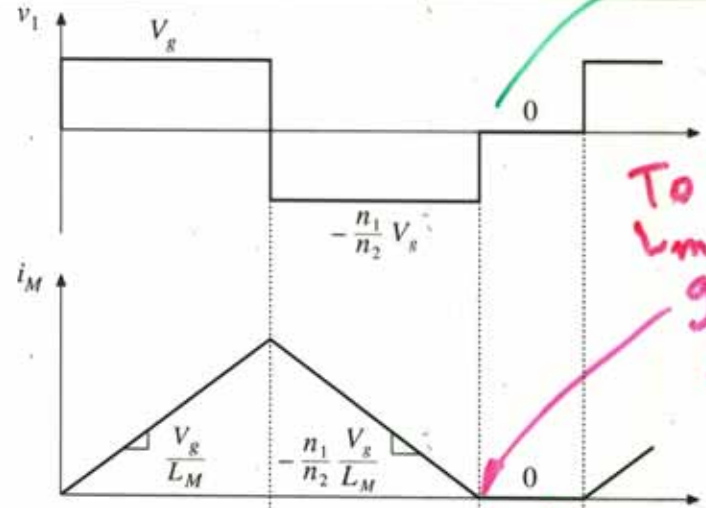


(3) i_L forces diode 3 ON

Is $V_{DS} = 0$ for both D_2 & D_3 intervals ?

(1) $i_{Lm} = 0$ dry ⇒ $V_1 = 0$

Magnetizing inductance volt-second balance



$$\langle v_1 \rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

$i_M = 0$ & flat $\Rightarrow V_{L_m} = 0$

To insure no L_m saturation goal: $v_{L_m} = 0$ each SW cycle

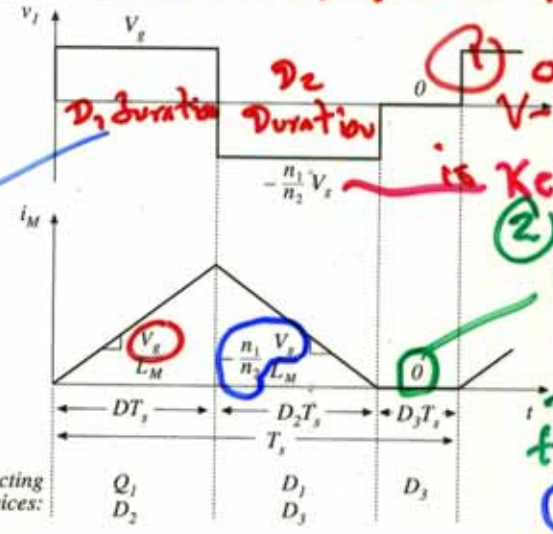
Force a D_3 interval

Quantifying Trf. Reset Condition

Magnetizing inductance volt-second balance

ON coil #1 (L_m)

Fig 6.24 pg 155

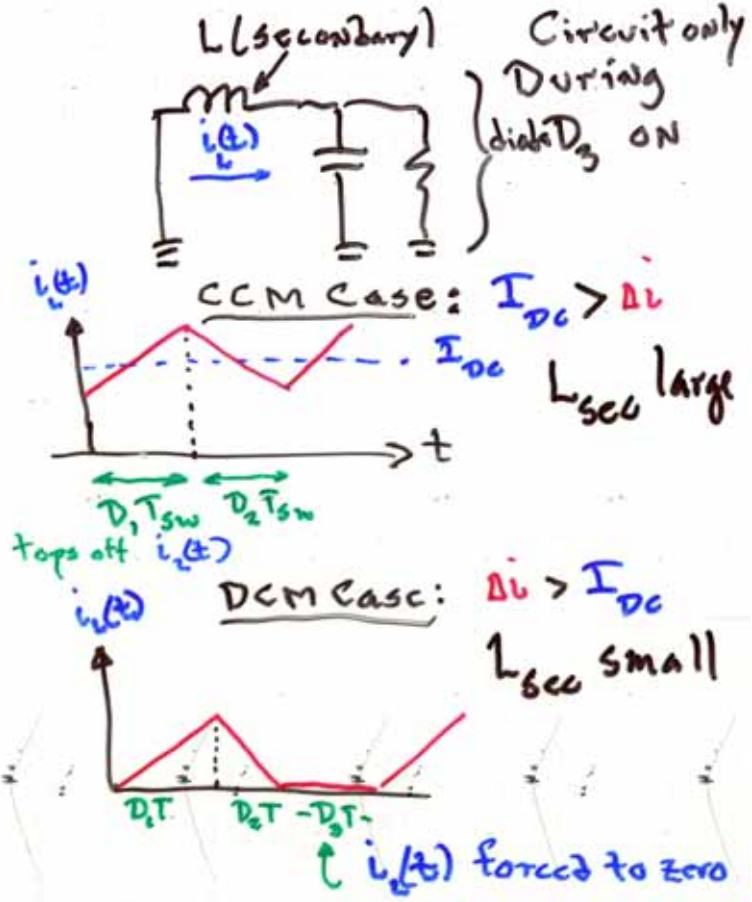


(1) ON coil #1 V-sec balance is Key! D_1 is time!

(2) $i_M \to 0$ is a Must for reset of L_m hence why DCM best for doing so

(2) Solve for D_2 as D_1 is set by Q control

(3) Times: D_1, D_2, D_3: $\langle v_l \rangle = D(V_g) + D_2(-V_g n_1/n_2) + D_3(0) = 0$

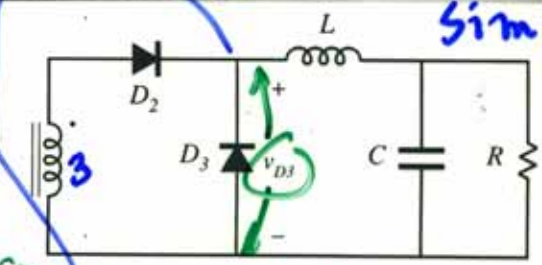

L (secondary)
Circuit only
During
diode D_3 ON
$i_L(t)$
CCM Case: $I_{DC} > \Delta i$
I_{DC}
L_{sec} large
t
$D_1 T_{sw}$
$D_2 T_{sw}$
tops off $i_L(t)$
DCM Case: $\Delta i > I_{DC}$
L_{sec} small
$D_1 T$
$D_2 T$
$D_3 T$
$i_L(t)$ forced to zero

-Vpreally

(1) $V = \frac{N_3}{N_1} V_g$ during D_1 interval

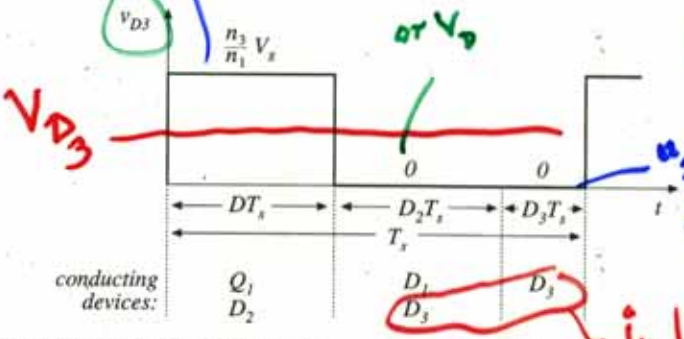
Conversion ratio $M(D)$

(2) Note secondary appears CCM Simple Buck with tr. while Lm operates DCM



(3) Find "Buck" ON average

$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} D V_g$$



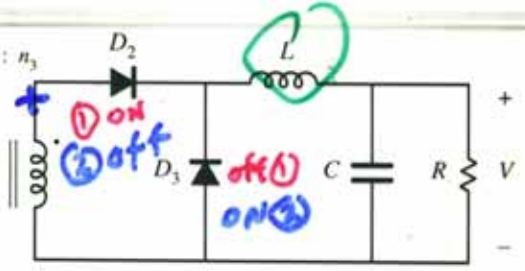
"1" ≈ 0 for $\frac{n_3}{n_1} V_g$ large

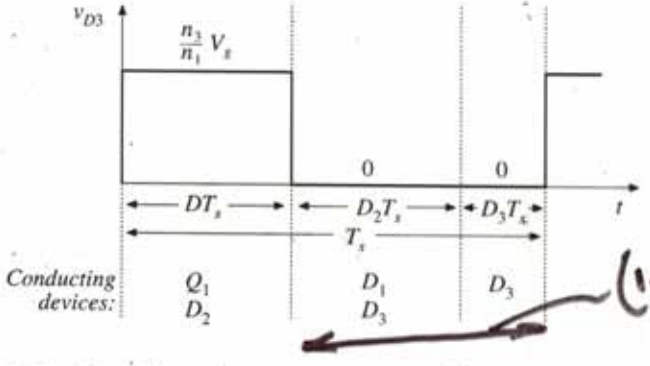
i_L (Buck) flows"

(1) During $D_1 T_{sw}$: Q_1 ON D_3 off

(2) During $D_2 T_{sw}$: Q_2 off but D_1 ON causes $n_3 \Rightarrow D_2$ off, D_3 ON (due to L)

Conversion ratio $M(D)$





$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} D V_g$$

CCM & DCM

$(1-D_1)$ interval of time

D_3 is ON !

$\frac{N_2}{N_1}$ or $\frac{N_1}{N_2}$ choices

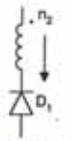
#1 $\frac{N_1}{N_2} > 1 \Rightarrow$ DCM mode

ramp down at $\frac{\left(\frac{N_1}{N_2}\right) V_g}{L_m}$

But

$$V_Q^{off} = \left(1 + \frac{N_1}{N_2}\right) V_g$$

Oh no V stress!



But i_2 tries to flow out but diode D_1 does not allow this direction of current flow. So diode D_1 goes off.

Likewise i_{Lm} flow into n_1 dot $\Rightarrow$ current flow into the n_3 dot and D_3 is turned on when i_{Lm} hits zero.
Since both transistor Q_1 and diode D_1 are off i_{Lm} remains zero for the whole period D_3T_s.
A tradeoff must be made in the forward converter since:

$D_2 = \frac{n_2}{n_1} D_1$ moving the turns ratio $\frac{n_2}{n_1}\downarrow$ allows the interval $D_1\uparrow$ for fixed interval D_2

$\frac{n_2}{n_1}\downarrow \Rightarrow D_1\uparrow$

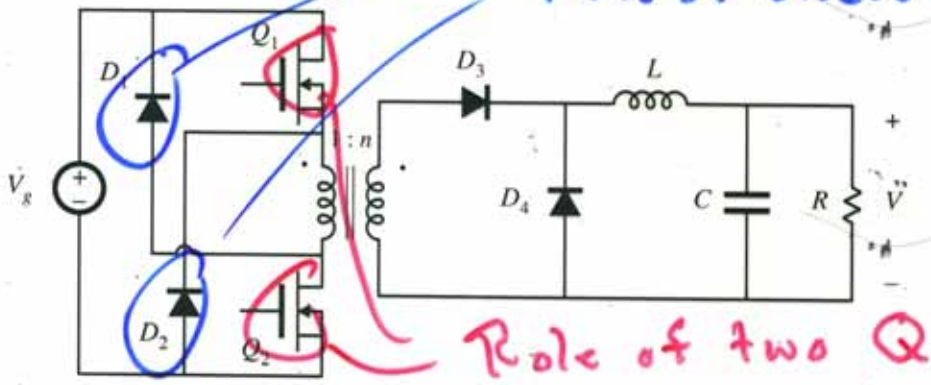
BUT $\frac{n_1}{n_2}\uparrow$ implies that the standoff voltage across the transistor increases since:

$V_{Tr}(off) = V_g[1 + \frac{n_1}{n_2}]$ So we trade off decreased Tr on time — heat issue ?

D_1 for increased voltage stress.
This transistor switch voltage stress may be too much for one transistor to work in its safe operating area (SOA). Below we show a way to solve this by utilizing two rather than one switch and dividing the switch stress between them.

Playing with $\frac{N_2}{N_1}$ Exceed V_{ds}^{max} $\Rightarrow$ heat Q

The two-transistor forward converter



$$V = nDV_g \qquad D \le \frac{1}{2} \qquad \max(v_{Q1}) = \max(v_{Q2}) = V_g$$

driving in this type of topology, designers should take care

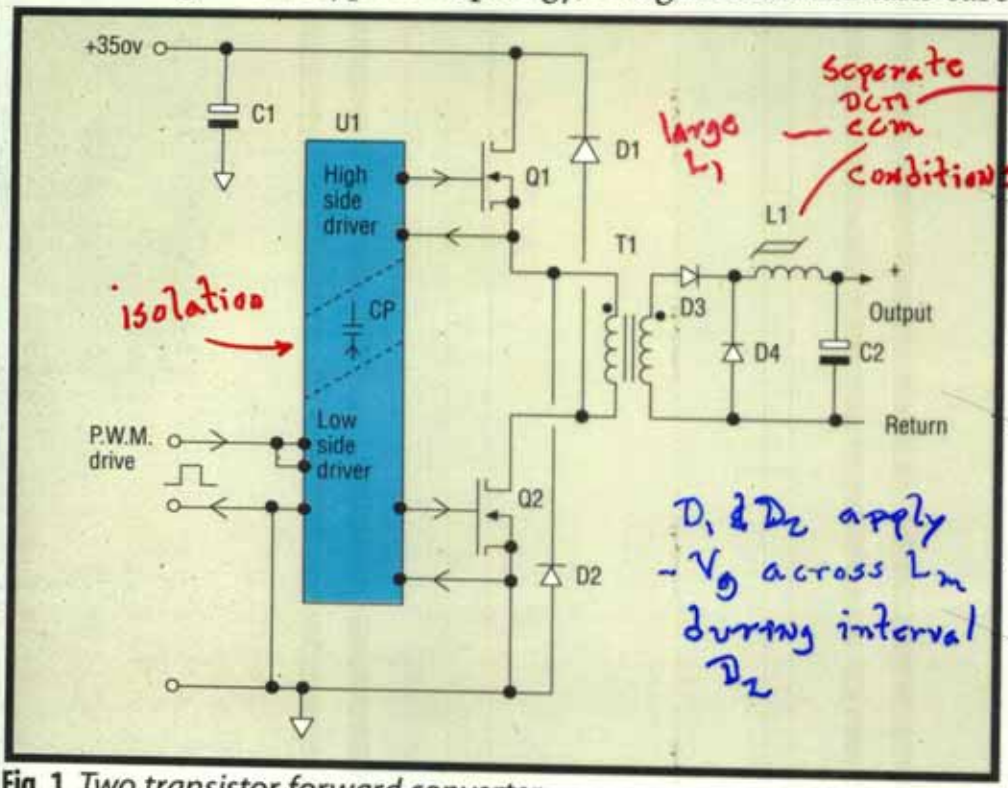
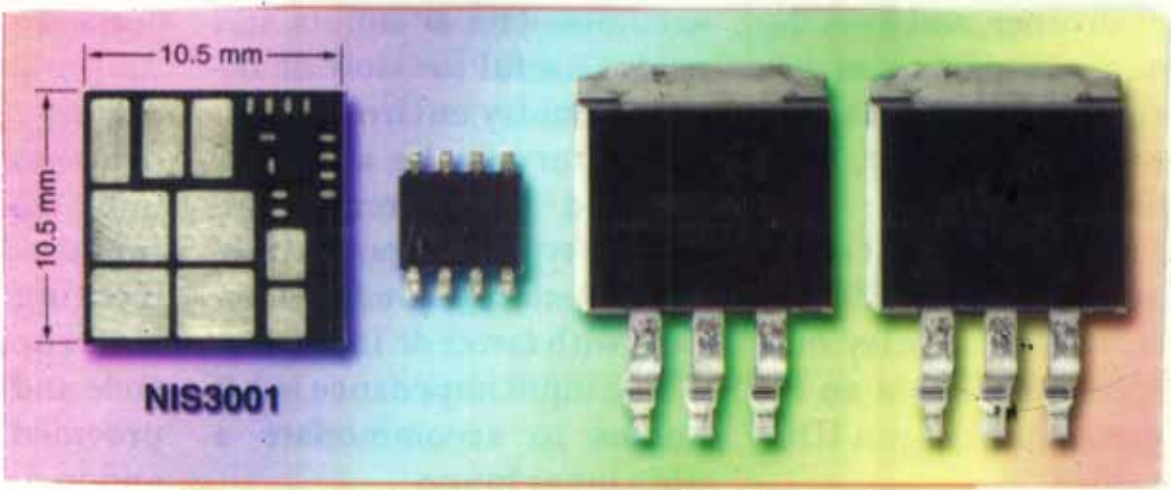


Fig. 1. *Two transistor forward converter.*



ON Semiconductor's 25-amp NIS3001 (left) is an integrated driver and MOSFET combination. It replaces three discrete components (shown at right).

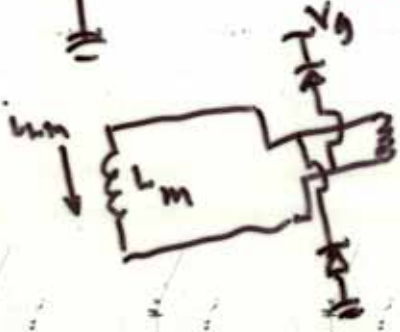
Role of diodes: D_1 & D_2

Clamps V_{lower} of primary to $+V_g$

no ringing

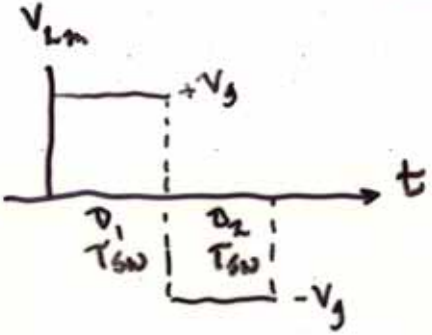
Clamps V_{upper} of primary to ground

No ringing



$-V_g$ placed on N_p

2Q Forward — CCM / DCM ← CAN guarantee?



$+V_g$ on primary for $D_1 T_{SW}$ ⇒ both diodes D_1, D_2 off

$-V_g$ on primary ⇒ diodes D_1, D_2 ON

$V_Q(max) = V_g + \text{diode drop}$

$+V_g$ on primary ⇒ $i_{primary}(ref) = \frac{I_{Load}}{n}$

lower i_{drain} than I_2

$n > 1$

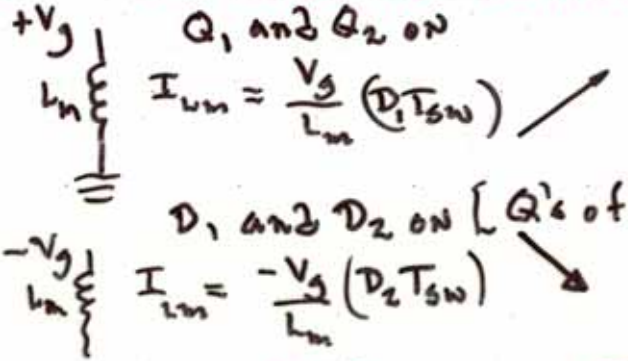
$n < 1$?

$i_g = i_{Prim} + i_{Lm}$

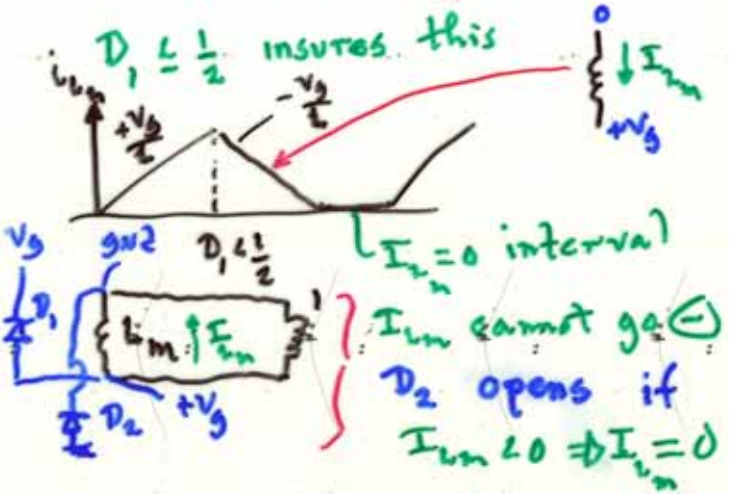
big Ω-wave

small Ω-wave due to big L_m

How to Guarantee L_m reset: DCM

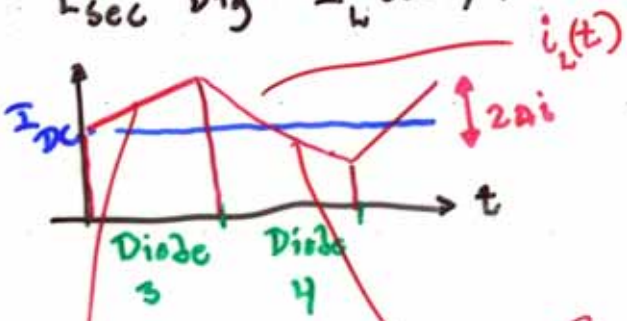


Reset insured if $i_{L_m} = 0$ over T_{SW}



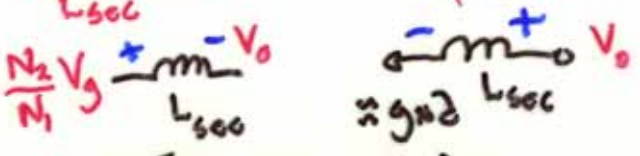
Secondary for CCM conditions

L_{sec} big $I_L^{Av}(sec) > \Delta i$



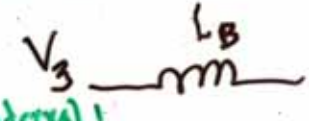
$\frac{V_L(sec) = ?}{L_{sec}}$

$\frac{V_L = ?}{L_{sec}}$



i_{sec} conditions Δi & $I_L^{Av}(sec)$

i_L (in buck inductor)



interval 1: $V_3 = \frac{n_3}{n_1} V_g$ — Q_{on}

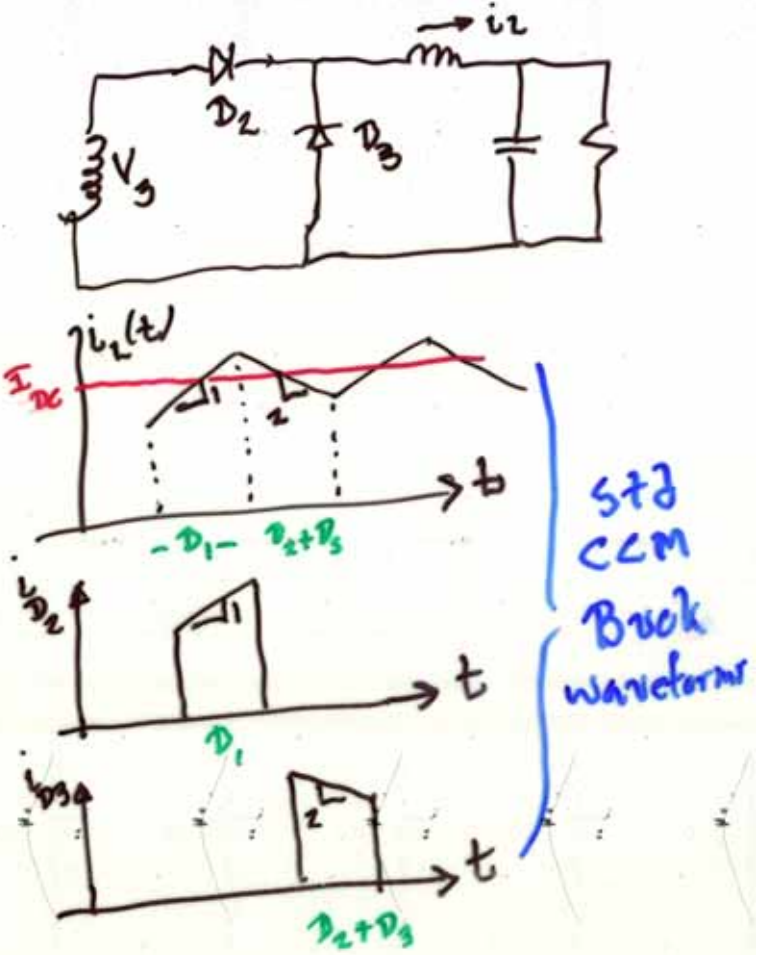
interval 2: $V_3 = 0$ — Q_{off} diode 2 off

interval 3: $V_3 = 0$ — Q_{off} diode 1 off, diode 3 on

$V_{out} \approx V_g$ goal

Slope 1: $\frac{\frac{n_3}{n_1} V_g - V_o}{L_B}$

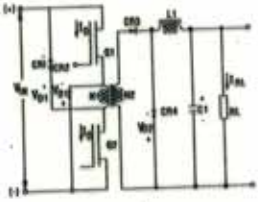
Slope 2: $\frac{-V_o}{L_B}$


i_2
D_2
D_3
V_g
$i_L(t)$
I_{DC}
1
2
t
$-D_1-$ D_2+D_3
i_{D_2}
t
D_1
i_{D_3}
2
t
D_2+D_3
Std CCM Buck waveforms

TYPE OF CONVERTER

Two-Switch Forward

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = \frac{N_2}{N_1}\left(\frac{t_{on}}{T_S}\right) = \frac{N_2}{N_1}(D)$$

PEAK DRAIN CURRENT •

$$I_{DMAX} = \frac{N_2}{N_1}\left(I_{RL} + \frac{\Delta I_{L1}}{2}\right) + \hat{I}_{MAG}$$

(I_{MAG} = Peak magnetizing current.)

PEAK DRAIN VOLTAGE •

(Q_1 or Q_2) $V_{DS} = V_{IN} + V_{D1}$

AVERAGE DIODE CURRENTS •

$$I_{CR1,AVE} = I_{CR2,AVE} = \frac{\hat{I}_{MAG}}{2} D$$

$$I_{CR3,AVE} = I_{RL} D$$

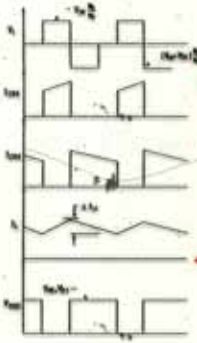
$$I_{CR4,AVE} = I_{RL}(1-D)$$

DIODE VOLTAGES (VRM) •

$$V_{CR1,PK} = V_{CR2,PK} = V_{IN}$$

$$V_{CR3} = V_{CR4} = \left(\frac{N_2}{N_1}\right) V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

Drain currents reduced by turns ratio. Lossless snubber recovers energy. Drain voltage 1/2 that of conventional forward converter. Low output ripple.

DISADVANTAGES

Poor transformer utilization, high parts count, high-side switch drive required. Transformer reset limits duty ratio. High input current ripple.

TYPICAL APPLICATIONS

High input voltage, moderate power. Supports multiple outputs.

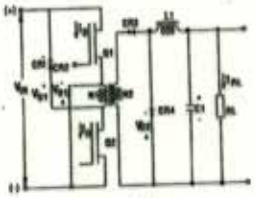
APPLICABLE HARRIS PRODUCTS

HIP2500, HV400

TYPE OF CONVERTER

Two-Switch Forward

CIRCUIT CONFIGURATION



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($\hat{I}_{MAG}$ = Peak magnetizing current.)

PEAK DRAIN VOLTAGE

- (Q_1 or Q_2) $V_{DS} = V_{IN} + V_{D1}$

AVERAGE DIODE CURRENTS

- $I_{CR1,AVE} = I_{CR2,AVE} = \frac{\hat{I}_{MAG}}{2} D$

$$I_{CR3,AVE} = I_{RL} D$$

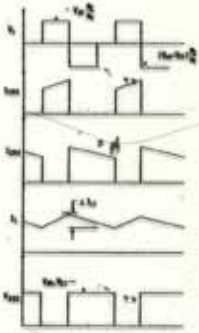
$$I_{CR4,AVE} = I_{RL}(1-D)$$

DIODE VOLTAGES (VRM)

$$V_{CR1,PK} = V_{CR2,PK} = V_{IN}$$

$$V_{CR3} = V_{CR4} = \left(\frac{N_2}{N_1}\right) V_{IN}$$

VOLTAGE AND CURRENT WAVEFORMS



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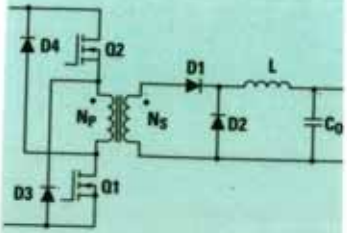
HIP2500, HV400



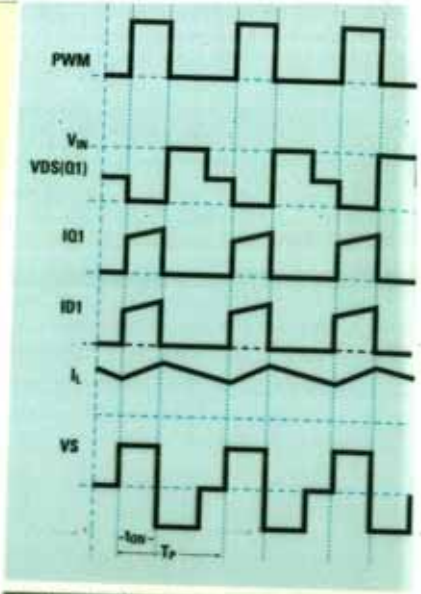
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{N_S}{N_P}\right) \times \left(\frac{t_{ON}}{T_P}\right) = \left(\frac{N_S}{N_P}\right) \times D$$

$$I_{Q1}\,(max) = \left(\frac{N_S}{N_P}\right) \times I_{OUT}$$

$$VDS = V_{IN}$$

$$I_{D1} = I_{OUT} \times D$$

$$V_{D1} = V_{OUT} + V_{IN} \times \left(\frac{N_S}{N_P}\right)$$



Application Notes:**	
150-W Off-Line Forward Converter Design Review	(SEM400)
Practical Considerations in Current Mode Power Supplies	(SLUA110)

Controllers:	
UCC35701	UCC28220
UCC3800	UCC3809-1
UCC38C42	UCC2891

Forward Converter

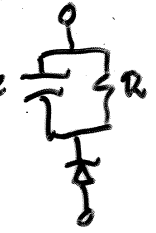
$D \leq 1/2$ restriction

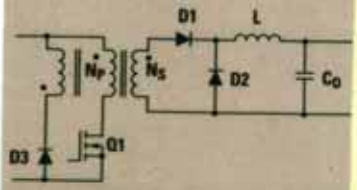
avoided by

R-C-diode circuit

to

eliminate "reset coil"





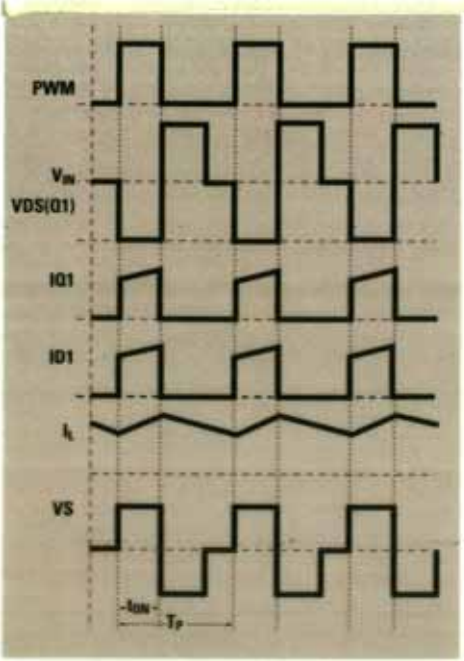
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{N_S}{N_P}\right) \times \left(\frac{t_{ON}}{T_P}\right) = \left(\frac{N_S}{N_P}\right) \times D$$

$$I_{Q1}\,(max) = \left(\frac{N_S}{N_P}\right) \times I_{OUT}$$

$$VDS = 2 \times V_{IN}$$

$$I_{D1} = I_{OUT} \times D$$

$$V_{D1} = V_{OUT} + V_{IN} \times \left(\frac{N_S}{N_P}\right)$$



Application Notes:**	
25-W Forward Converter Design Review	(SLUA276)
Multiple Output Forward Converter Design	(SEM1200)
Controllers:	
UCC35701	UCC28220
UCC3800	UCC3809-1
UCC38C42	UCC2891

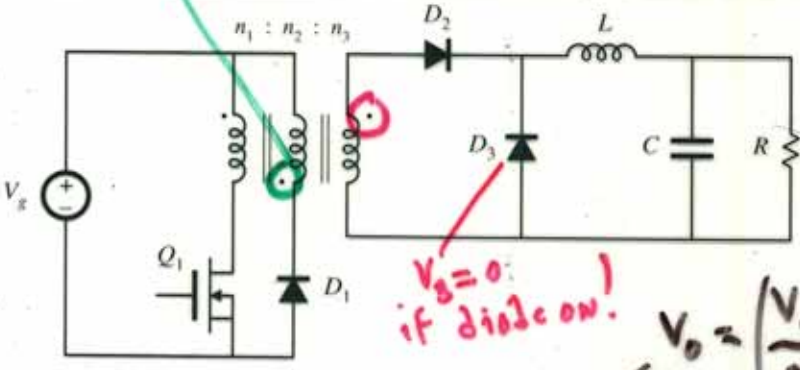
note dot on reset coil

Pg 154-159

6.3.2. Forward converter

with diode reset coil

HW Prob 6.11



$V_3 = 0$ if diode on!

$$V = \left(\frac{V_2}{N_1} N_3\right) D_{on}$$

- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited ← D_{on} too big: saturation of L_m
- Transformer is reset while transistor is off ← N_2 D_1 Clever

Fig 6.22 p154

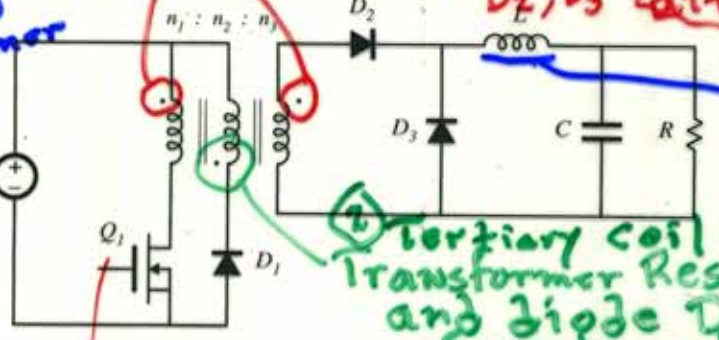
(1) DCM mode guarantees Trt reset

(1) Buck with n_3/n_1 transformer and attitude

6.3.2. Forward converter

(1) Forward Dots / diodes D_2, D_3

(2) 3 winding transformer is Key to Core reset (4)



(3) CCM or DCM mode ~ L

(4) Tertiary coil i n_3 Transformer Reset "dot" and diode D_3 smart reset due to dots/diodes

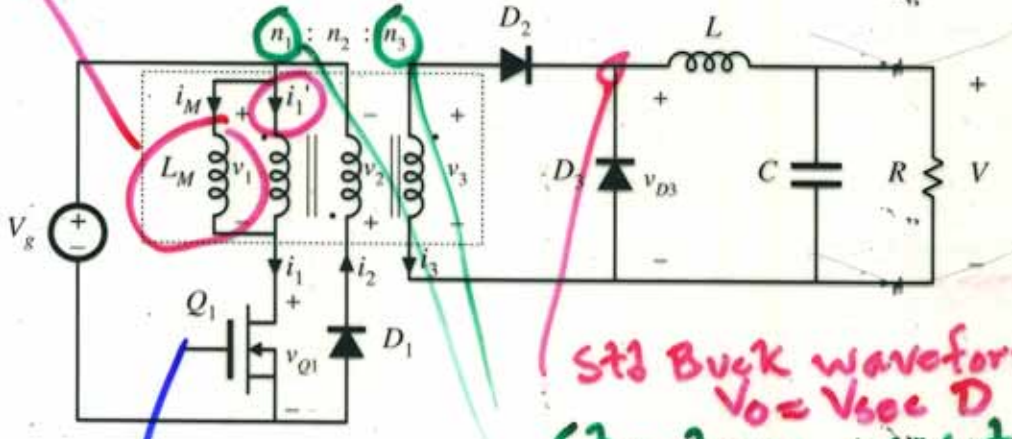
- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited ← insures i_m goes dry if $t(Q_{ON})$ is small
- Transformer is reset while transistor is off

Limited duration of "D" for DCM

Crucial

Focus on L_m of Trf & $\pm V_{in}$ / L_m

Forward converter with transformer equivalent circuit

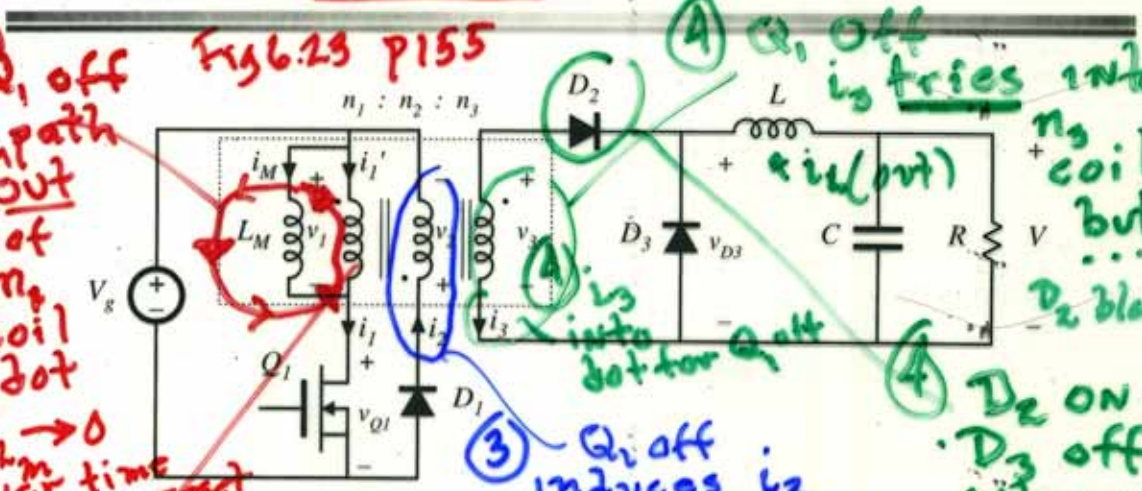


Std Buck waveform
$V_0 = V_{sec} D$
Step down assist
$\frac{n_2}{n_1}$

limited duty cycle to avoid saturation

(1) Reset: To fathom n_2 & D_1 (diode) then Q_1 switches off
Consider Q_1 was ON

Forward converter
with transformer equivalent circuit



(2) Q_1 off
in path
out
of
n_3
coil
dot
$i_{n_3} \rightarrow 0$
over time
to ensure reset

(4) Q_1 off
i_3 tries into
n_3 coil
but ...
D_2 block

i_3 into dot for Q_1 off

(4) D_2 ON
D_3 off
when
Q_1 ON

(3) Q_1 off induces i_2 into n_2 coil
Note i_2 direction

(5) $V_1 = ?$ 0

V (across n_2) = ?

Reset on coil n_2
Always V_g if
D_1 is ON $V_1 = ?$

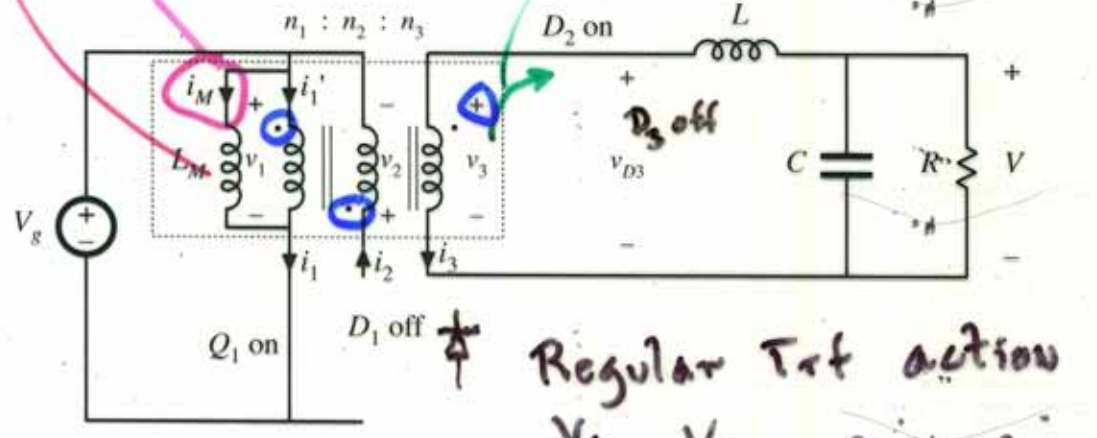
Only coil #1 Has L_m

$D_1 T_{sw}$ has Q_1 ON ⇒ D_1 off, D_2 ON, D_3 off

Subinterval 1: transistor conducts

rises while Q_1 ON

load current out dot

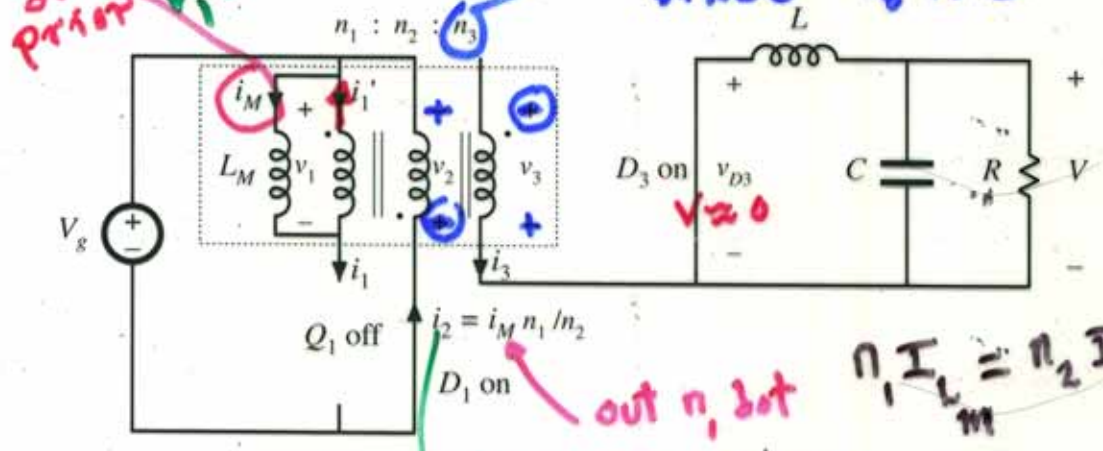


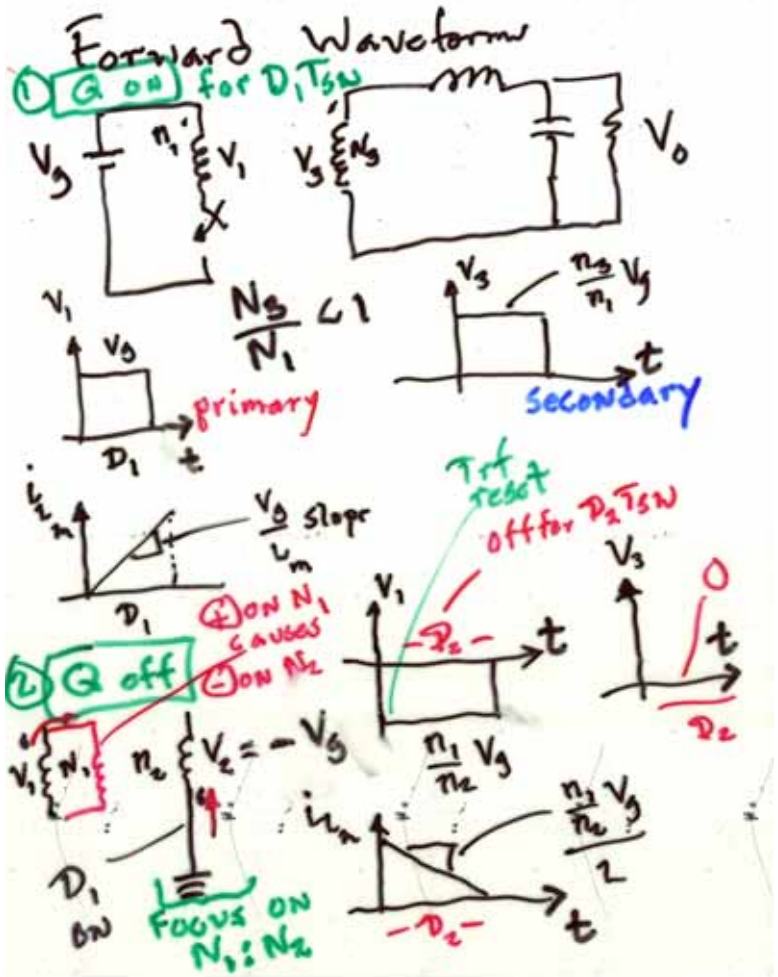
Regular Tx action

$$\frac{v_2}{n_1} = \frac{v_3}{n_3}, \quad n_1 i_1' = n_3 i_3$$

dots

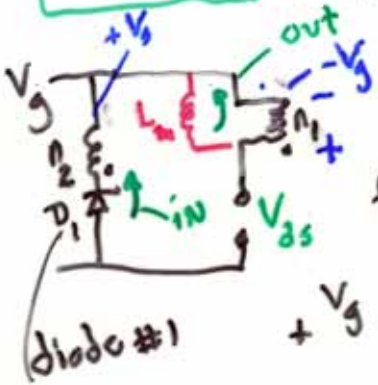
Subinterval 2: transformer reset




Forward Waveforms
1 Q on for $D_1 T_{SW}$
V_g
n_1
V_1
V_3
N_3
V_0
V_1
V_0
primary
D_1
t
$\frac{N_3}{N_1} < 1$
V_3
$\frac{n_3}{n_1} V_g$
t
secondary
i_{L_m}
$\frac{V_g}{L_m}$ slope
D_1
+ on N_1 causes
- on N_2
2 Q off
V_1
N_1
n_2
$V_2 = -V_g$
D_1 on
focus on $N_1 : N_2$
T_{rst} reset
off for $D_2 T_{SW}$
V_1
$-D_2-$
t
$\frac{n_1}{n_2} V_g$
V_3
0
t
D_2
i_{L_m}
$\frac{n_1}{n_2} V_g$
2
$-D_2-$
t

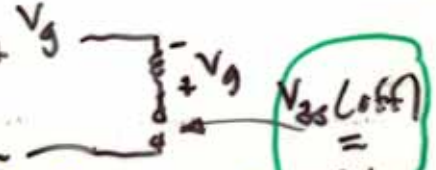
Switch Stress Q off D_1 ON

FET off: $V_{DS}(off) = ?$



$\frac{V_g}{n_1} = \frac{V_2}{n_2}$ Could vary

for $n_1 = n_2$



easy fix?

Diode #2 Diode off D_2 in secondary

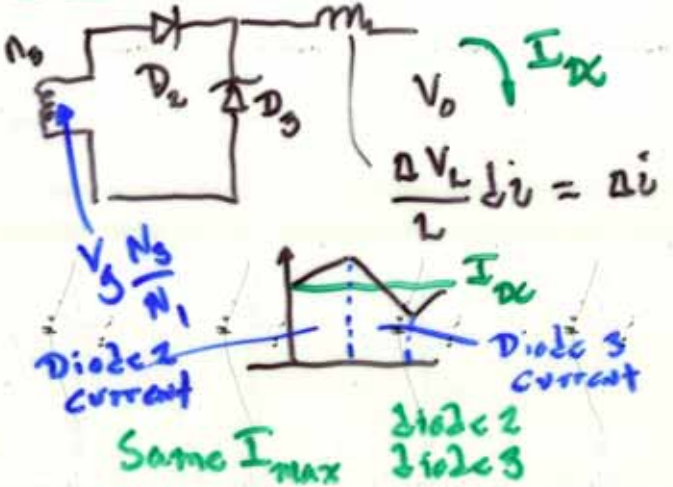
$V_D(off) = V_o + V_g \frac{N_3}{N_1}$

Max I(FET): Q on, N_1 coil open, N_3 coil active

$$N_1 I_Q = N_3 I_{out}$$

$$I_Q = \frac{N_3}{N_1} I_{out}$$

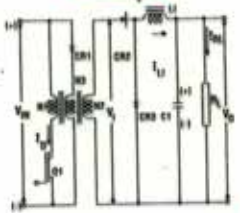
Secondary Diodes: I_{max}



TYPE OF CONVERTER

Forward

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = \frac{N_2}{N_1}\left(\frac{t_{on}}{T_S}\right) = \frac{N_2}{N_1}(D)$$

PEAK DRAIN CURRENT

$$I_{DMAX} = \frac{N_2}{N_1}\left(I_{RL} + \frac{\Delta I_L}{2}\right) + I_{MAG}$$

(I_{MAG} = I_{Peak} magnetizing current.)

PEAK DRAIN VOLTAGE

$$V_{DS} = V_{IN}\left(1 + \frac{N_1}{N_3}\right)$$

AVERAGE DIODE CURRENTS

$$I_{CR1} = \frac{I_{MAG}}{2}(D)$$

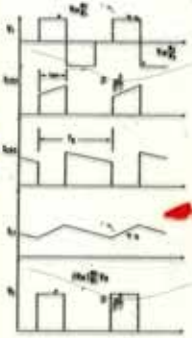
$$I_{CR2} = I_{RL}(D)$$

$$I_{CR3} = I_{RL}(1-D)$$

DIODE VOLTAGES (VRM)

$$V_{RM}\begin{cases} V_{CR1} = V_{IN}\left(1 + \frac{N_3}{N_1}\right) \\ V_{CR2} = V_{IN}\left(\frac{N_2}{N_3}\right) \\ V_{CR3} = V_{IN}\left(\frac{N_2}{N_1}\right) \end{cases}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

Drain current reduced by ratio of N_2/N_1. Low output ripple.

DISADVANTAGES

Poor transformer utilization. Poor transient response. Transformer design is critical. Transformer reset limits duty ratio. High voltage required for Q1. High input current ripple.

TYPICAL APPLICATIONS

Low-to-moderate output power. Supports multiple outputs.

APPLICABLE HARRIS PRODUCTS

HIP5061, ICL7667, HV400

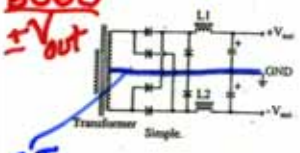
Variations on Forward

1.15 my notes

V_2 & V_1

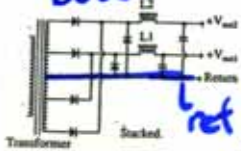
BOGO

$-V_{out}$



C.T.

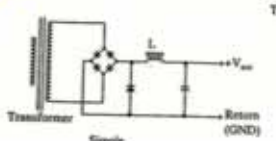
BOGO

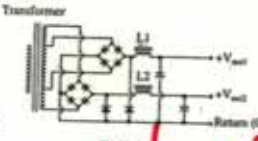


ret

Center tap V_1, V_2 forward

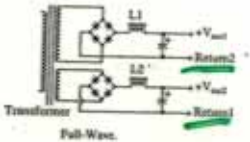
(a)

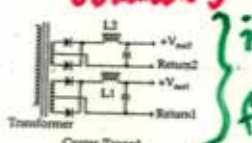




full wave forward

(b) Common gnd





isolated F.W forwards

(c)

Forward-mode secondary winding arrangements: (a) center-tapped secondaries; (b) full-wave secondaries; (c) isolated secondaries.

On the next page we will outline the voltage and current waveforms in a simple half-wave forward converter to give a clear picture of the unipolar drive that occurs in each portion of the transformer secondary that is synchronous with the primary drive sequence. In full wave center tapped operation each half of the transformer sees similar waveforms. The full wave rectification in the secondary insures that the current waveforms are unipolar as does half-wave rectification.

Operation and Benefits of Active-Clamp Forward Power Converters

— Bob Bell, Power Applications Engineer

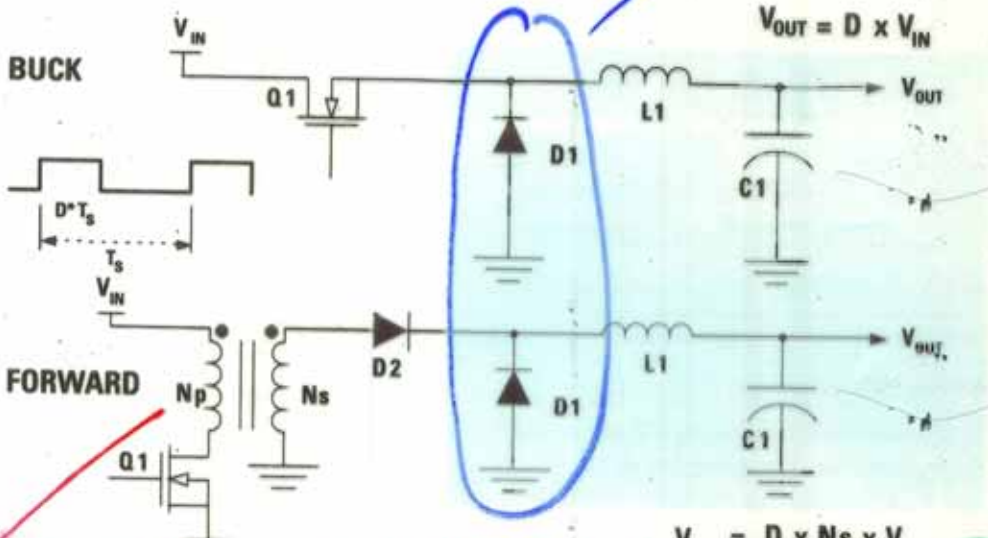
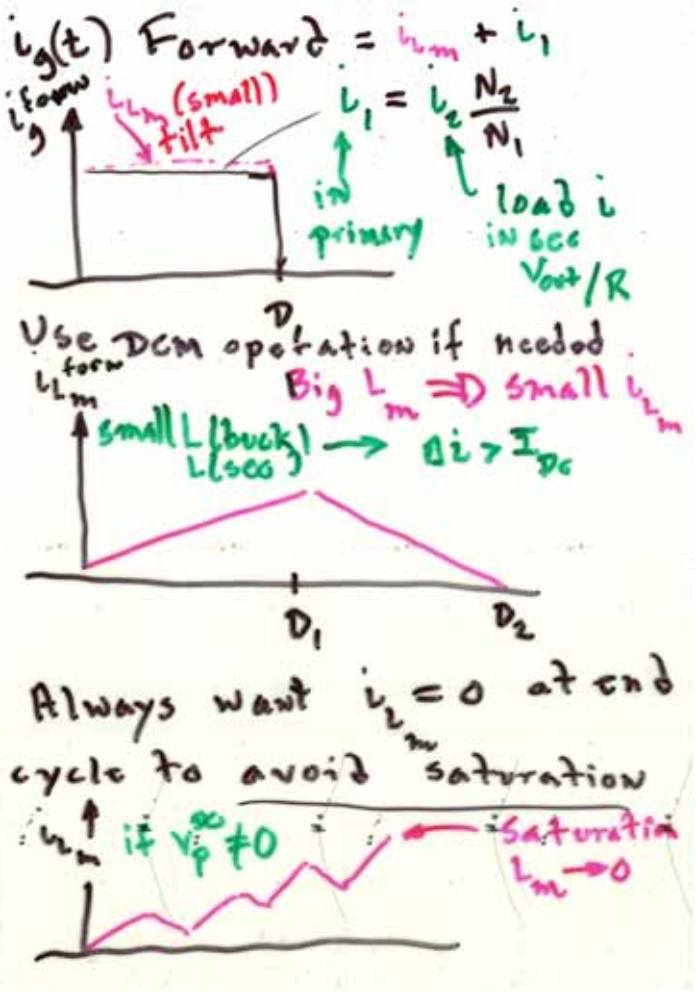


Figure 1. Buck and Forward Topologies


$i_g(t)$ Forward = i_{L_m} + i_1
$i_{forward}$
i_{L_m} (small) tilt
$i_1 = i_2 \frac{N_2}{N_1}$
in primary
load i in sec
V_{out}/R
D
Use DCM operation if needed
i_{L_m} forward
Big L_m ⇒ small i_{L_m}
small L (buck) L (sec) → $\Delta i > I_{DC}$
D_1
D_2
Always want $i_{L_m} = 0$ at end of cycle to avoid saturation
i_{L_m}
if $V_p^{sec} \neq 0$
saturation
$L_m \to 0$

How Guarantee No saturation of L_m even for CCM?

L_m $\begin{matrix} + & - \\ - & + \end{matrix}$

Add another primary winding

Key → but make it provide $-V_{in}$

extra coil { - opposite dot convention
to Apply $(-)V_{in}$ across L_m

Case #1 Q_1 ON D_1 off

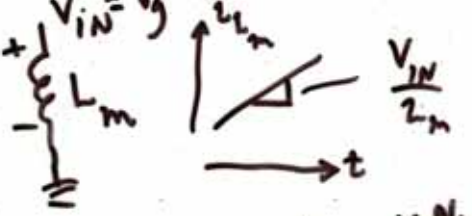
Case #2 Q_1 off D_1 ON

OK? {
$i_2 = i_{L_m}$ (when Q_1 off) $\frac{n_1}{n_2}$
i_2 flows until $i_{L_m} \to 0$

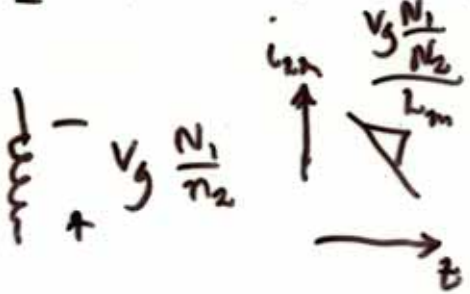
When D_1 ON $\frac{V_g}{N_2} = \frac{V_{L_m}}{N_1}$

$V_{Lm} = \frac{N_1}{N_2} V_g$ for reset is $(-)$

Q_1 ON



Q_2 off



Goal is to insure i_{L_m} resets to zero

$$\frac{V_{IN}}{L_m} T_{ON}(Q) = \frac{V_{IN}}{L_m} \frac{N_1}{N_2} T_{off}(Q_2)$$

Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

Choices

which can be increased by increasing the turns ratio n_2 / n_1. But this increases the peak transistor voltage:

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

Consequences

For $n_1 = n_2$

$$D \leq \frac{1}{2} \quad \text{and} \quad \max(v_{Q1}) = 2V_g$$

$n_1 = n_2$ $V_{max} = 2V_g$

Maximum duty cycle vs. transistor voltage stress

$\frac{N_2}{N_1}$ ↑ D ↑

$\frac{N_2}{N_1}$ ↑ D ↓ ↓ downside effects

1. Maximum duty cycle limited to

$$D \le \frac{1}{1 + \frac{n_2}{n_1}}$$

which can be decreased by increasing the turns ratio n_2 / n_1. But this increases the peak transistor voltage:

$$\max v_{Q1} = V_g \left(1 + \frac{n_1}{n_2}\right)$$

V across Q_1 (off) is 2 V_g for $n_1 = n_2$

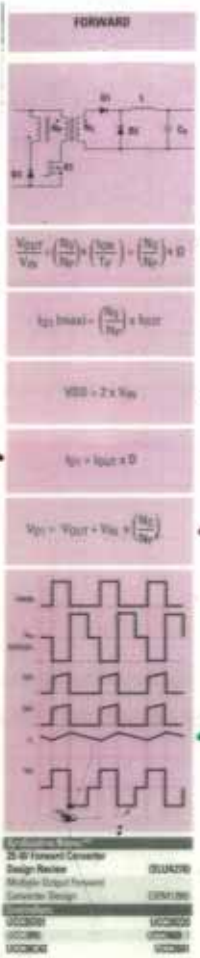
2. For $n_1 = n_2$ ← Easy to achieve $i_{L_m} \to 0$

$$D \le \frac{1}{2} \quad \text{and} \quad \max v_{Q1} = 2V_g$$

Max V stress

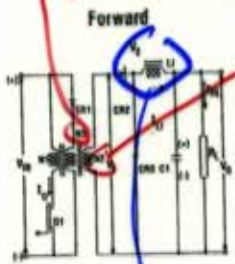
$n_2 = 3n_1$

D ≤ 1/4


FORWARD
trade Cu vs. Si
Ns/Np ↓
Ia ↑
FET Voff
Np = Ns
D, only ON for DTsw
diode Voff
Buck iL

TYPE OF CONVERTER

CIRCUIT CONFIGURATION



IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = \frac{N_2}{N_1}\left(\frac{t_{on}}{T_S}\right) = \frac{N_2}{N_1}(D)$$

PEAK DRAIN CURRENT

$$I_{DMAX} = \frac{N_2}{N_1}\left(I_{RL} + \frac{\Delta I_L}{2}\right) + I_{MAG}$$

(I_{MAG} = Peak magnetizing current.)

PEAK DRAIN VOLTAGE

$$V_{DS} = V_{IN}\left(1 + \frac{N_1}{N_3}\right)$$

AVERAGE DIODE CURRENTS

$$I_{CR1} = \frac{I_{MAG}}{2}(D)$$

$$I_{CR2} = I_{RL}(D)$$

$$I_{CR3} = I_{RL}(1\text{-}D)$$

DIODE VOLTAGES (VRM)

$$V_{RM}\begin{cases} V_{CR1} = V_{IN}\left(1 + \frac{N_3}{N_1}\right) \\ V_{CR2} = V_{IN}\left(\frac{N_2}{N_3}\right) \\ V_{CR3} = V_{IN}\left(\frac{N_2}{N_1}\right) \end{cases}$$

VOLTAGE AND CURRENT WAVEFORMS

ADVANTAGES

Drain current reduced by ratio of N_2/N_1. Low output ripple.

DISADVANTAGES

Poor transformer utilization. Poor transient response. Transformer design is critical. Transformer reset limits duty ratio. High voltage required for Q1. High input current ripple.

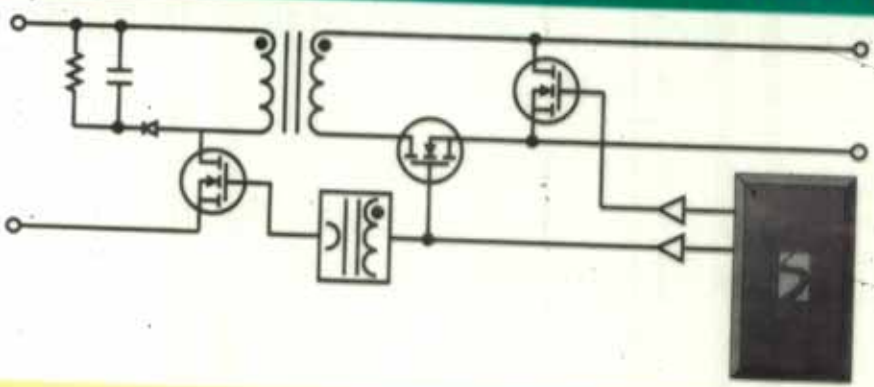
TYPICAL APPLICATIONS

Low-to-moderate output power. Supports multiple outputs.

APPLICABLE HARRIS PRODUCTS

HIP5051, ICL7667, HV400

SC4910 Single-Stage PWM Controller

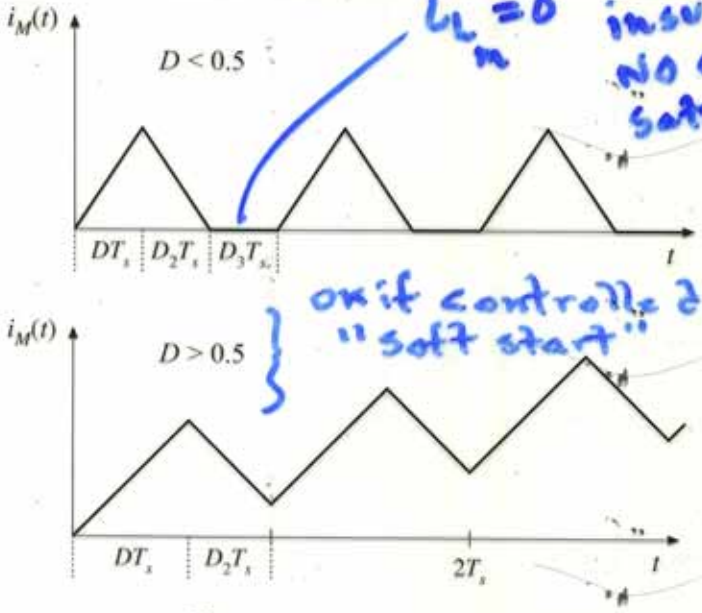


The SC4910 is the industry's first secondary-side, single-stage, low output voltage power supply controller. Features include:

- **single-stage power conversion for higher efficiency**
- **multiphase isolated topologies reduce filtering needs**
- **load sharing for N+1 redundant systems**
- **synchronous rectification minimizes switching losses**
- **0.75V reference for sub-1V solutions**
- **current or voltage-mode operation**

What happens when $D > 0.5$

magnetizing current waveforms, for $n_1 = n_2$



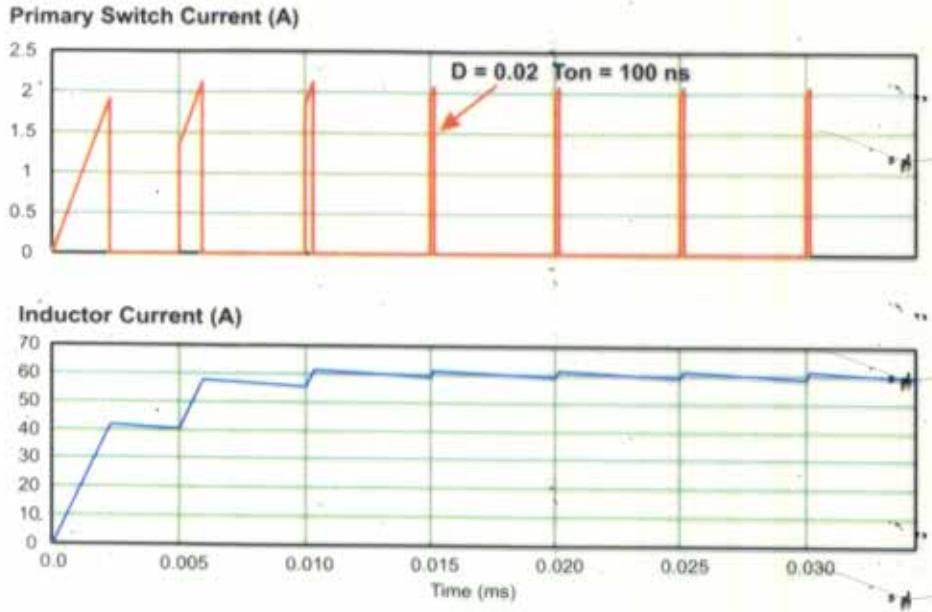


Figure 2 : Switch current and inductor current for the forward converter. Input voltage = 425 VDC, output load = short circuit, soft-start disabled. After 4th pulse, duty cycle must cut back to 2%, or control of the peak current is lost.

Q on time D_2 '15 for $n_2 = 4n_1$, Price you pay for $\frac{n_2}{n_1}$?

Transformer reset

(Requires DCM to "ensure" trf. reset)

From magnetizing current volt-second balance:

$$\langle v_1 \rangle = D(V_g) + D_2(-V_g n_1/n_2) + D_3(0) = 0$$

Solve for D_2:

(1) $$D_2 = \frac{n_2}{n_1} D$$ ← For guaranteed V-sec balance we need D_2 AND limit size of D_1

D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

(2) $$D_3 = 1 - D - D_2 \geq 0$$ for dcm interval to occur!

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0$$

The requirement $i \to 0 \Rightarrow$ limited first interval duration

Solve for D

(3) limit on D_1: $$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

(4) for $n_1 = n_2$: $D \leq \frac{1}{2}$ insures i_2 goes "dry" during interval 2 $\Rightarrow$ Successful Reset

(5) V_Q stress? $n_2 = 4n_1$? D_2?

Forward Converter
Active Clamp Reset
via Two FET's / two body diodes

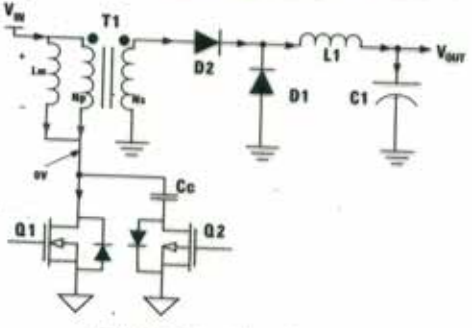


Figure 3a. Operation at Step t0

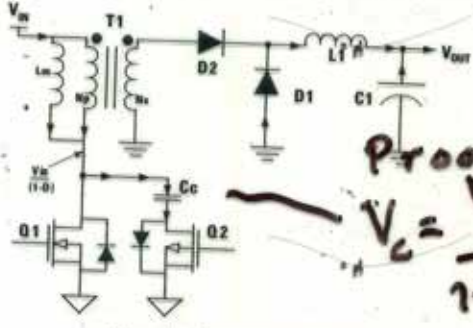


Figure 3b. Operation at Step t1

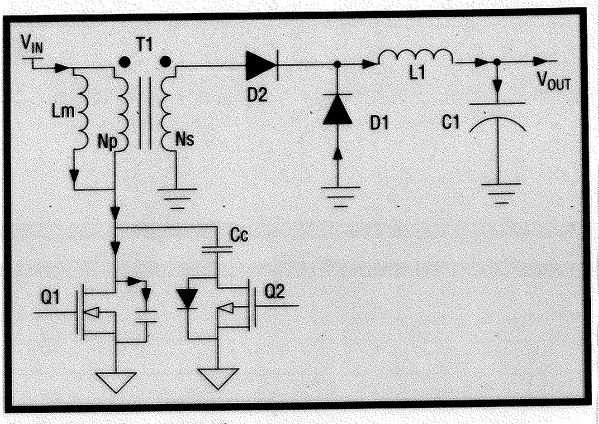


Fig. 3b. *Operation at step t1.*

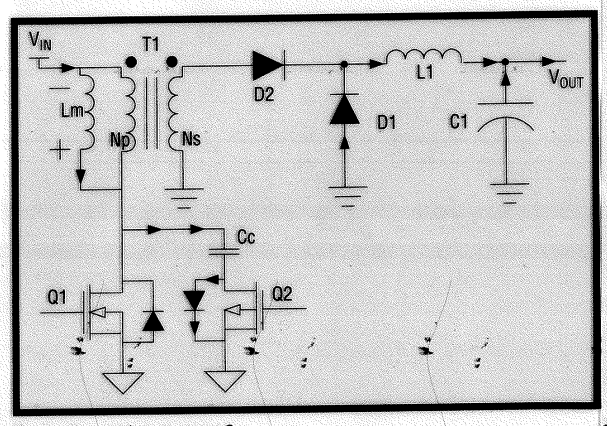


Fig. 3c. *Operation at step t2.*

time, the voltage across the transformer primary is re-

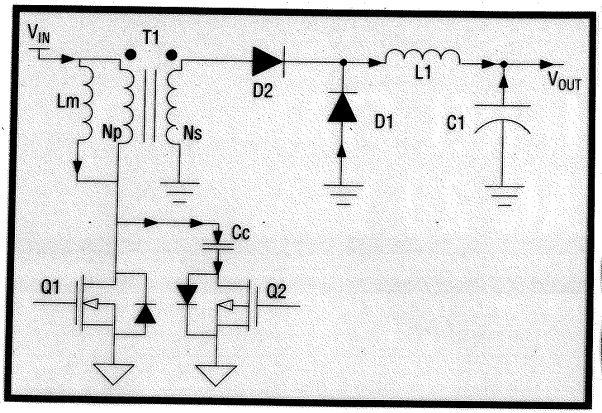


Fig. 3d. *Operation at step t3.*

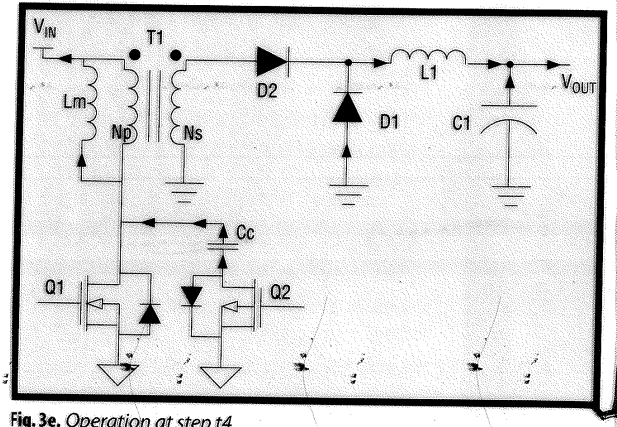


Fig. 3e. *Operation at step t4.*

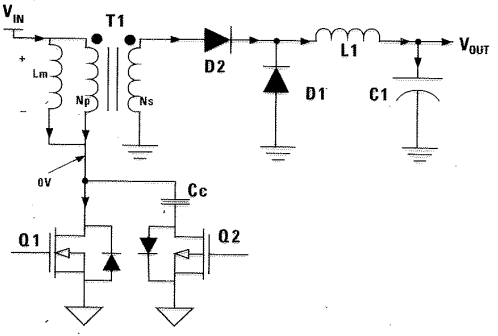


Figure 3a. Operation at Step t0

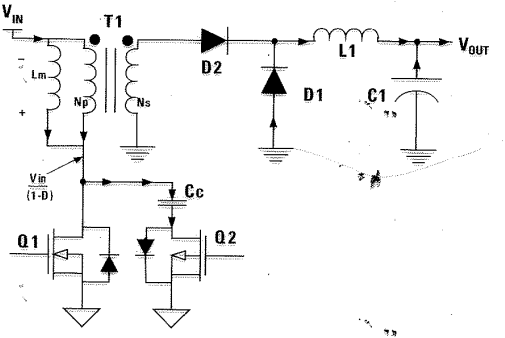


Figure 3b. Operation at Step t1

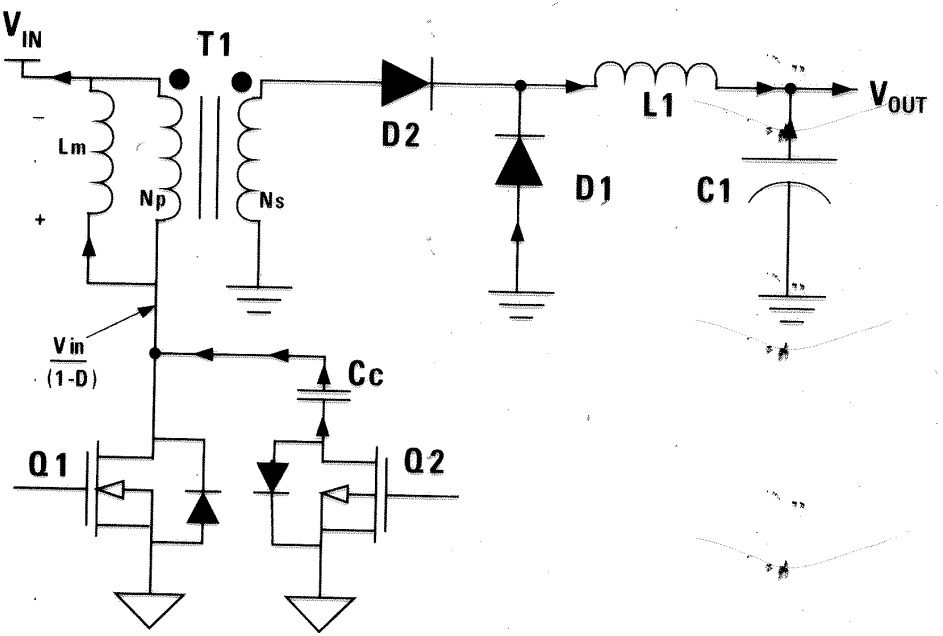


Figure 3c. Operation at Step t2

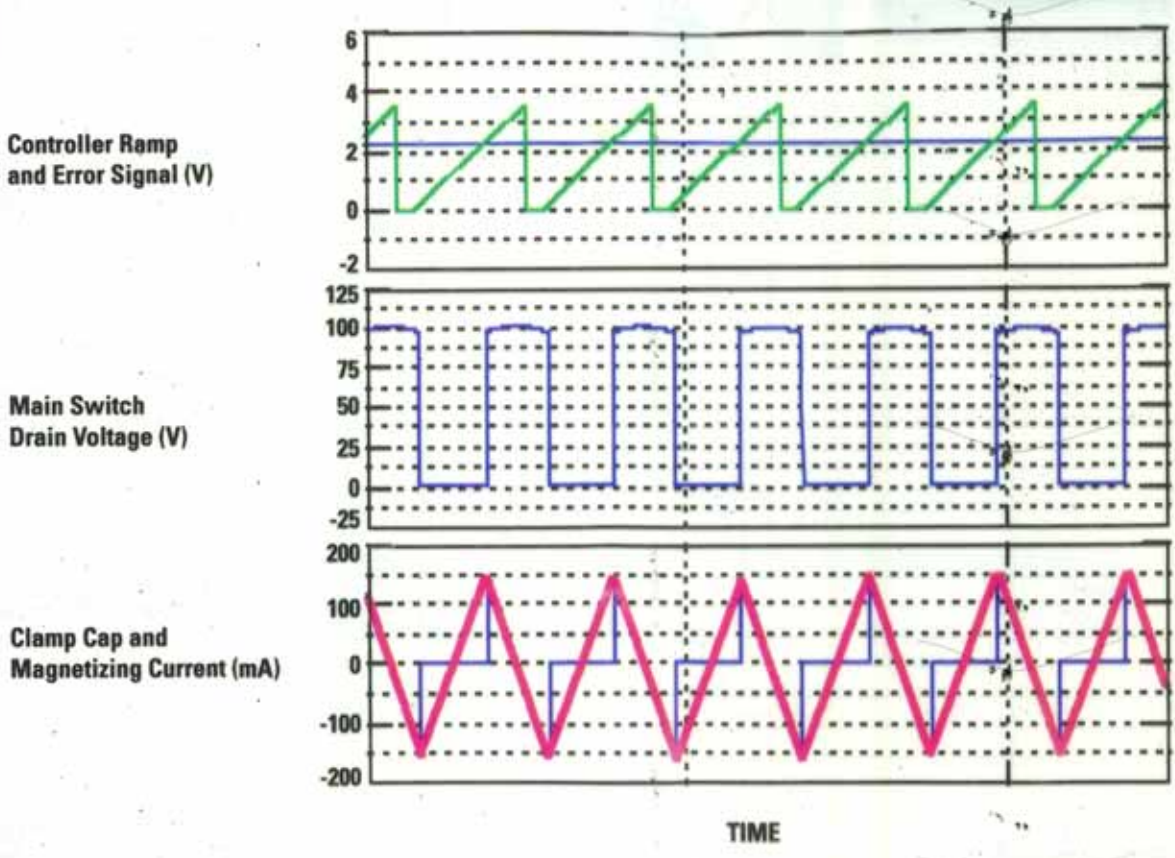


Figure 4. Key Active-Clamp Waveforms

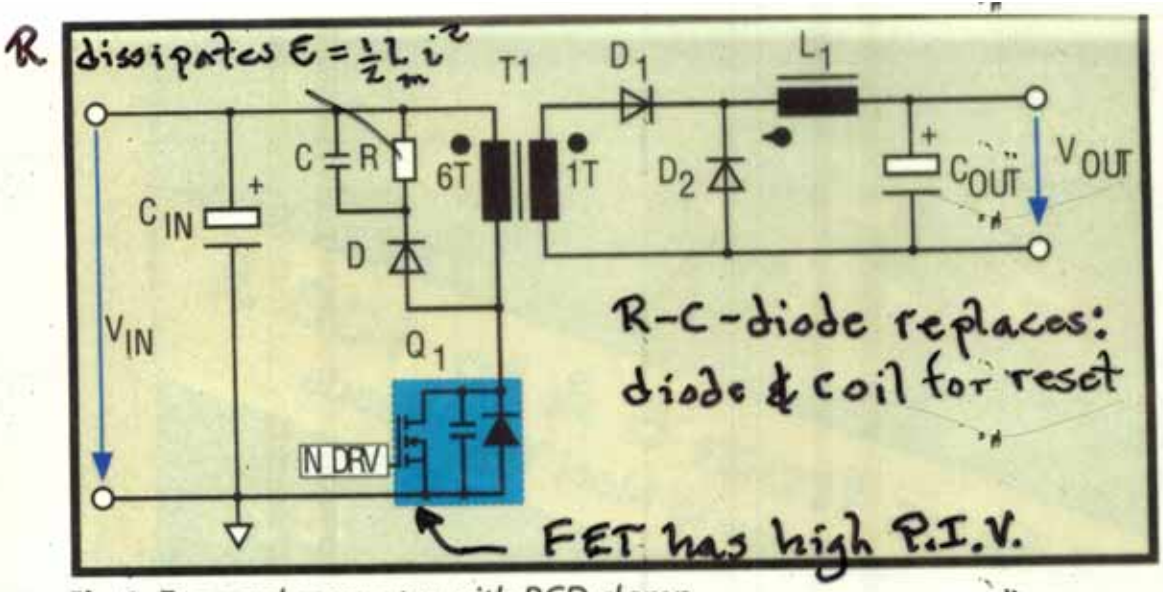


Fig. 1. *Forward converter with RCD clamp.*

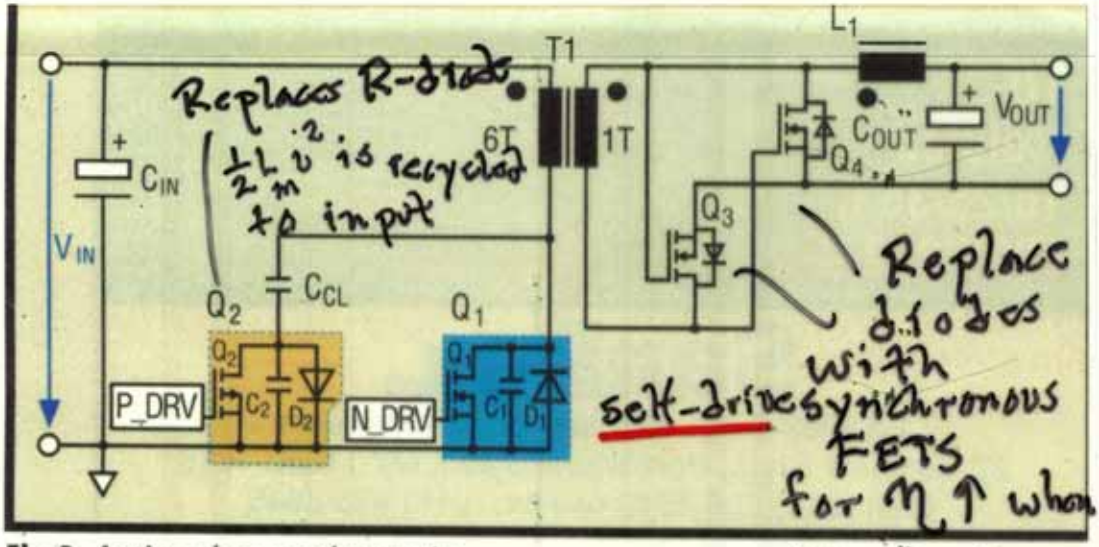


Fig. 2. *Active clamp schematic.*

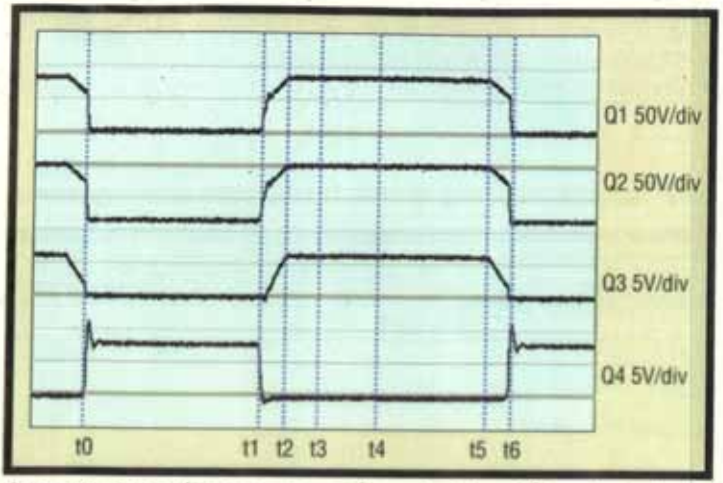


Fig. 3. *MOSFET Drain to source waveforms for Q_1 and Q_2 on the primary and Q_3 and Q_4 on the secondary side.*

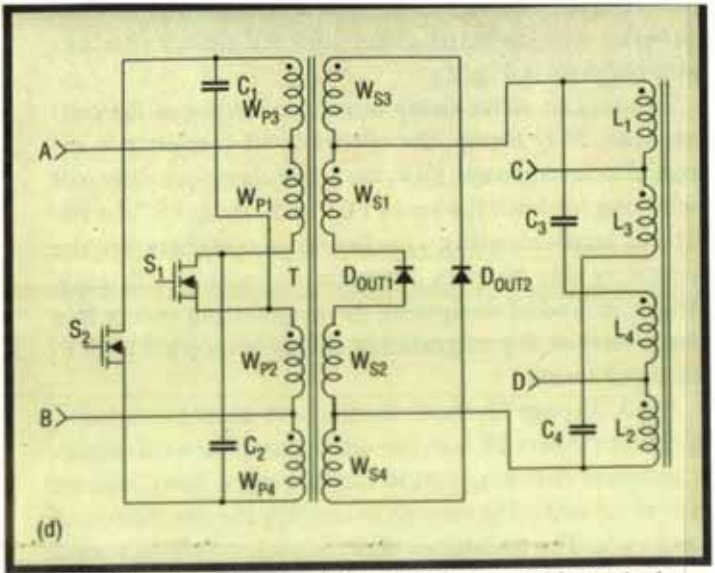


Fig. 4. (d) *Fully balanced push-pull forward converter with terminal ripple current cancellation.*

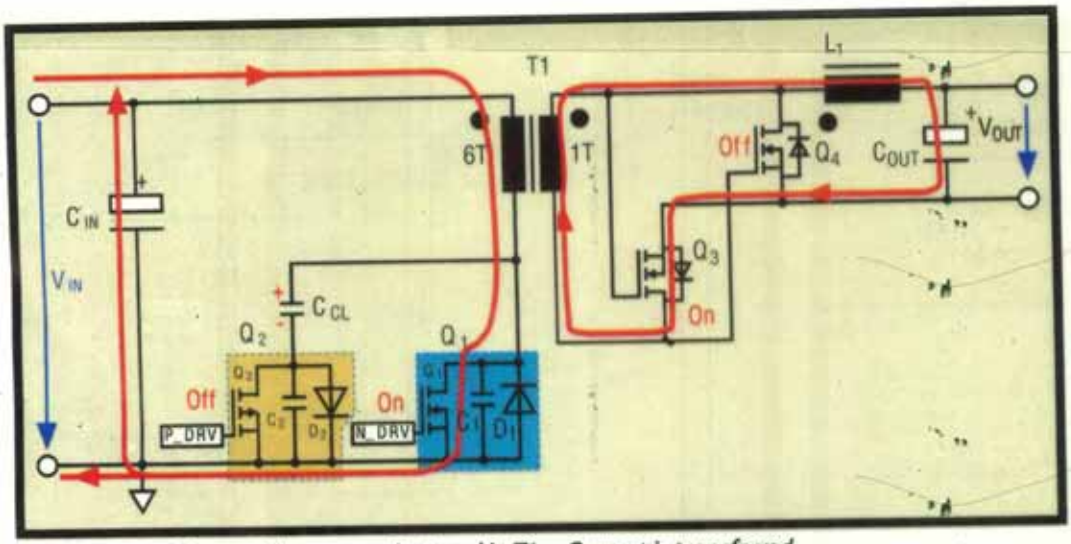


Fig. 4. t_0 -> t_1—*Magnetizing energy is stored in T1—Current is transferred.*

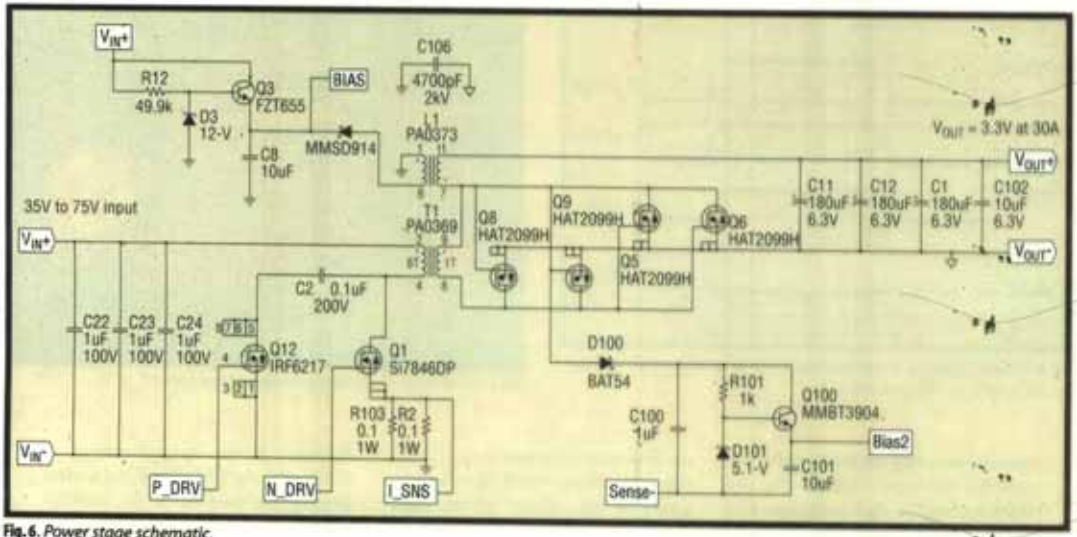


Fig. 6. *Power stage schematic.*

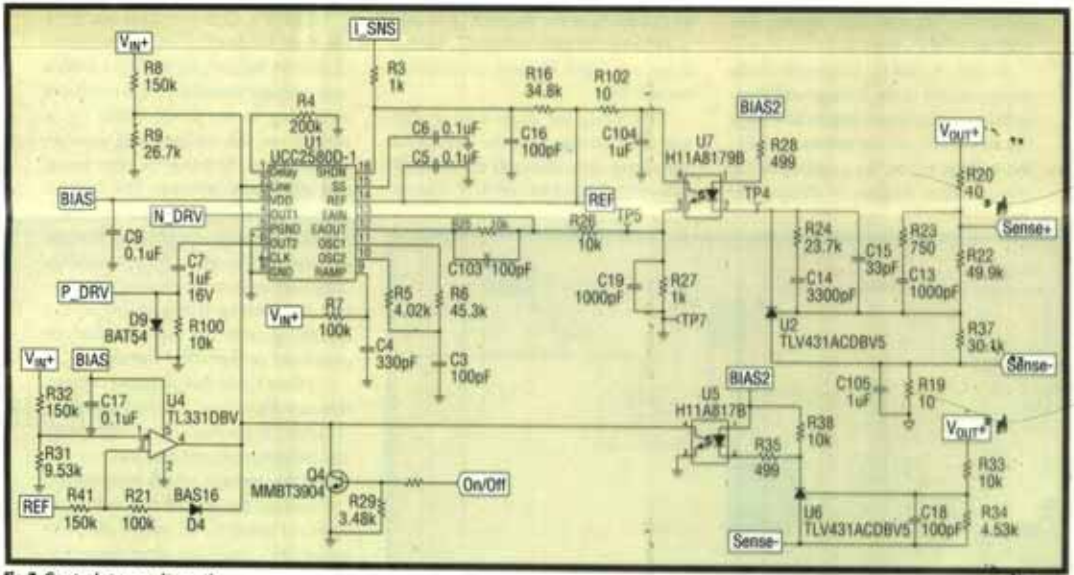
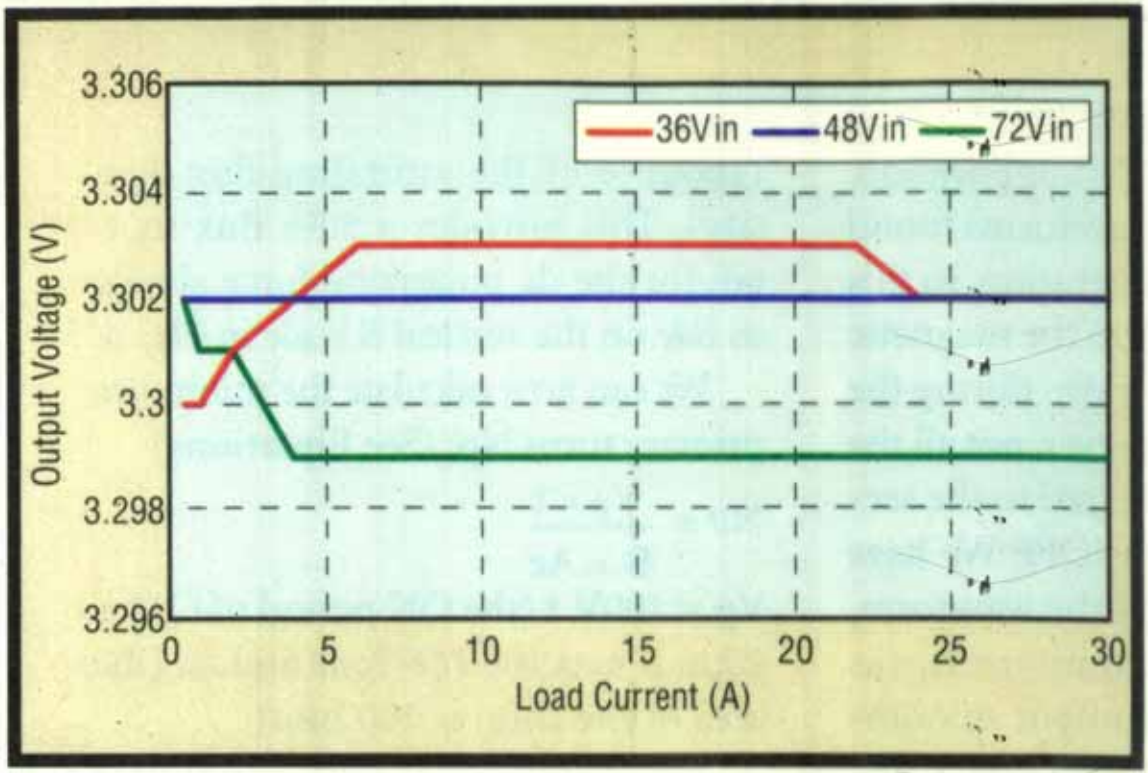
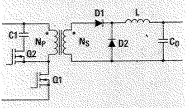


Fig. 7. *Control stage schematic.*


3.306
3.304
3.302
3.3
3.298
3.296
Output Voltage (V)
36Vin
48Vin
72Vin
0
5
10
15
20
25
30
Load Current (A)

ACTIVE CLAMP FORWARD



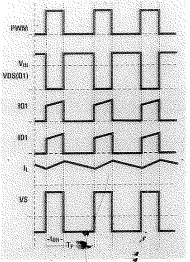
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{N_S}{N_P}\right) \times \left(\frac{t_{ON}}{T_P}\right) = \left(\frac{N_S}{N_P}\right) \times D$$

$$I_{Q1}\,(max) = \left(\frac{N_S}{N_P}\right) \times I_{OUT}$$

$$VDS = V_{IN} \times \left(\frac{1}{1-D}\right)$$

$$I_{D1} = I_{OUT} \times D$$

$$V_{D1} = V_{OUT} + V_{IN} \times \left(\frac{N_S}{N_P}\right) \times \left(\frac{1}{1-D}\right)$$



Application Notes:
Active Clamp and Reset Technique Enhances Forward Converter Performance (SEM1000)
Design Considerations for Active Clamp and Reset Technique (SEM1100)

Controllers:
UCC2891, 2, 3, 4, 7
UCC3580-1
UC3824