L7

The Bypass Capacitor in High-Speed Environments

SCBA007A

TEXAS INSTRUMENTS

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Introduction

High-speed switching environments generate noise on power lines (or planes) due to the charging and discharging of internal and external capacitors of an integrated circuit. The instantaneous current generated with the rising and falling edges of the outputs causes the power line (or plane) to ring. This behavior can violate the V_{CC} recommended operating conditions or generate false signals, creating serious problems. A simple and easy solution must be considered to prevent such a problem from occurring. This solution is the bypass capacitor.

Bypass Definition

A bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low-impedance supply, thereby minimizing the noise generated by the switching outputs of the device.

Bypassing Considerations

A system without bypassing techniques can create severe power disturbance and cause circuit failures. Figure 1 shows the V_{CC} line of the 'ABT541 ringing while all outputs are switching. Note that there is no bypass capacitor at the V_{CC} pin. There are a few issues that should be considered when bypassing power lines (or planes).

- The capacitor type
- The capacitor placement
- The output load effect
- The capacitor size

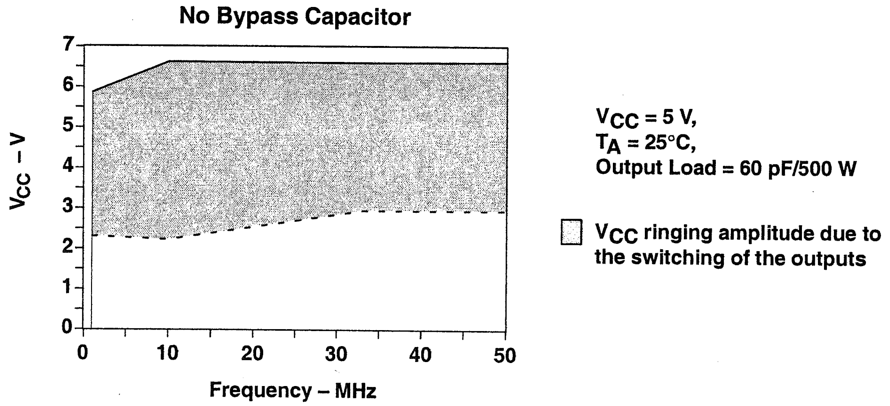


Figure 1. V_{CC} Line Disturbance vs Frequency

Capacitor Type

In a high-speed environment the lead inductances of a bypass capacitor become very critical. High-speed switching of a part's outputs generates high frequency noise (>100 MHz) on the power line (or plane). These harmonics cause the capacitor with high lead inductance to act as an open circuit, preventing it from supplying the power line (or plane) with the current needed to maintain a stable level, and resulting in functional failure of the circuit. Therefore, bypassing a power line (or plane) from the device internal noise requires capacitors with very small inductances. That is why the multilayer ceramic chip capacitors (MLC) are more favorable than others for bypassing power lines (or planes). They exhibit negligible internal inductance, thereby allowing the charge to flow easily, when needed, without degradation.

Capacitor Placement

Most of the printed circuit boards are designed to maintain a short distance between power and ground. This is done by laminating the power line (or plane) with the ground plane and can be electrically approximated with lumped capacitances as shown in Figure 2. However, this is not enough to have a reliable system, and another technique must be considered to provide a low-impedance path for the transient current to be grounded. This can be done by placing the bypass capacitor close to the power pin of the device.

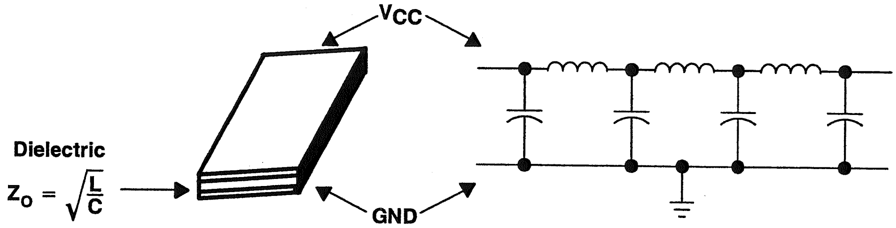


Figure 2. Typical Power Layout

Why This Location Is Very Important

Consider a device driving a line from low to high having an impedance ($Z \cong 100\ \Omega$) and a supply voltage ($V_{CC} = 5$ V) (see Figure 3). In order for the device to change state, an output current ($I = 50$ mA) is needed instantaneously. Note that for eight outputs switching, $I = 50 \times 8 = 400$ mA. This current is provided by the power line (or plane) in a period less than or equal to the rise time of the output (approximately 3 ns for ABT). The bypass capacitor must supply the charge in that same period to avoid V_{CC} drop; therefore, distance becomes an important issue. Line inductances can block the charge from flowing, leaving the power line (or plane) disturbed.

Using the formula for paralleled wires:

$$L = l\frac{\mu_0}{\pi}\ln\frac{d}{r} \tag{1}$$

Where:

d = distance between wires
l = length of the wires
r = radius of the wires
μ_0 = permeability of medium between wires

The inductance (L) is directly proportional to the distance between the lines as well as the length of the lines. Therefore, by reducing the loop ABCD in Figure 3, the inductance is minimized, allowing the capacitor to function more efficiently and, hence, keep the noise off the power line (or plane).

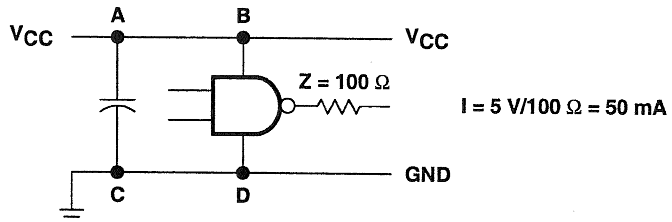
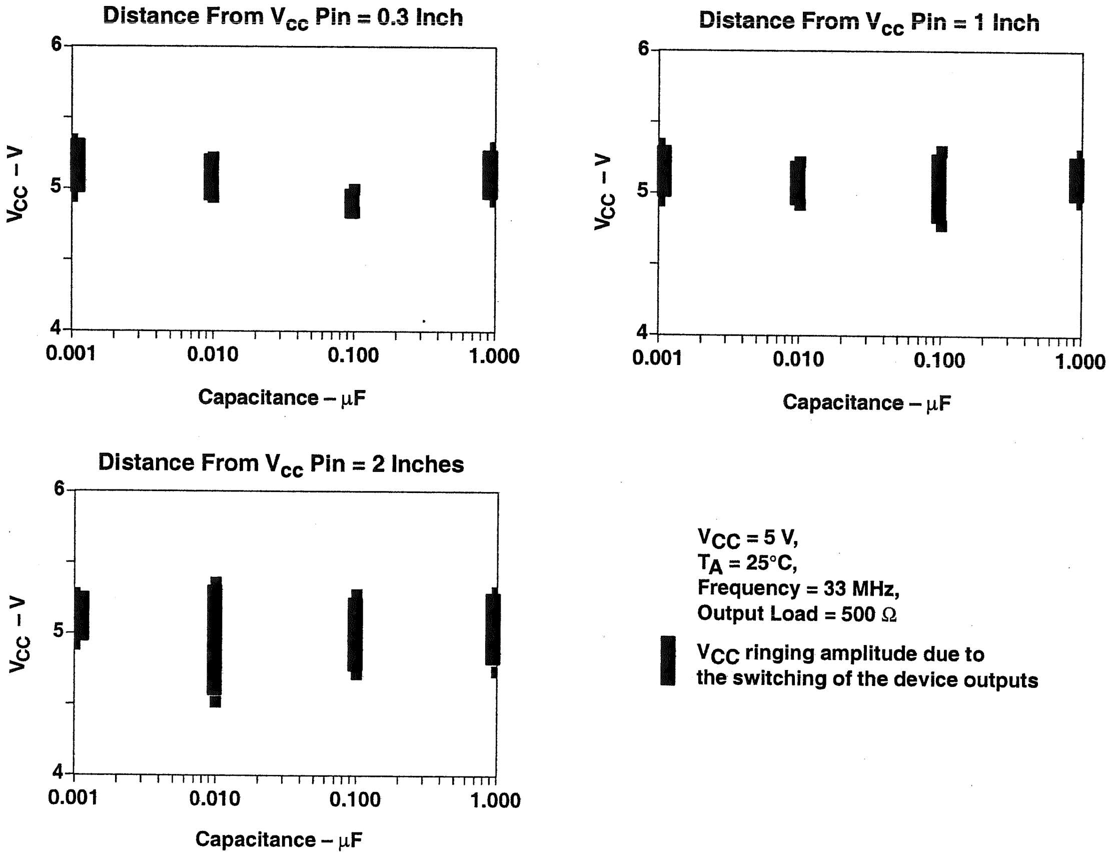


Figure 3. Capacitive Storage (Bypass Capacitor)

Several tests were performed on an 'ABT541 device to study the behavior of its power line (or plane) as the outputs switch simultaneously. This data is taken at different distances from the power pin (0.3, 1, and 2 inches) using four capacitors (0.001, 0.01, 0.1, and 1 μF), with an input frequency of 33 MHz and all eight outputs switching simultaneously (worst case). Figure 4 shows that the line disturbance increases as the capacitor is moved away from the power pin.


Distance From V_{CC} Pin = 0.3 Inch

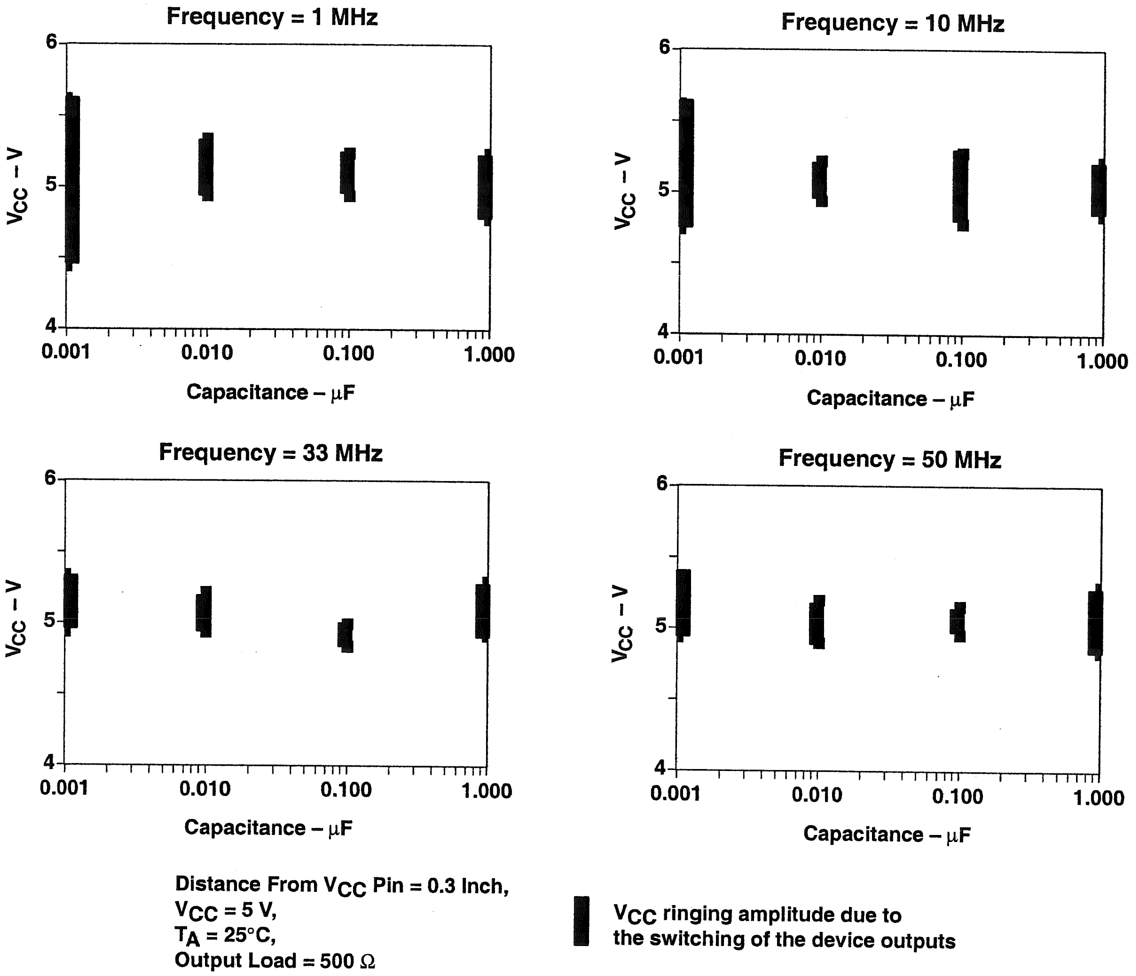
Distance From V_{CC} Pin = 1 Inch

Distance From V_{CC} Pin = 2 Inches

Figure 4. V_{CC} Line Disturbance vs Capacitor Size at Different Distances

Output Load Effect

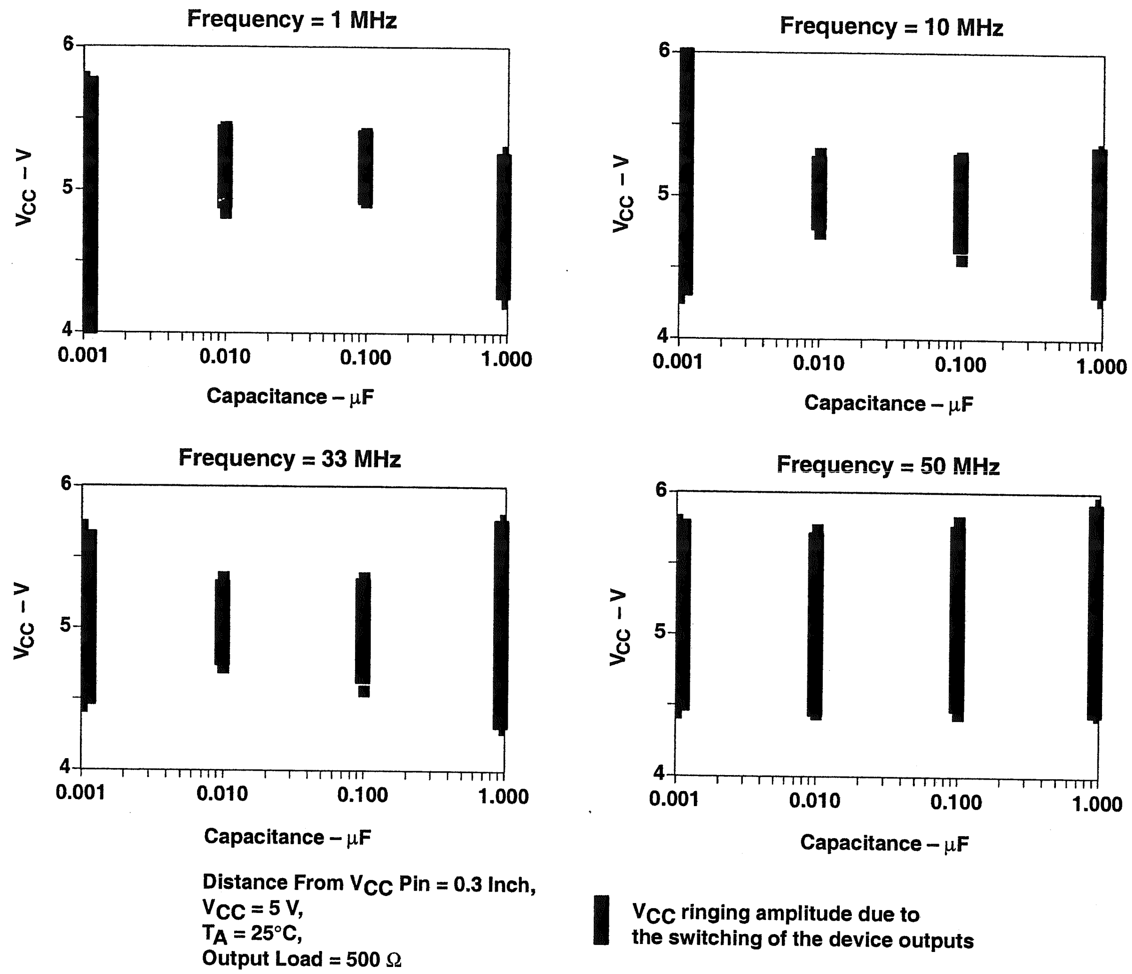
Capacitive loads combined with increased frequency result in higher transient current and possible V_{CC} oscillation. If the output load is purely resistive, the increase in frequency does not affect the rising and falling edge of the outputs; therefore, it does not increase the V_{CC} line disturbance. Figure 5 shows the power line behavior across frequency while driving only a resistive load. Figure 6 shows the same plot with an additional 60-pF capacitive load.



Distance From V_{CC} Pin = 0.3 Inch,
V_{CC} = 5 V,
T_A = 25°C,
Output Load = 500 Ω

▮ V_{CC} ringing amplitude due to the switching of the device outputs

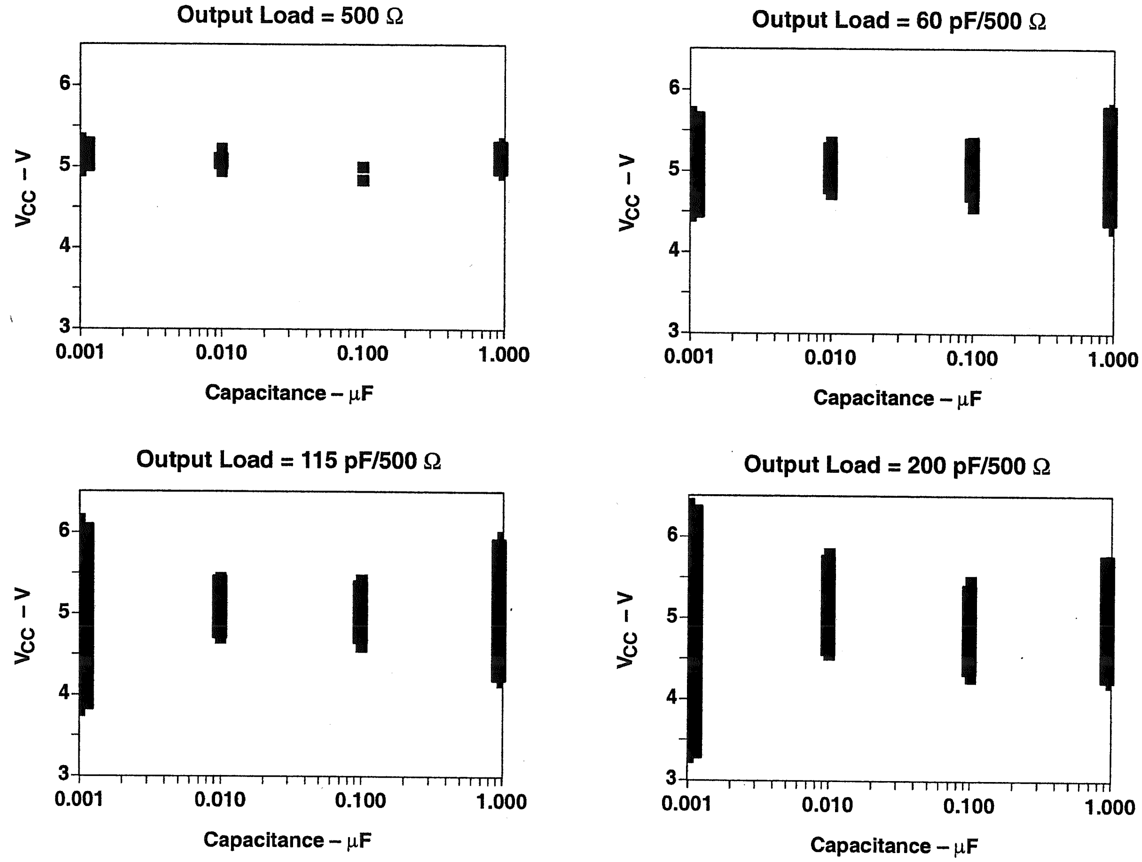
Figure 5. V_{CC} Line Disturbance vs Capacitor Size With Resistive Load at Different Frequencies



Distance From V_{CC} Pin = 0.3 Inch,
V_{CC} = 5 V,
T_A = 25°C,
Output Load = 500 Ω

Figure 6. V_{CC} Line Disturbance vs Capacitor Size With 60-pF Load at Different Frequencies

When driving large capacitive loads, more charge must be supplied to the output load, resulting in a slower rising or falling edge. However, if the bypass capacitor is not capable of providing the needed charge, power lines (or planes) start to ring and eventually oscillate, causing failures across the board. These oscillations can be of a great amplitude, 2- to 3-V p-to-p. Figure 7 shows these oscillations at four different loads (0, 60, 115, and 200 pF) using four different bypass capacitors (0.001, 0.01, 0.1, and 1 μF).



Distance From V_{CC} Pin = 0.3 Inch,
V_{CC} = 5 V,
T_A = 25°C,
Frequency = 33 MHz

▮ V_{CC} ringing amplitude due to the switching of the device outputs

Figure 7. V_{CC} Line Disturbance vs Capacitor Size at Different Capacitive Loads

Capacitor Size

How can we choose the right bypass capacitor? The most important parameter is the ability to supply instantaneous current when it is needed.

There are two ways to calculate the bypass-capacitor size for a device:

1. The amount of current needed to switch one output from low to high (I), the number of outputs switching (N), the time required for the capacitor to charge the line (Δt), and the drop in V_{CC} that can be tolerated (ΔV) must be known.

   The following equation can be used:

$$C = \frac{I \times N \times \Delta t}{\Delta V} \tag{2}$$

   where Δt and ΔV can be assumed.

For example, with $\Delta V = 0.1$ V, $\Delta t = 3$ ns, $N = 8$, and I obtained from either Figure 3 (for rough estimate) or from the plot in Figure 8 (assuming 50-MHz frequency), using $I = 44$ mA, the equation is:

$$C = \frac{44 \times 10^{-3} \times 8 \times 3 \times 10^{-9}}{0.1} = 10080 \times 10^{-12} = 0.01\ \mu F \tag{3}$$

2. Several capacitor manufacturers specify the maximum pulse slew rate. This allows the capacitor's maximum current to be calculated. For example, a 0.1-µF capacitor rated at 50 V/µs can supply: $i = c\ dv/dt = 0.1 \times 50 = 5$ A. This current is greater than the maximum current ($I \times N = 44$ mA $\times$ 8 outputs switching $= 352$ mA) required by the device used in the previous example.

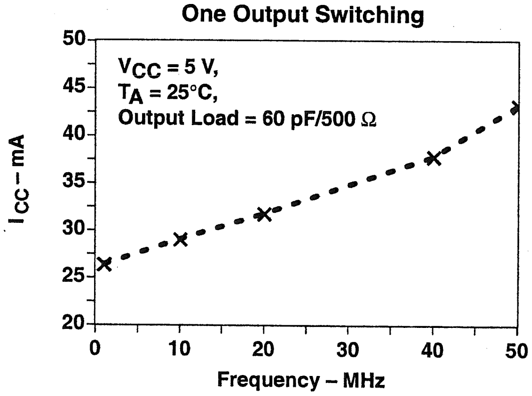


Figure 8. I_{CC} vs Frequency

Summary

Bypass capacitors play a major role in achieving reliable systems. The absence of the bypass capacitor can generate false signals and create major problems across the entire board. Figure 1 shows the undesired ringing caused by simultaneously switching the outputs of the 'ABT541. Also, choosing a capacitor with negligible lead inductance can avoid unpredictable behavior at high frequencies. Locating the capacitor closer to the V_{CC} pin of a device can avoid further complications and eliminate the ringing entirely. Figure 6 shows the V_{CC} line behavior with the bypass capacitor placed 0.3 inch away from the V_{CC} pin, whereas Figure 9 shows the same plot with the same load, but the bypass capacitor is located at the pin; there is dramatic improvement in the latter case. This technique can also be applied to Texas Instruments Widebus™ family by bypassing all V_{CC} pins. This is the most effective method for eliminating the V_{CC} line ringing. It is always important to minimize the loop between the V_{CC} pin, the ground, and the bypass capacitor. Finally, choosing the capacitor size by using either method mentioned earlier is highly recommended. If one considers all these issues, a good bypass technique can be employed.

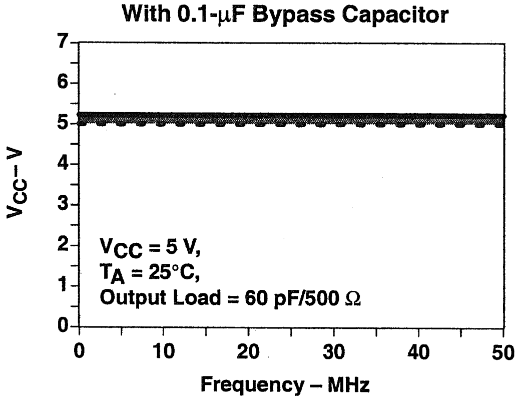


Figure 9. V_{CC} Line Disturbance vs Frequency

References

1 Texas Instruments Incorporated, "Advanced Schottky Family (ALS/AS) Applications," *ALS/AS Logic Data Book*, 1995, literature number SDAD001C.

2 Walton, D., "P.C.B. Layout for High-Speed Schottky TTL".