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DIRECTED ENERGY, INC. TECHNICAL NOTE

50MHz?

DE-SERIES FAST POWER MOSFET™

AN INTRODUCTION

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Abstract

The DE-SERIES Fast Power™ MOSFETs are unique high power devices designed as a circuit element from the ground up for high speed, high frequency, high power applications. This technical note describes the patented technology utilized to achieve and optimize the electrical, thermal and mechanical performance of the DE-SERIES devices.

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Table Of Contents

Introduction

From its inception, power MOS has held great promise because of its potential speed. In fact, the particle transit time, drain to source, in any cell of the silicon die is theoretically on the order of 200ps (1). However conventional power MOSFET packages are poorly suited to high speed, high frequency applications.

It is interesting to note that the TO-3, a common high power package, was designed in the 1950s and mimics the octal pin and bolt pattern of a vacuum tube socket. The plastic TO-220 and TO-247 packages followed, providing some improvements, and more recent packages like the TO-254 and large block configurations have appeared. However, the topology and materials of these large high power packages are highly inductive, their thermal performance poor, and their mounting configuration at variance with low impedance circuit layout.

Even Radio Frequency (RF) type packages, when used with large power MOSFET die, suffer from similar problems. In short, die packaging has been addressed as a mechanical tooling convenience more than a circuit element. And in the interim, die chemistry and topology have been altered to stabilize operation because of these shortcomings (2).

The DE-SERIES Fast Power ™ MOSFETs illustrated in Figure 1 are a new class of unique high power devices designed as a circuit element from the ground up for high speed, high frequency, high power applications. DEI's Fast Power ™ technology features low insertion inductance (≈1.5nH), and a low profile package, with a $R_{\theta JC}$ as low as 0.17°C / W, which provides exceptional switching speeds and power handling capabilities.

The DE-SERIES, available in 4 power ranges (DE-150, DE-275, DE-375 and the DE-475) offer 10 times the speed and 3 times the power dissipation, with 1/2 the volume, 1/3 the weight and greatly reduced die stress, of comparable conventional power MOSFET devices. This article will describe the patented (13) technology utilized to achieve and optimize the electrical, thermal and mechanical performance of the DE-SERIES.

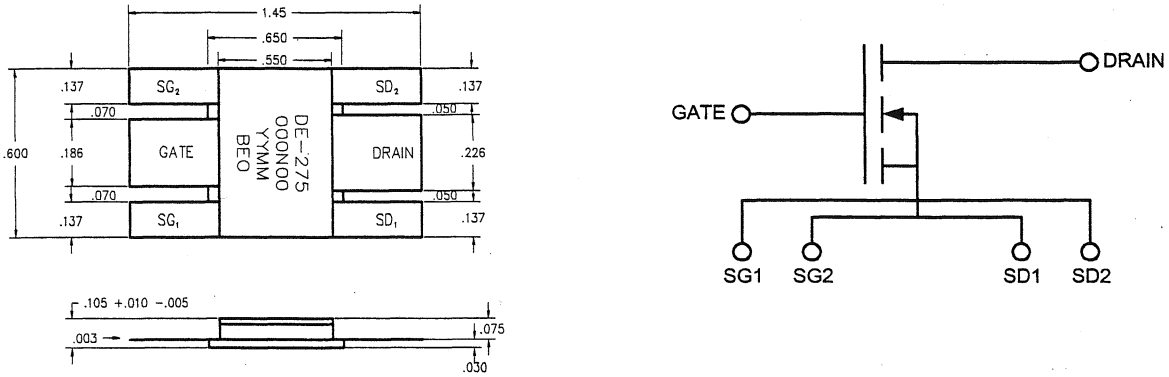
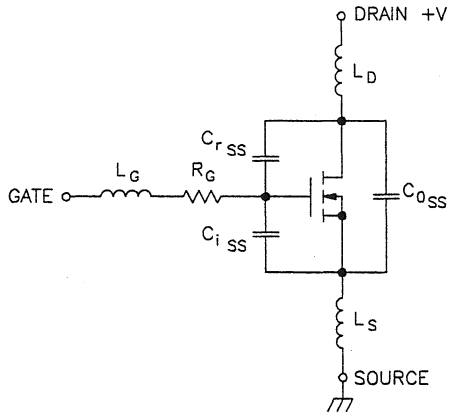


FIGURE 1. DE-SERIES Fast Power Mosfet™

Standard Packaging



TO-247 (Typical)	DE-275 (Typical)
V_{DS} = 500V	V_{DS} = 500V
I_{DS} = 16A	I_{DS} = 16A
gfs = 14S	gfs = 14S
C_{ISS} = 2700pF	C_{ISS} = 2400pF
C_{RSS} = 75pF	C_{RSS} = 25pF
C_{OSS} = 350pF	C_{OSS} = 125pF
$R_{DS\ (ON)}$ = 0.40Ω	$R_{DS\ (ON)}$ = 0.40Ω
$R_g \approx$ 2-5Ω	$R_g \approx$ 0.2Ω
$L_S \approx$ 13nH	$L_S \approx$ 0.5nH
$L_G \approx$ 13nH	$L_G \approx$ 1nH
$L_D \approx$ 5nH	$L_D \approx$ 1nH
$R_{\theta jhs}$ = 1.0°C/W	$R_{\theta jhs}$ = 0.33°C/W

Figure 2. MOSFET Circuit Model

In order to more clearly understand the necessity for the mechanical topology of the DE-SERIES, it is useful to first look at some of the negative feedback terms in power MOSFETs.

Negative Feedback Terms in Active Devices

Figure 2 illustrates the circuit model for a conventional MOSFET; the same analysis applies to bi-polar devices. The effect of the L_D term is on the output circuit and is often of little consequence. There are several parasitic elements that inhibit high-speed operation. At turn-on, if we apply a step voltage function to the external gate terminal, with T_r= 0 and Z_o= 0, the parasitic elements L_G, R_G and L_S isolate in time the capacitance of the internal gate structure of the power MOSFET such that the rate of voltage rise on the gate structure is limited to the quarter wave time of this network (T_r = 1/4F), thus slowing the turn-on of the device. Furthermore, this L_G, L_S, R_G, C_{iss}, C_{rss} network forms a resonant tank circuit which can oscillate and cause spurious operation of the MOSFET (2). In addition, this resonance will limit the maximum useful frequency of the device.

When the device turns on, there are additional parasitic elements that further inhibit high-speed operation. As current rises in the drain circuit, the voltage developed across L_S provides a negative feedback term, which further limits the turn on speed. In conjunction with the L_S term, as current rises in the drain circuit, the voltage fall at the drain is coupled to the gate circuit via C_{rss} (the Miller effect), providing additional negative feedback to the gate. The effect of the input RLC on rise time and frequency are given by equations 1 and 2. The first of these is the C term. This includes the input capacitance and the miller capacitance. We will call this term $C_{(NET)}$.

E1. $$C_{(NET)} = C_{iss} + \left(C_{rss} \frac{dV_{DS} - (dV_{GS})}{dV_{GS}} \right) = C_{iss} + \left(C_{rss} \frac{dV_{DG}}{dV_{GS}} \right)$$

E2. $$F_{MAX} \approx \frac{1}{2\pi \sqrt{\left((L_G + L_S) \bullet \left(C_{iss} + \left(C_{rss} \frac{dV_{DG}}{dV_{GS}} \right) \right) \right)}}$$

E3. $$T_r \equiv \frac{1}{4F} \approx \frac{2\pi \sqrt{\left(\left((L_G + L_S) \bullet \left(C_{iss} + C_{rss} \frac{dV_{DG}}{dV_{GS}} \right) \right) \right)}}{4}$$

Substituting values into equation 1 from Figure 2, assuming a 26nH loop inductance between the source lead and gate lead of the TO-247 MOSFET (note that no allowance is made for the inductive or capacitive contributions of the gate driver), and given a gate drive of 15V and a drain voltage fall of 465V we get:

E4. $$T_r \approx \frac{2\pi \sqrt{\left((13nH + 13nH) \bullet \left(2.7nF + \left(75pF \frac{450V}{15V} \right) \right) \right)}}{4} = 17.8ns$$

From equation 4 we see that for large signal operation the gate voltage will not rise any faster than ≈18ns. Looking at the maximum frequency we have:

E5. $$F_{MAX} \approx \frac{1}{2\pi \sqrt{\left((13nH + 13nH) \bullet \left(2.7nF + \left(75pF \frac{450V}{15V} \right) \right) \right)}} = 14.0MHz$$

From equation 5 we see that the device goes self-resonant at approximately 14MHz. If the gate-source loop inductance is reduced to to 1.5nH, which is consistent with the insertion inductance for the DE-SERIES, and insert the capacitive terms from the DE-SERIES data sheet we find that $F_{MAX} \approx 69MHz$ and $T_r \approx 4ns$. This does not mean that the absolute maximum frequency of the device is 69MHz (it is actually higher), but is a means of comparing the relative frequency capability between TO-247 and DE-275 Series devices.

Equations 1 and 2, however do not include the negative feedback effect of the source lead inductance L_S or the negative effect of L_G and R_G on gain, gfs. To look at this effect, recall that:

E6. $I_{DS} = gfs(V_{GS} - V_{TH})$ also $V_{GS} = V_{GATE-DRIVE} - V_{LS}$

$$V_{LS} = L_S \frac{dI_{DS}}{dt} \text{ therefore:}$$

$$I_{DS(t)} = gfs\left(V_{GATE-DRIVE_{(t)}} - V_{TH} - L_S \frac{dI_{DS}}{dt} \right)$$

Recall from Figure 2 that the two V_{GS} nodes are nested in the L_G, R_G, L_S loop. This loop forms a frequency dependent voltage divider given by:

E7. $$\frac{X_{(CNET)}}{R_G + X_{(CNET)} + X_{LS} + X_{LG}}$$ combining all terms we have:

E8. $$I_{DS(t)} = gfs\left(V_{GS} - V_{TH} - L_S \frac{dI_{DS}}{dt} \right) \times \left(\frac{X_{(CNET)}}{R_G + X_{(CNET)} + X_{LS} + X_{LG}} \right)$$

If we set the I_{DS} at a fixed value and rearrange the terms, we can plot the change in required gate voltage $\mathbf{V_{GSR}}$ and gfs vs frequency.

E9. $$V_{GSR} = \frac{I_{DS}}{gfs\left(\frac{X_{(CNET)}}{R_G + X_{(CNET)} + X_{LS} + X_{LG}} \right)} + L_S \frac{I_{DS}}{\left(\frac{1}{4F} \right)} + V_{TH}$$

In Figures 3 and 4 below, a DE-Series DE-275 device and a typical TO-247 device of the same voltage rating were operated in a common test fixture. In Figure 3 we see the required gate drive voltage $\mathbf{V_{GSR}}$ to overcome the negative feedback terms of equation 9. The following plots show an L_S+L_G product of 1.5nH for the typical DE-SERIES device to 26nH for the typical TO-247 device. The difference in required drive voltage between 1.5nH (a typical DE-SERIES) and 26nH (a typical TO-247) at 100MHz is an increase of about a factor of seven.

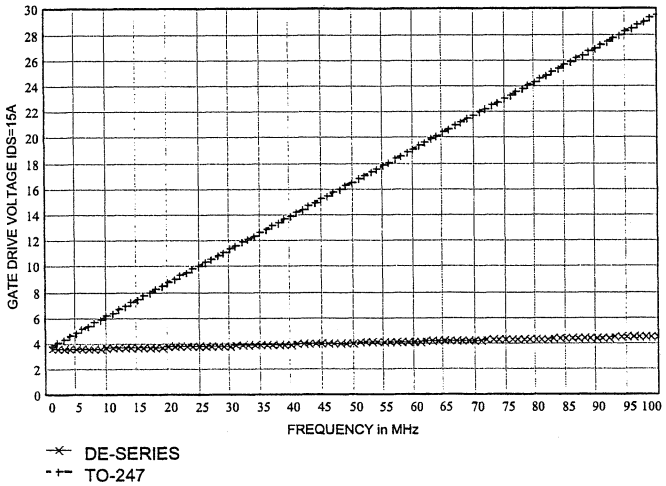


Figure 3 Gate Drive vs Frequency

Substituting V_{GSR} of Equation 9 for the V_{GS} term in the classical gfs equation we get gfs vs frequency gfs_F ;

$$E10. \quad gfs_F = \frac{Ids}{V_{GSR} - V_{TH}}$$

In Figure 4 we see the gfs vs frequency for the same inductance values. At 50MHz the difference from 26nH of the TO-247 to 1.5nH of the DE-SERIES is a 10 to 1 increase in gain.

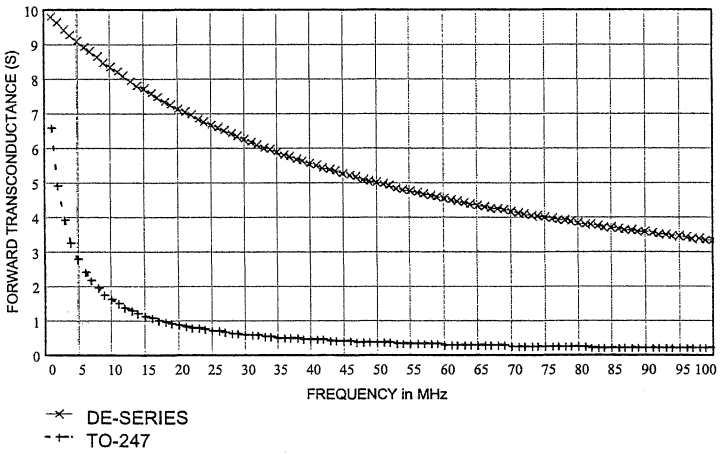


Figure 4 gfs vs Frequency

It is clear that a new packaging concept, a new paradigm, is necessary to address and, as much as practical, eliminate these parasitic inductive elements. To explore this further, let us look at the mechanical nature of these inductive terms.

Inductance in Three Dimensional Space

Recalling the previous discussion on the effects of stray inductance, it is useful to examine just how big, physically, a 26nH inductor is. This lets us see, in a dynamic way, the need for extreme care in package and die design as well as circuit layout.

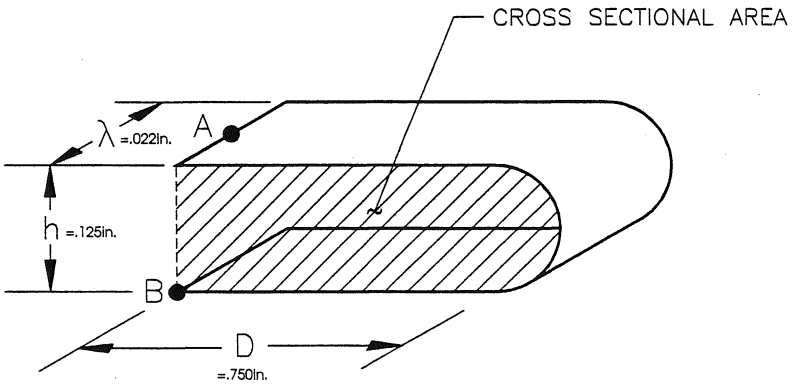


Figure 5. One Turn Inductor

The one turn inductor shown in Figure 5 is equivalent to one turn of 0.022 inch wide conductor (λ) wound on a 0.125 inch diameter (h). With distance (D) equal to 0.750 inches, the inductance of this one turn coil is given by equation 11 (4):

$$\text{E11.} \quad L \approx \left[\frac{K\mu_0\mu_r N^2 A}{\lambda} \right]$$

Where:

L = inductance in Henrys
K = a dimensionless constant, form factor correction (10.) (K=.2)
μ_o = the permeability of free space, ($\mu_o = 4\pi$E-7 H/M)
μ_r = the relative permeability ($\mu_r = 1$)
N = the number of turns (N = 1)
A = the cross sectional area of the coil (A = 5.81E-5M^2)
λ = width of the conductor (λ = 5.5E-4M)

Inserting values as described for Figure 5 in equation 11, we get:

$$\text{E12.} \quad L \approx \frac{.2\left[\left(12.5\text{E}-7\,\frac{\text{H}}{\text{M}}\right)\bullet\left(5.81\text{E}-5\,\frac{\text{H}}{\text{M}}\right)\right]}{5.5\text{E}-4\text{M}} = 26\text{nH}$$

This is the inductance for the mechanical loop of Figure 5 and is equal to the L_G+L_S loop inductance for the MOSFET of Figure 2. Given the small size of the loop, it would appear that any attempt to reduce its inductance could prove futile. However the reduction of the inductance, as shown earlier, can provide exceptional improvement in performance and is therefore worth the effort.

Recalling equation 11, we can simplify this equation so that we can get a feel for what parameters are driving the inductance.

Let: μ_o , N and μ_r = 1, then:

$$\text{E13.} \quad L \propto \frac{A}{\lambda}$$

From equation 13 we see that we must minimize the cross sectional area A (Area Minimization) (Figure 5) and maximize the width λ (Multiple Distributed Paths). If we reduce A by 10 or increase λ by 10, the inductance would be down to 2.6 nH. However there are practical limits that will limit how far we can push these parameters. This means that we must invoke additional physics to drive the inductive term even lower.

If we recall that the inductive term is actually derived from the energy stored in the magnetic field, and if we can reduce or eliminate the energy stored in the magnetic field (B), then the inductive term will be reduced accordingly. We can do this by coupling magnetic field vectors of equal magnitude 180° out of phase to yield a resultant of ≈0. This is the patented technique we call EM-Symmetry. In fact, EM-Symmetry by necessity invokes Area Minimization (A) and Multiple Distributed Paths (λ), which are subsets of the complete process.

Electrical Advantages

EM-Symmetry

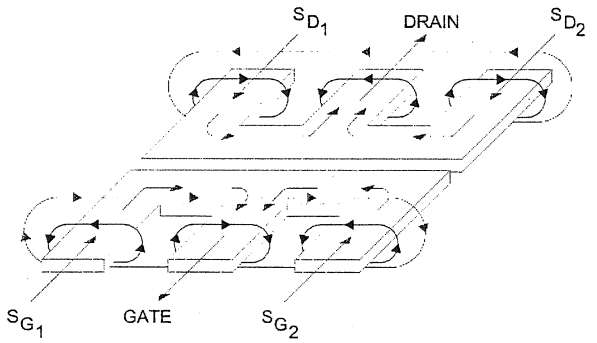


Figure 6. Coplanar DE-Series Structure

DEI developed EM-Symmetry, shown in Figure 6, to address the need for a true low inductance, high speed, and high power device. The package design is best described as a distributed coplanar transmission line.

In a coplanar line the ground tracks lie on either side of the signal track (3). This topology provides several benefits. The distribution of the E and B fields are symmetric and uniform, the currents flow in sheets, and the voltage gradient changes are smooth and continuous. Referring to Figure 6, the conductors and die are shown as one element. In the DE-SERIES devices they form a coplanar transmission line. As illustrated, S_{G1} and S_{G2} are the ground tracks for the Gate signal while S_{D1} and S_{D2} are the power ground tracks used for the Drain signal. By circuit topology we insure that:

E14. $I_G = I_{SG1} + I_{SG2}$ and $I_{SG1} \approx I_{SG2}$ so that $B_{IGS1} + B_{IGS2} \Rightarrow 0$

Furthermore:

E15. $I_D = I_{SD1} + I_{SD2}$ and $I_{SD1} \approx I_{SD2}$ so that $B_{IDS1} + B_{IDS2} \Rightarrow 0$

This symmetry (E14 and E15) provides cancellation of magnetic field vectors in the far field, effectively reducing the insertion inductance. To enhance switching speed further, the source lead inductance negative feedback term $L_S di/dt$ found in all conventional devices (5) has been eliminated by integrating a differential Kelvin lead with EM-Symmetry of the input leads. Thus, the gate drive reference plane floats on the $L_S di/dt$ term, and therefore the drain source currents flowing in S_{D1} and S_{D2} are prevented by topology from flowing in S_{G1} and S_{G2}.

Some manufacturers have invoked a Kelvin lead with no reduction in insertion inductance. This can have serious effects on device stability and reliability (5).

Die Topology

The DE-SERIES die, shown in Figure 7, are manufactured with epitaxial material to more precisely control material properties (6). They are also designed with "small" horizontal and vertical structures and "small" cell size so that particle transit times are consistent with the desired operating frequency (6). These die also employ multiple gate and source pads consistent with the coplaner package design of the DE-SERIES. The die also has an extraordinarily low value of R_G. Coupled with the preceding, the IXYS Q_g process provides a low capacitance per I/V.

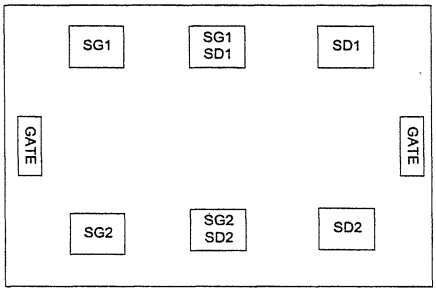


Figure 7 DE-SERIES die topology

Electrical Performance

The DE-Series represent the highest level of performance of any high voltage high power MOSFET available today.

1. Vds=100V to 1000V
2. $T_{ON} \leq 2ns$
3. $T_{ON\ DLY} \leq 3ns$
4. $T_{OFF} \leq 2ns$
5. $T_{OFF\ DLY} \leq 3ns$
6. $F_{MAX} \geq 150MHz$
7. $I_{DS\ CONT} \geq 50A$
8. $I_{DS\ MAX} \geq 6X\ I_{DS\ CONT}$ in pulse mode
9. $P_{DIS\ MAX} \geq 700W$

This level of performance is now limited only by the parasitic elements C_{OSS}, C_{RSS}, C_{ISS}, and the capability of the gate drive. Therefore DEI has developed and continues to develop an extensive array of high performance gate driver designs (7).

Thermal and Mechanical Advantages

The drain substrate, usually copper in typical devices, is by default a very electrically active node. This requires an electrical insulator and therefore loss of thermal performance. The mismatch in Thermal Coefficient of Expansion (TCE) between the die and this substrate is large, often requiring buffering materials that further degrade the thermal performance. Furthermore, the mounting screw attaches the package to the heat sink at one point. The heatsink and the drain substrate are usually very different materials. When operated in a high power dissipation mode, the package will warp as shown in Figure 8 by the red arrow. This causes a loss of thermal contact, hence loss of power handling capability and an increase in mechanical die stress.

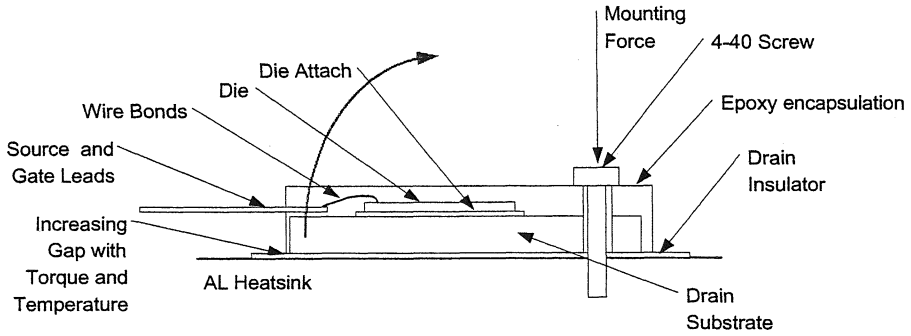


Figure 8 TO-247 Cross-section

For high power applications, the DE-SERIES incorporates several design features to provide excellent thermal dissipation and high power handling capability while offering a less cumbersome mounting technique than the conventional devices we have described. The first of these is illustrated in Figure 9.

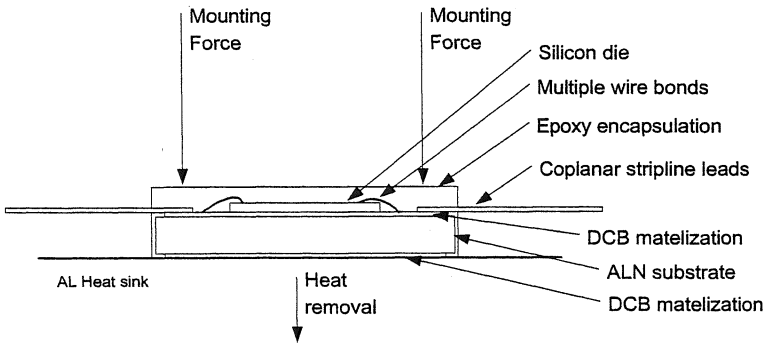


Figure 9 DE-SERIES Cross-Sectioned View

Here we see a cross-sectioned view of a DE-SERIES device and the thermal path from die surface to the heat sink. By minimizing layer thickness, selecting materials with low thermal impedance and with a TCE near silicon, a multi-layer configuration is assembled that not only provides low thermal impedance and low die stress but also allows for electrically isolated elements, gate, drain and source. This configuration and selection of materials provide the DE-SERIES devices with exceptional thermal resistance, ($R_{\theta jc}$) as low as 0.17^0 C/W.

There is a further electrical advantage of the DE-SERIES that falls out of this mechanical topology. The case (drain) to ground capacitance is approximately 10pF, compared to 100pF for a TO-247 isolated from the heat sink with a 2 mil thick kapton insulator. In high frequency, high power applications, this large capacitance can cause large ground currents and EMI problems. Furthermore, it appears directly across the drain and contributes to C_{oss} losses.

In a low power mounting configuration, the device can be mounted on the top side of the PCB in a standard surface mount configuration. Furthermore due to the mechanical symmetry of the DE-SERIES, the device can also be mounted with the ambient air in contact with the heat removal surface (device label against the PCB). This is still a low power configuration.

Mechanical Performance

In order to maintain a low thermal impedance, the package design must be capable of maintaining intimate contact between the heat extraction surface of the package and the heat sink, and at the same time allow the device to expand in X (width of heat sink), Y (length of heat sink), and Z (normal to heat sinking surface). Figure 10 illustrates how this is accomplished with the DE-SERIES.

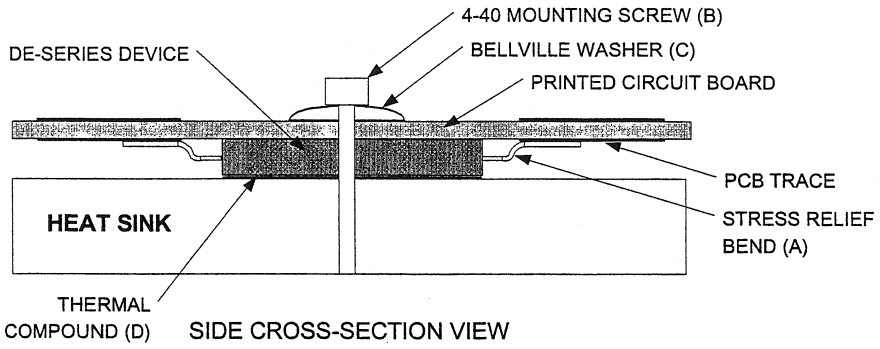


FIGURE 10. High Power MOSFET Mounting

(A) The leads are bent up and soldered to the bottom side of the PCB. This allows the device to be removed from the heat sink with the PCB, simplifying assembly procedures. The leads of the DE-SERIES are made of 99.9% pure copper with the grain structure aligned in the direction of the lead length, producing an extremely soft lead. This, along with the stress relief bend, provides excellent lead compliance and offers low stress to the package seals.

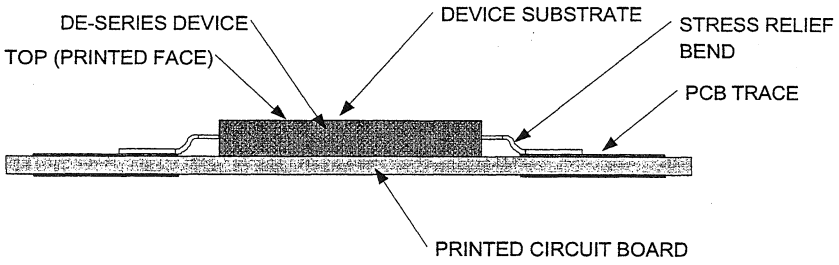
(B) Two screws pass through the PCB on either side of the device, and place it in compression this provides X and Y compliance.

(C) Belleville washers provide vertical compliance and maintain an even pressure on the device. This allows vertical Z expansion with no loss of contact.

(D) The DE-SERIES package design virtually floats on the thermal compound. This allows the device to maintain excellent thermal contact with the heat sink, yet expand in X, Y and Z while minimizing the mechanical stress.

This package design and mounting configuration give the DE-SERIES a factor of 3 increase in power handling capability over conventional devices while also providing for isolated elements. In the low power configuration, the device is mounted on the component side in traditional surface mount style.

For low average power applications, the device may be mounted on the component side in traditional surface mount style as shown in Figure 11 below. (Low power is defined as that power level which will not exceed the free air dissipation rating of the device when mounted as shown in Figure 11.) The MOSFET is mounted on the component side of the PCB, with the top (printed face) of the device flat against the PCB.



SIDE CROSS-SECTION VIEW

FIGURE 11 Low Power MOSFET Mounting

Thermal Performance

In order to illustrate the high power performance of the DE-SERIES, TO-247 and DE-SERIES devices were operated in a high power configuration. These data were taken under real world operating conditions. The devices were installed on the heat sink, which was maintained at 25°C. The TO-247 was mounted with a 0.002 kapton insulator and thermal compound was used on both devices.

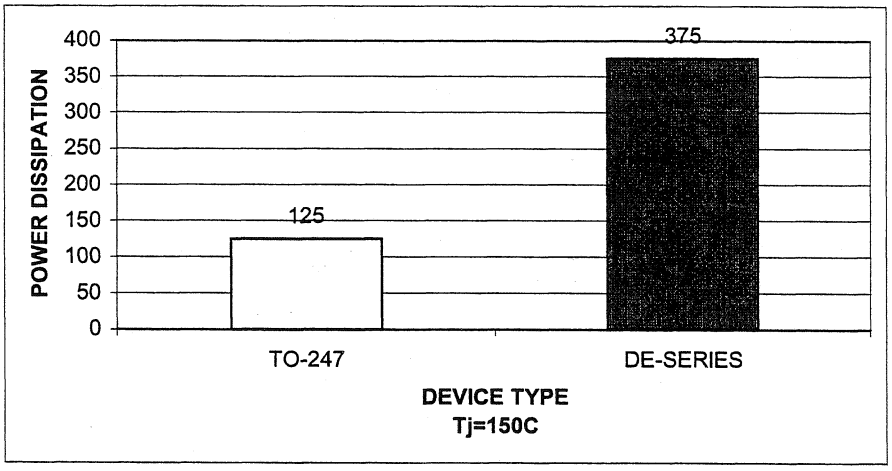


Figure 12 Power Dissipated in MOSFET

In Figure 12, we see that the power dissipation of the DE-SERIES device is a factor of 3 over the TO-247.

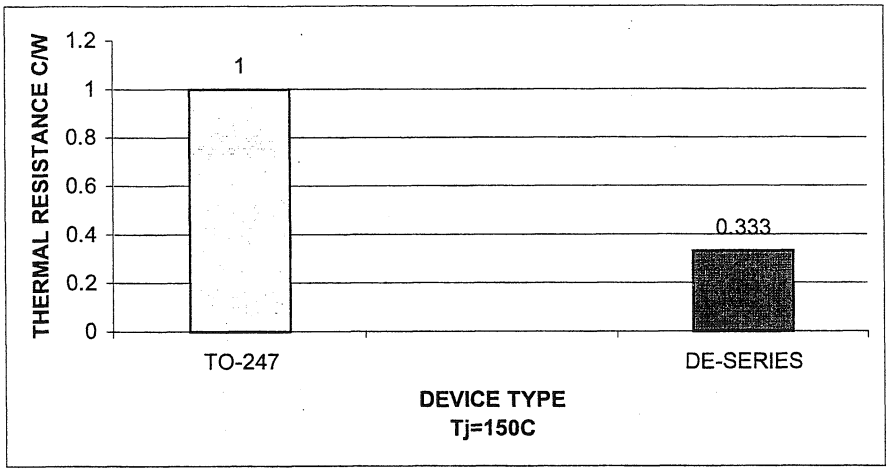


FIGURE 13. Thermal Resistance $R_{\theta jHS}$

Figure 13 shows that the $R_{\theta jHS}$ of the DE-SERIES is far superior to that of the TO-247.

Quality and Reliability

DEI / IXYS are committed to setting a new standard for excellence in power semiconductors. Reflecting our dedication to industry leadership in the manufacture of medium to high power devices, reliability has assumed a primary position in raw material selection, design, and process technology. Reliability utilizes information derived from applied research, engineering design, analysis of field applications and accelerated stress testing and integrates this knowledge to optimize device design and manufacturing processes. All areas that impact reliability have received considerable attention in order to achieve our goal to be the #1 reliability supplier of power semiconductor products.

We believe DEI / IXYS products should be the most reliable components in your system. We have committed significant resources to continuously improve and optimize our device design, wafer fab processes, assembly processes and test capabilities. As a result of this investment, DEI / IXYS has realized a dramatic improvement in reliability performance on all standardized tests throughout the product line. Excellence in product reliability is "built-in", not tested-in. Moreover, it requires a total systems approach, involving all parties: from design to raw materials to manufacturing. In addition to qualifying new products released to the market, life and environmental tests are periodically performed on standard products to maintain feedback on assembly and fabrication performance to assure product reliability.

To that end the following tests are preformed: High Temperature Reverse Bias (HTRB), High Temperature Gate Bias (HTGB), Temperature Cycle Humidity Test and Power Cycling. More information is available on the DEI / IXYS web sites (www.directedenergy.com and www.ixys.com).

Conclusion

The DE-SERIES devices provide a combination of unparalleled speed, power and frequency. The specific advantages are reviewed below.

Key Advantages of the DE-SERIES

1. **Switching Speed:** ≤HF RF MOSFET devices and ≈5-10 times faster than conventional MOSFETs.
2. **Frequency:** Equal to many HF RF devices and at least 5-10 times higher than conventional MOSFETs.
3. **High gain:** Approximately 3 times higher than HF RF MOSFET devices.
4. **Power Dissipation:** Approximately twice that of HF RF MOSFET devices and over 3 times higher than conventional MOSFET devices.
5. **High Power Surface mount design:** This allows the device to be loaded on to the PCB with all the other components in a high or low power configuration, simplifying mechanical assembly of the system.
6. **Lowered Mechanical Stress:** The device floats on the thermal compound such that the mounting hardware will not induce further package stress.
7. **Low Inductance Packaging:** The DE-SERIES has the lowest insertion inductance of any equivalent power device.
8. **Economical High Power Mounting:** The mounting configuration does not require machining of the PCB or an expensive clamping mechanism.

The DE-SERIES employs the most electrically, mechanically and thermally advanced high-speed device design available today. The combination of silicon die and packaging make the DE-SERIES the device of choice for high power high-speed applications.

Design Assistance Program

DEI provides design assistance, which includes on-site training and product design assistance. The specifics of this service are dependent on the needs of the client. Please contact DEI for details.

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