LAB1 – WEBENCH SIMULATION

EE562: POWER ELECTRONICS

COLORADO STATE UNIVERSITY

PURPOSE: The purpose of this lab is to explore National Semiconductors WEBENCH, which is an online design and prototyping tool. WEBENCH provides a plug-in power supply design which is customized to particular specifications. This is an on-line environment which saves time in the design process. Design, optimize, generate a prototype, and download test vectors—all online. This can all be done for free, anywhere, anytime. This lab will introduce the following aspects of WEBENCH.

- Design a customized plug-in power supply
- Vary C_{SS}
- Vary C_{OUT}
- Vary Inductors
- Discuss tradeoffs between components

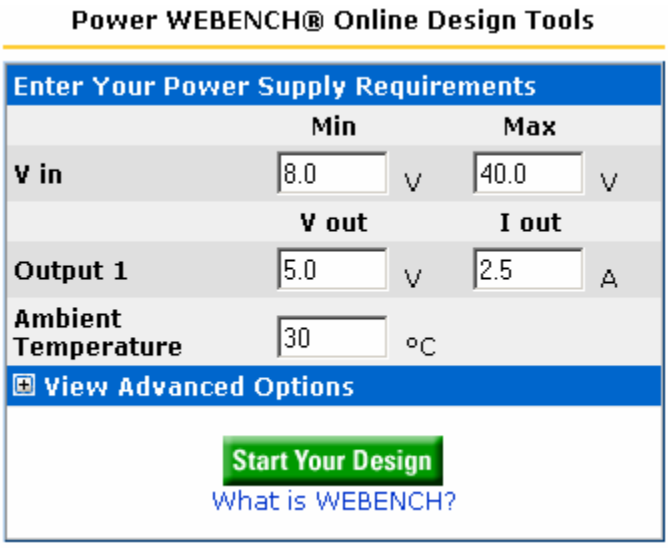
Design a customized plug-in power supply

Through four steps, WEBENCH enables its users to quickly design a power supply customized to their specifications.

1. Choose a part based on your specifications
2. Create a design including passive components and important calculated operating values
3. Analyze a design using the WEBENCH electrical simulation
4. Build it and take your virtual design to the real world

The focus will be to create a power supply design. WEBENCH can be accessed through the menu bar on the *National* web site homepage (be sure to select power).

The first step is to enter the power supply design requirements in the design tool displayed. For this design we will select the following:



It is now time to begin the design.

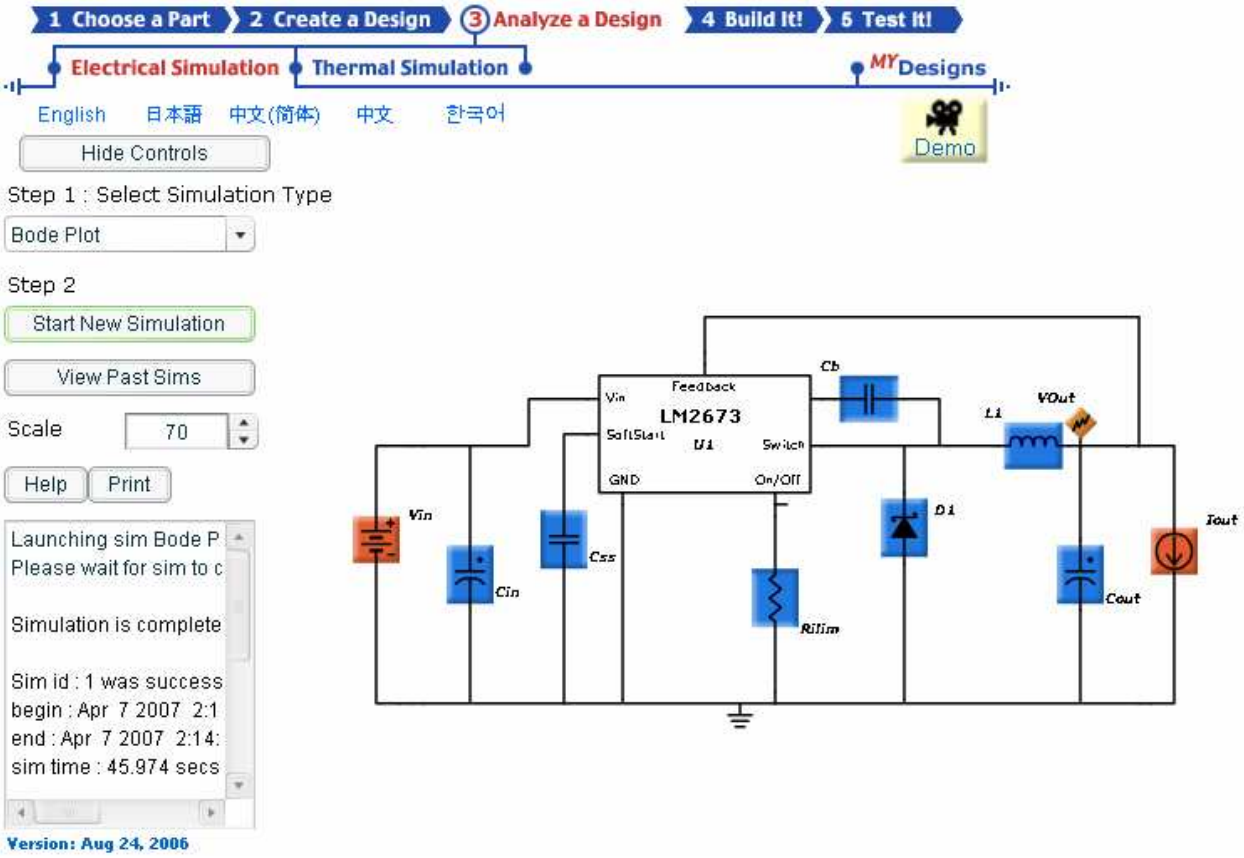
On the “Recommended Parts” page, the recommended devices are shown at the top of the page. This may include various regulators and/or converters. If the recommended part is enabled for WEBENCH, there will be a “Start Your Design” button below the part number. Clicking on that button will access the WEBENCH design environment.

Select the **LM2673-5.0** for this exercise (select “Start Your Design” adjacent to LM2673-5.0).

This is the “Components” screen. It summarizes the design thus far, including the power supply requirements and the IC selected. In addition, the external components needed for the total solution are listed with manufacturer, part number, and key values. Also shown is the footprint of the component.

Click the “Analyze a Design” tab. WEBENCH Electrical Simulator will be used, or click the “Click to start your electrical simulations” icon located on the right of the screen.

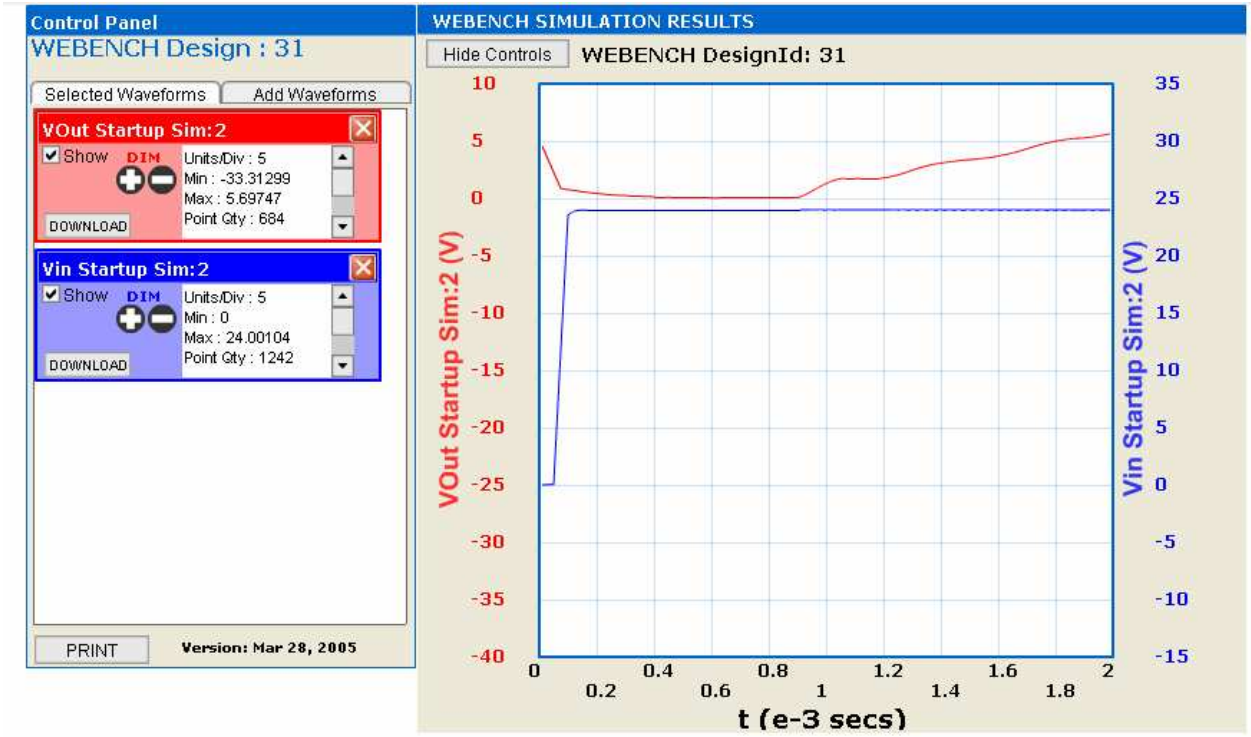
Now begin using the WEBENCH Electrical Simulator to do electrical simulations for the design. User changeable components used in the schematic are highlighted with blue boxes, simulation parameters are highlighted with red boxes and probe points are highlighted with yellow boxes. Hoover over any component to display any pertinent information.



Set up simulations by using the controls on the left side of the screen. To run a simulation, click on the "Start New Simulation" button. Simulation results typically take between 15 and 90 seconds. After the simulation is complete, the waveform viewer allows the user to view current and voltage waveforms as shown by the probe symbols of the schematic. Several types of simulations may be run including start-up, input line transient, output load transient and steady state. A Bode plot can also be obtained.

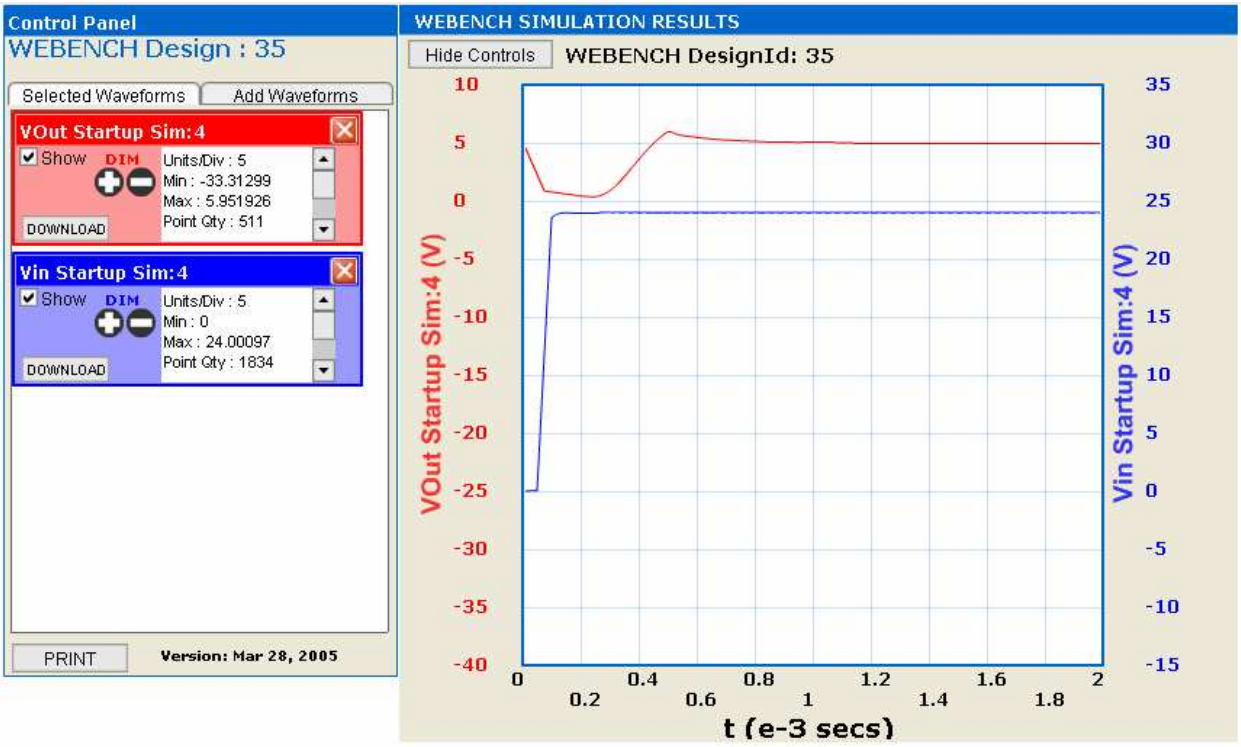
Vary C_{SS}

Select Startup in the drop down menu under step1: "Select Simulation Type" in the controls to run a start-up test on this circuit to see the various effects C_{SS} has on the circuit.
Do an initial start-up simulation with C_{SS} = 4.7 nF. (This was the default capacitor assigned to the design.)



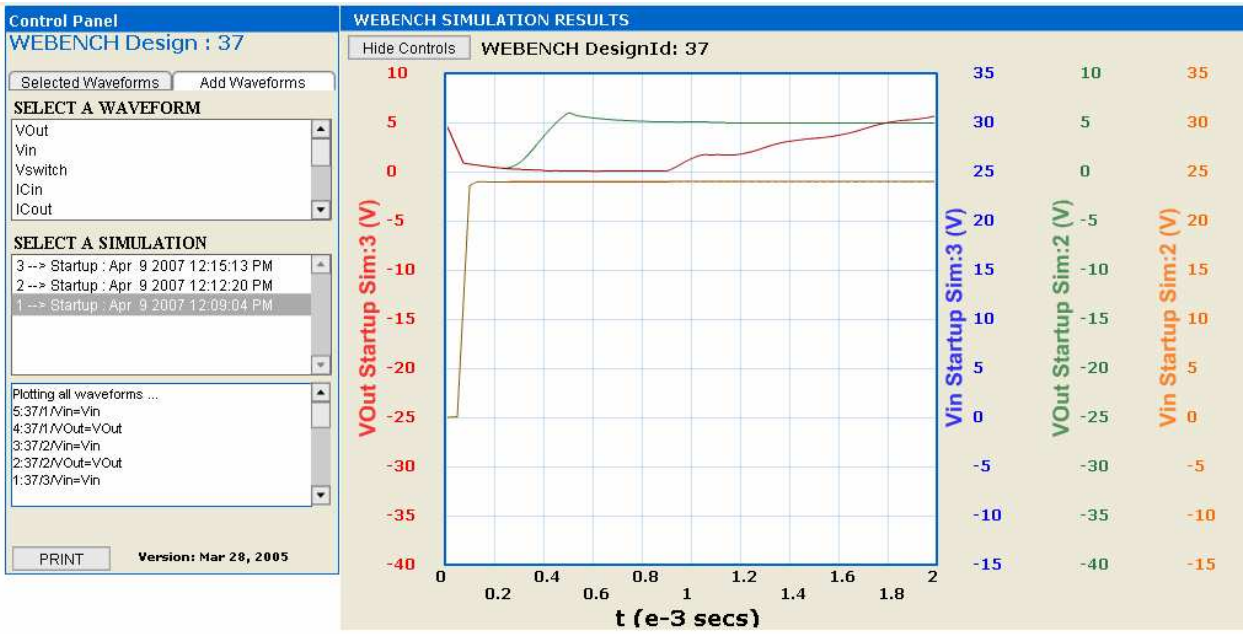
With C_{SS} = 4.7 nF it takes 1.8 milliseconds for V_{OUT} to reach 5 volts.

Now, click on the C_{SS} capacitor in the schematic. From the Select Alternate Component C_{SS}, select the custom bullet and enter a capacitance value of 1nF. After selecting the new component click the "Update BOM" button. Now, rerun the start up simulation with the new C_{SS} component.



The previous plot shows the startup simulation with C_{SS} = 1 nF. It can be seen that the time to reach 5 volts is now 0.5 milliseconds.

From this screen, open the Add Waveform window and select the previous Startup simulation in order to view both plots side by side.

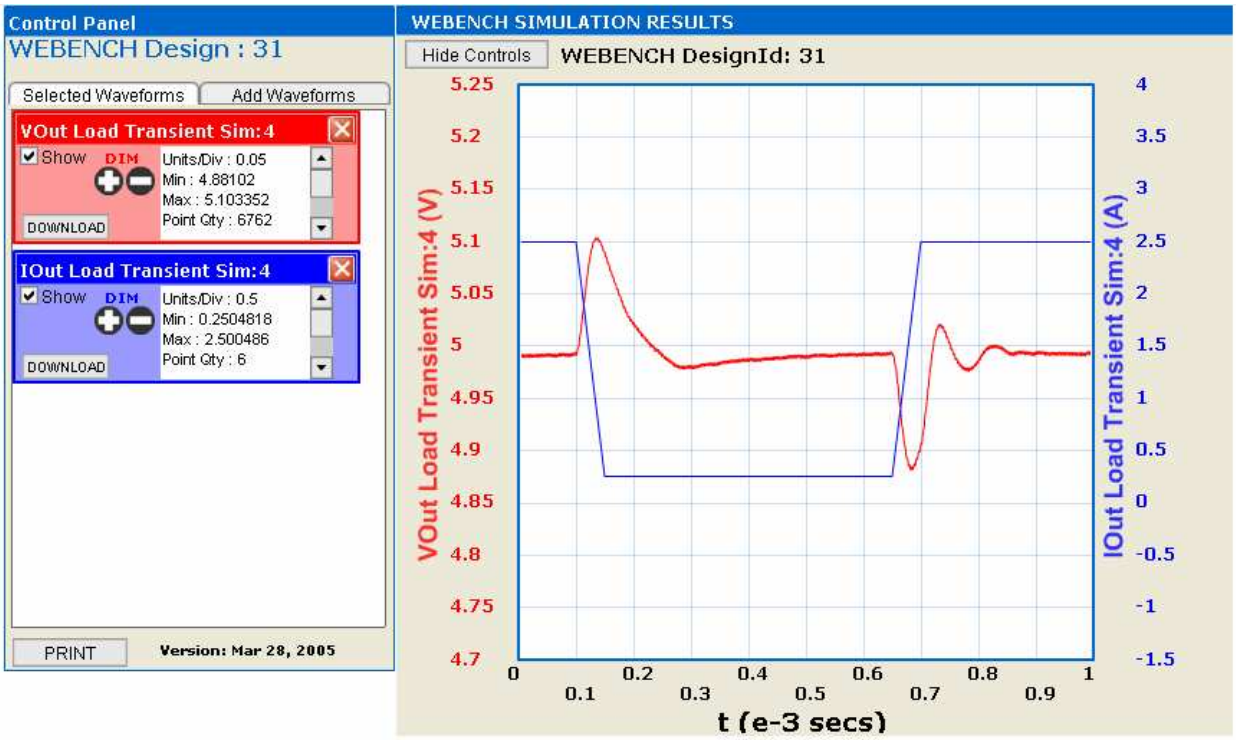


The green line shows V_{OUT} for C_{SS} = 1 nF and the red line shows V_{OUT} for C_{SS} = 4.7 nF.

It can be seen that the time to reach 5 volts is decreased from 1.8 milliseconds to 0.5 milliseconds by reducing the value of C_{SS}.

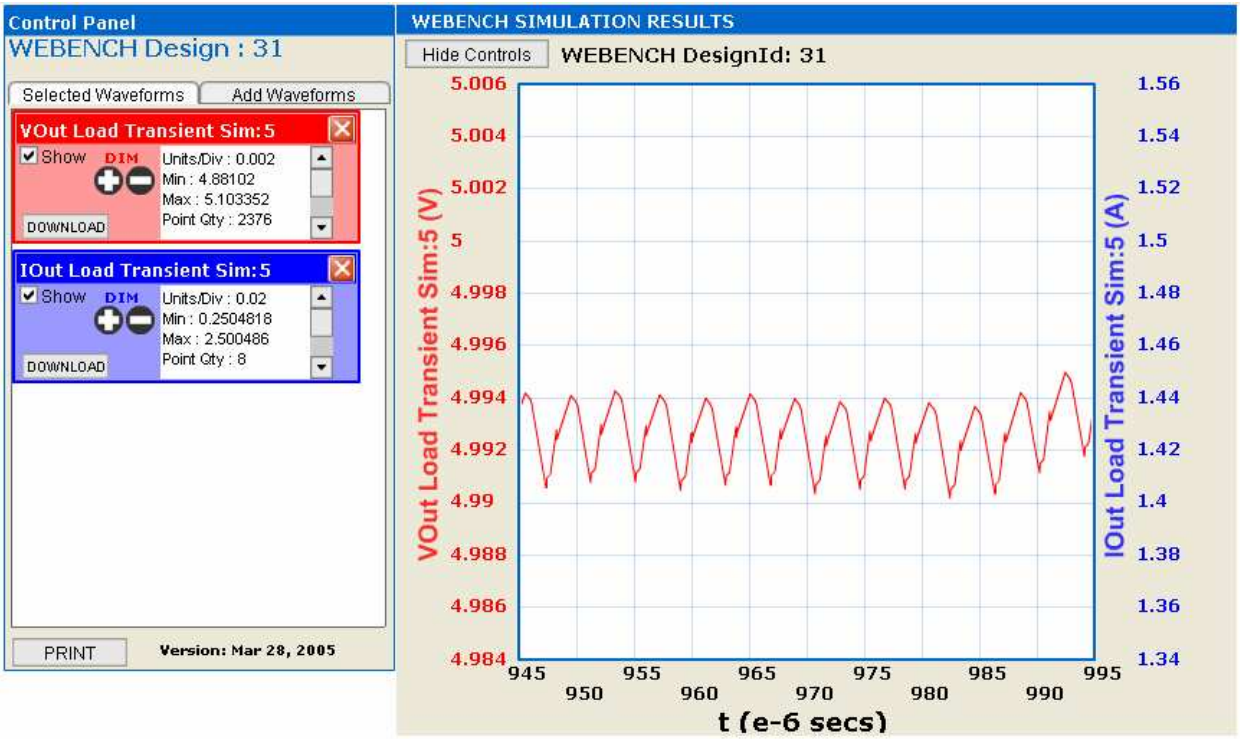
Load Transient

Next, the Load transient will be investigated. In the "Select Simulation Type" choose Load Transient and click the Start New Simulation button.



Here both the load transient pulse in blue and the corresponding V_{OUT} waveform in red can be seen. There is an overshoot of about 100 mV when the load current is falling and an undershoot of a slightly smaller amount when the load current is rising.

Zoom in on a section of the waveform by clicking and dragging with the mouse to get a closer look at the peak-to-peak change in voltage.

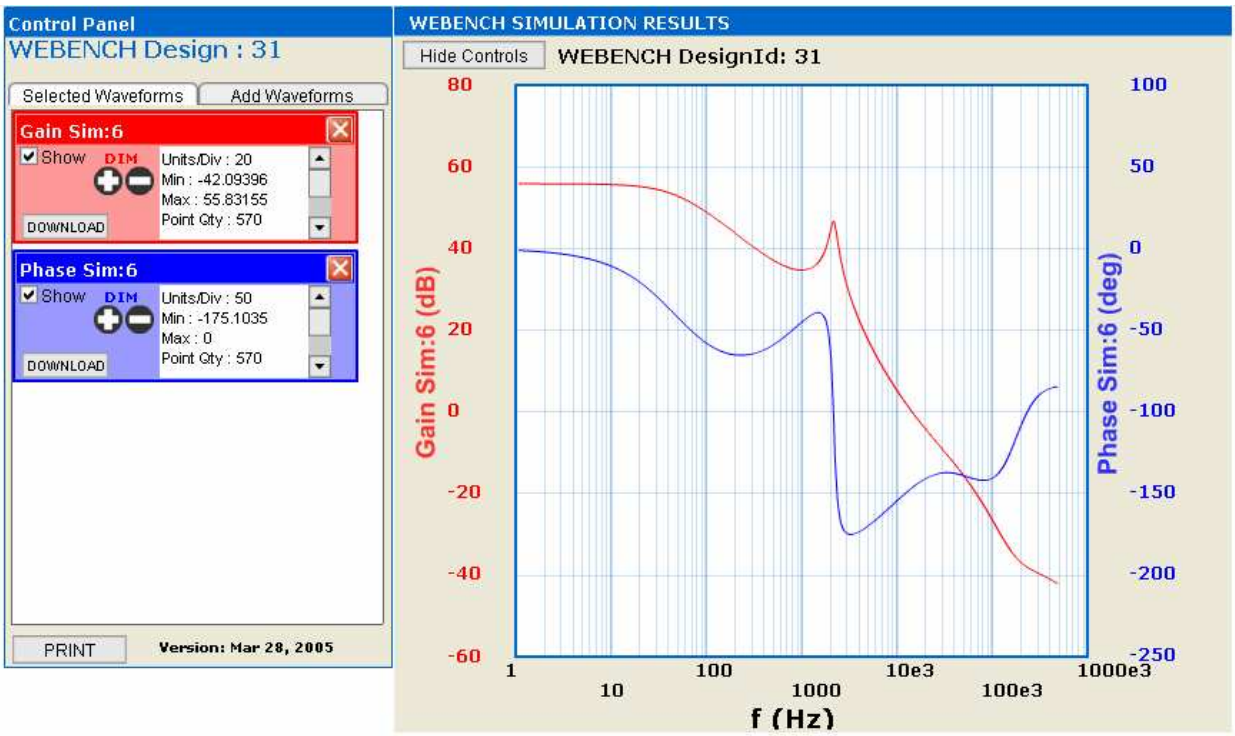


In the zoomed-in view, the peak-to-peak output ripple at full load can be estimated, to be less than 4 mV.

Bode Plot

The focus will now be on the Bode plot function. Bode plot is an important tool to examine the stability of a design. In the "Select Simulation Type" choose Bode Plot and click the Start New Simulation button.

-The Bode Plot shows the phase and gain on the same graph plotted vs. frequency.
-The phase margin should be at least 25 degrees but preferably 45 degrees.
-The phase margin is the difference between the phase and -180 degrees measured at the point where the gain = 0 dB (crossover frequency)
-The phase is not of concern when the gain drops below zero.
-If the phase approaches -180 at frequencies below crossover and it comes back up, that is conditional stability which is acceptable as long as the phase is good at the crossover frequency.



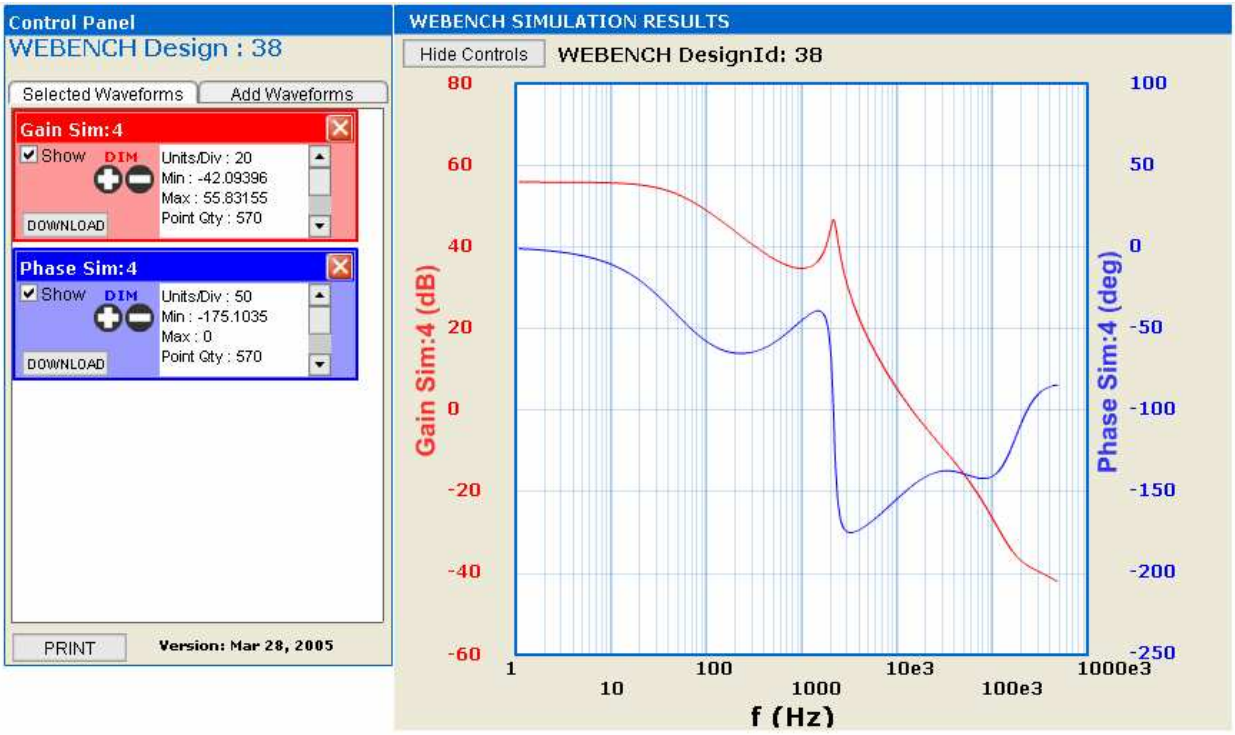
The crossover frequency is the frequency at which the gain reaches unity gain at 0db. To measure the phase margin, we get the phase at the crossover frequency and subtract 180 degrees. Here the crossover frequency is 50 kHz. At that frequency the phase is -139, so the phase margin is -139 – (-180) = 41 degrees. .

Vary C_{OUT}

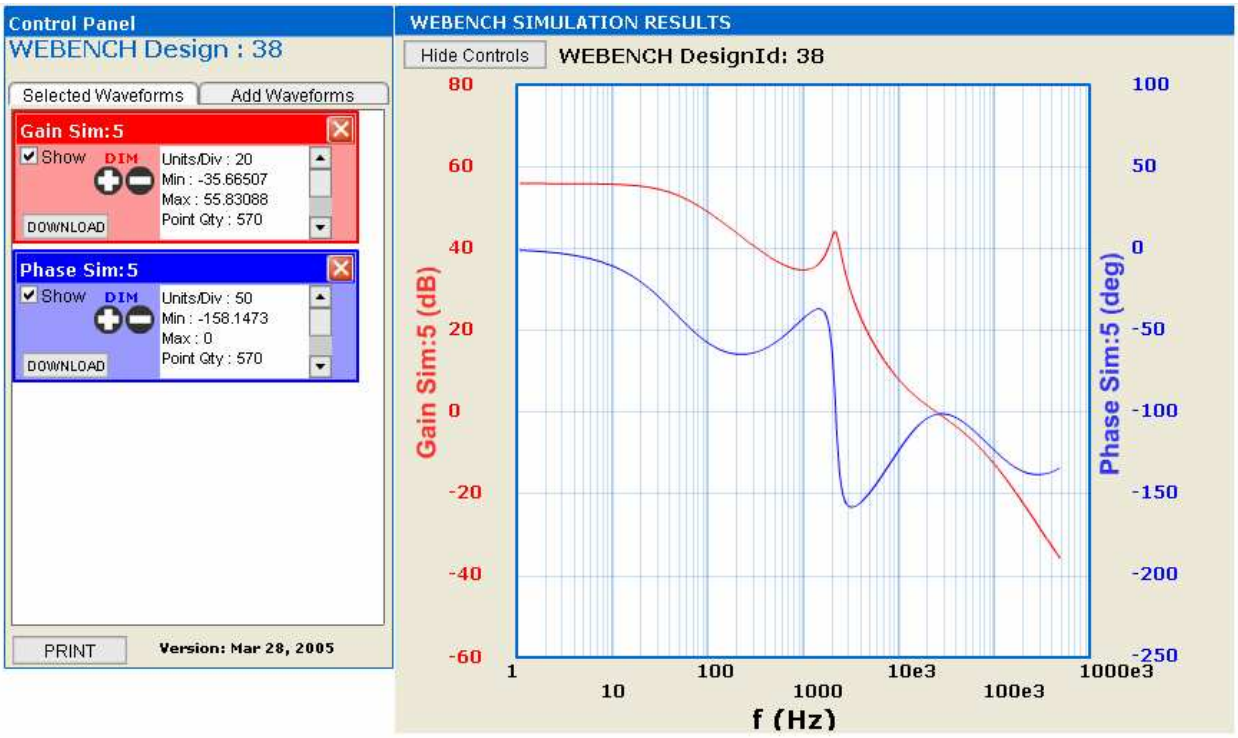
Evaluate effects of Equivalent Series Resistance (ESR) on stability

Next, the effect of output capacitor ESR on the circuit will be investigated. We will compare capacitors with ESR of 4 milliohms and 40 milliohms. The C_{OUT} capacitor initially assigned has 4 milliohms of ESR.

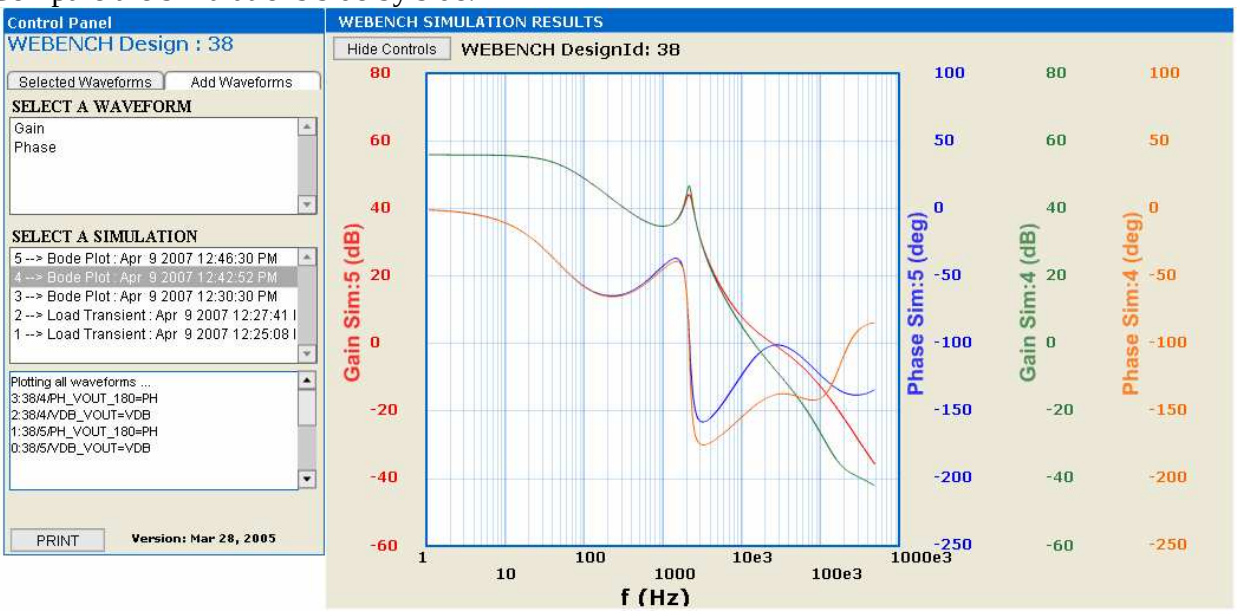
The bode plot just created is the initial scenario, as pictured below:



Next, create a custom C_{OUT} capacitor with an ESR value of 40 milliohms by clicking on the C_{OUT} capacitor on the schematic. Select the bullet for custom and then set the resistance to 0.04, but set the other parameters to the same as the original C_{OUT} values. Create a new bode plot (the capacitance should remain the same).



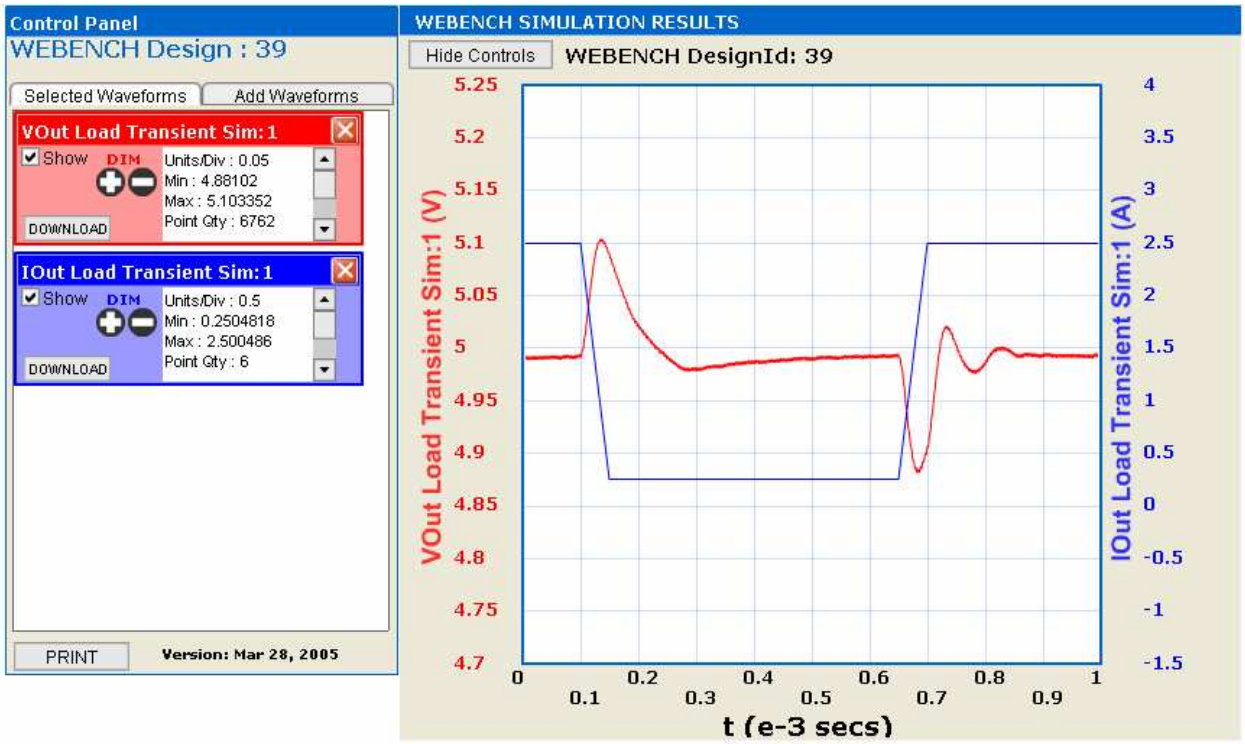
Compare the simulations side by side.



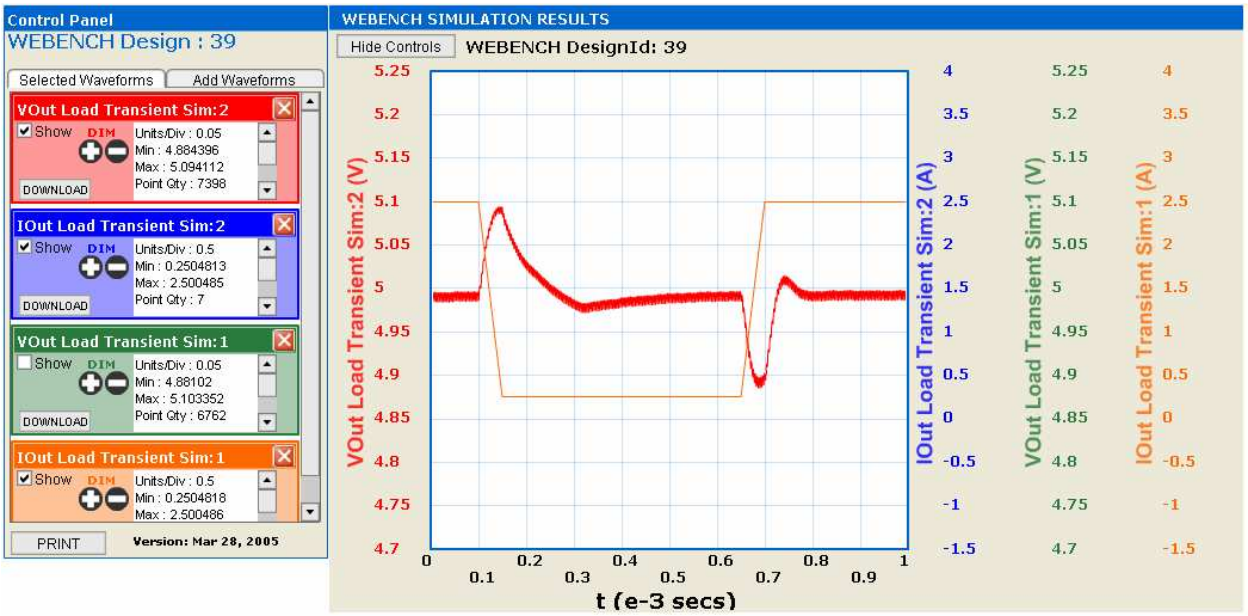
This is a WEBENCH Bode Plot showing different output capacitor ESRs. Both simulations show a dip in the phase at about 3kHz. This is called conditional stability. From the plot the conditional stability issue can be improved by lowering the ESR of the output capacitor. This also increases the crossover frequency and bandwidth.

Effect of Cout on load transient

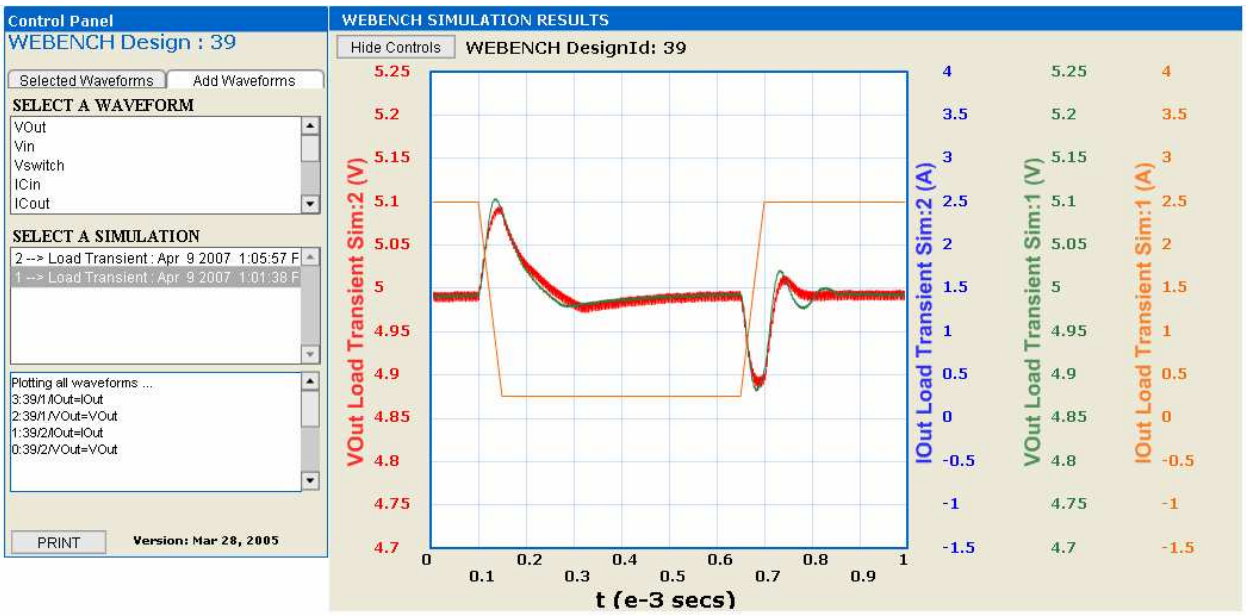
The effect of raising the C_{OUT} ESR on the output voltage during a load transient test will now be examined.



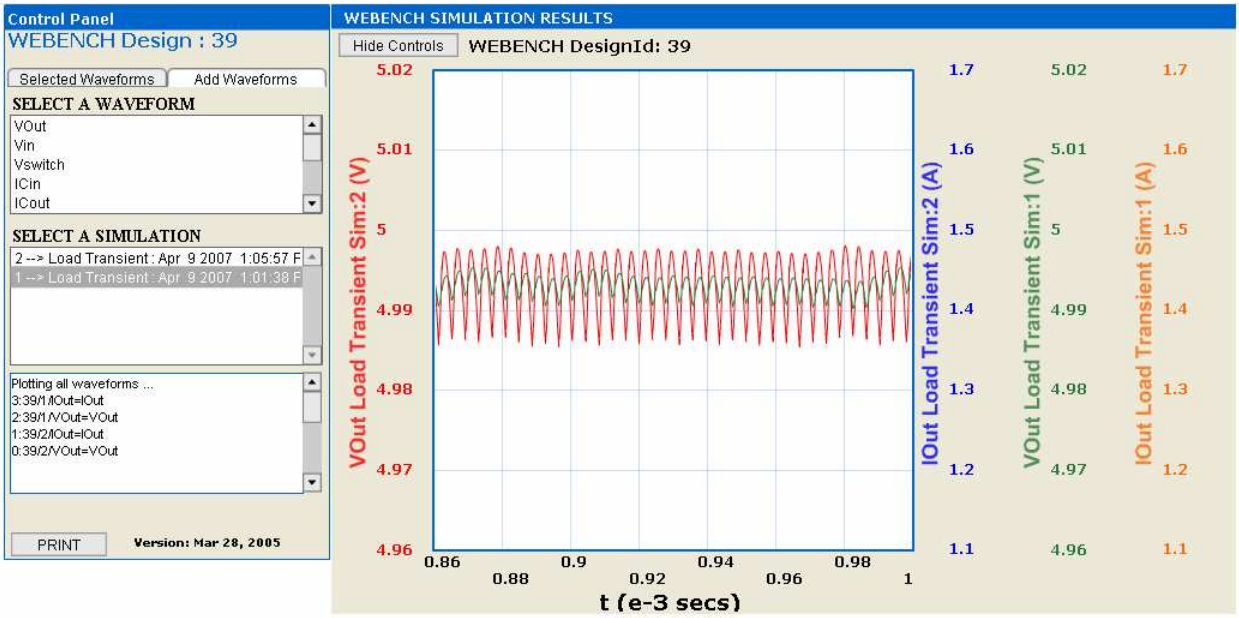
This simulation shows the initial Load Transient simulation where C_{OUT} ESR = 4 milliohms.



This simulation shows the initial Load Transient simulation where C_{OUT} ESR = 40 milliohms.



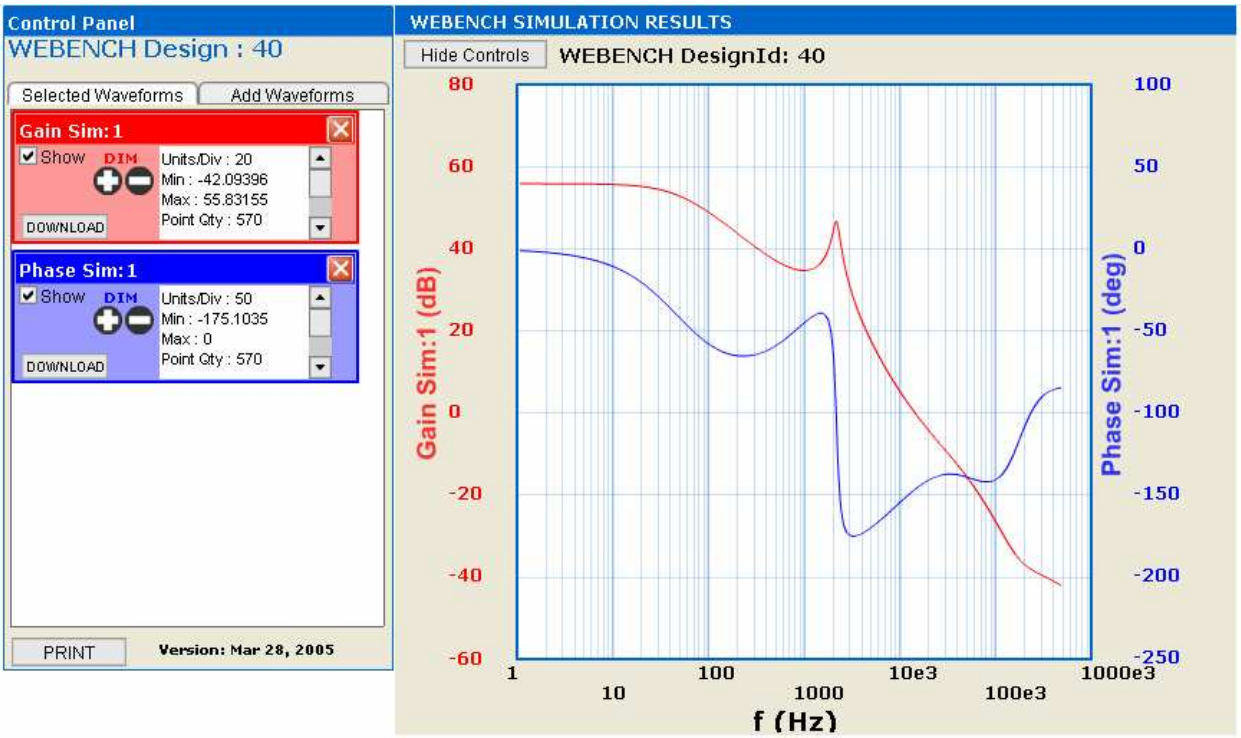
The green waveform represents V_{OUT} with the initial capacitor of lower ESR. The overshoot as the current ramps down has decreased slightly and the undershoot has increased slightly.



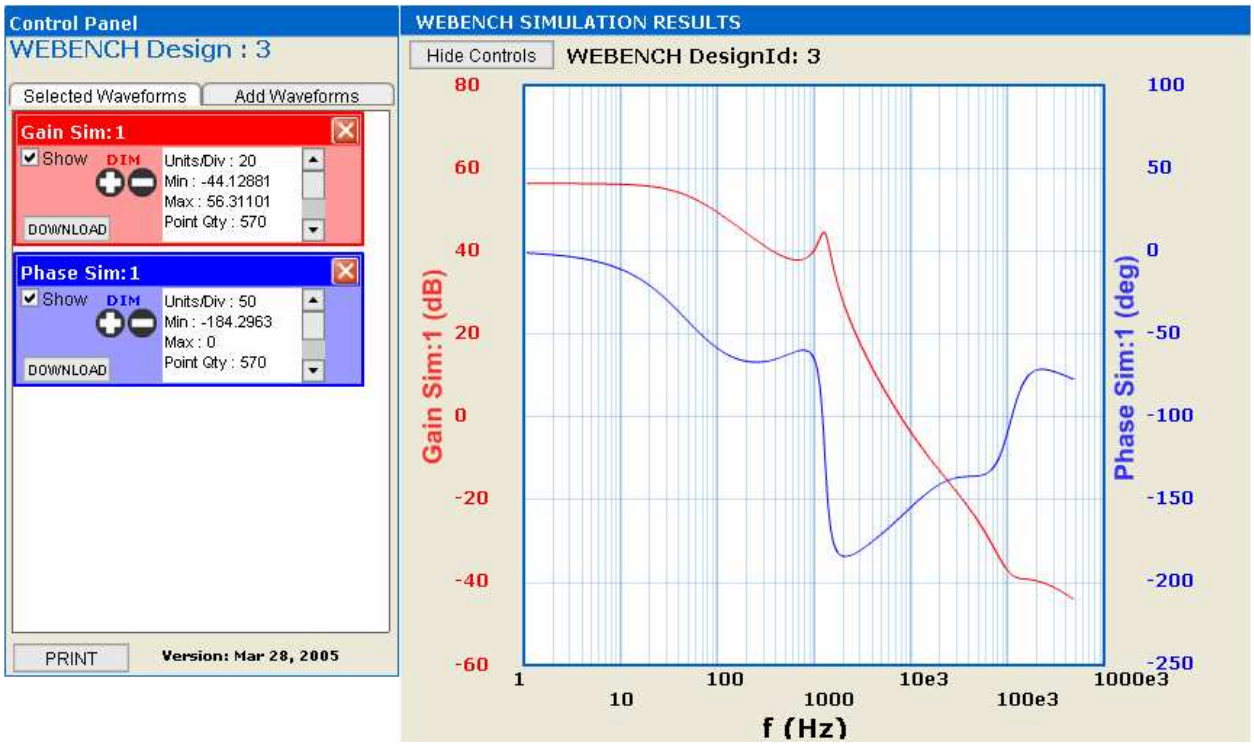
The other effect of changing the output capacitor is that the voltage ripple will change. The ripple has increased with increasing ESR on C_{OUT} from approximately 3 mV to 15 mV peak to peak.

Vary Inductors

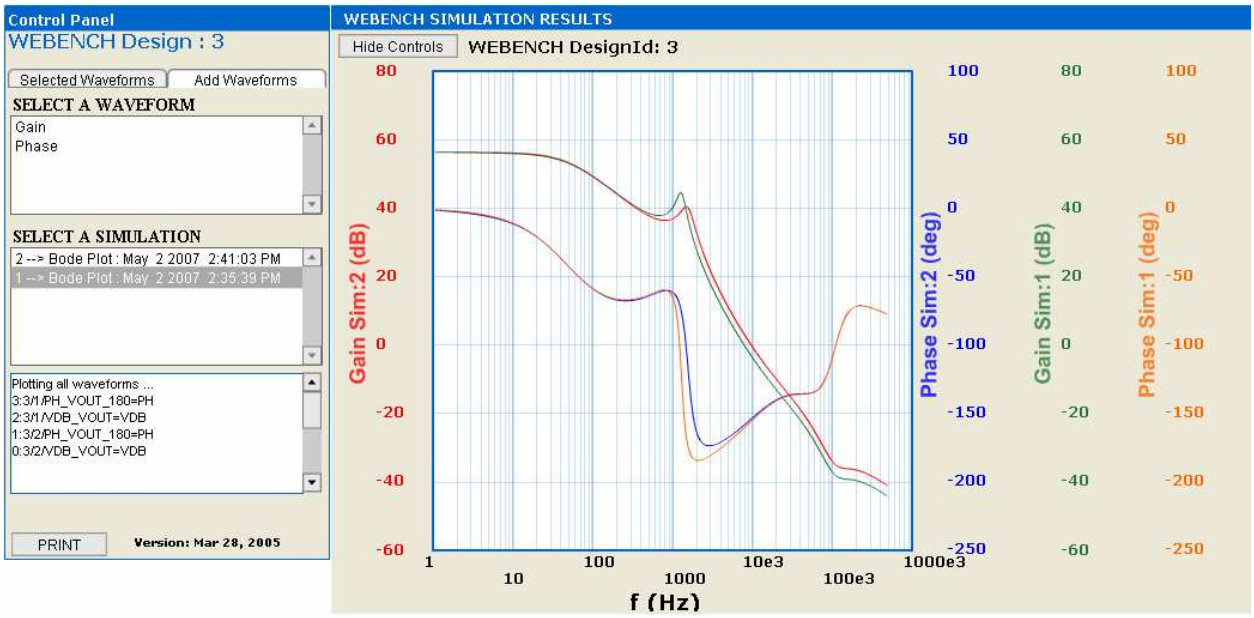
Next, we will investigate the effect of inductance on our design. Again, run two bode plot simulations: one using a 33 µH inductor and another using a 47 µH inductor.



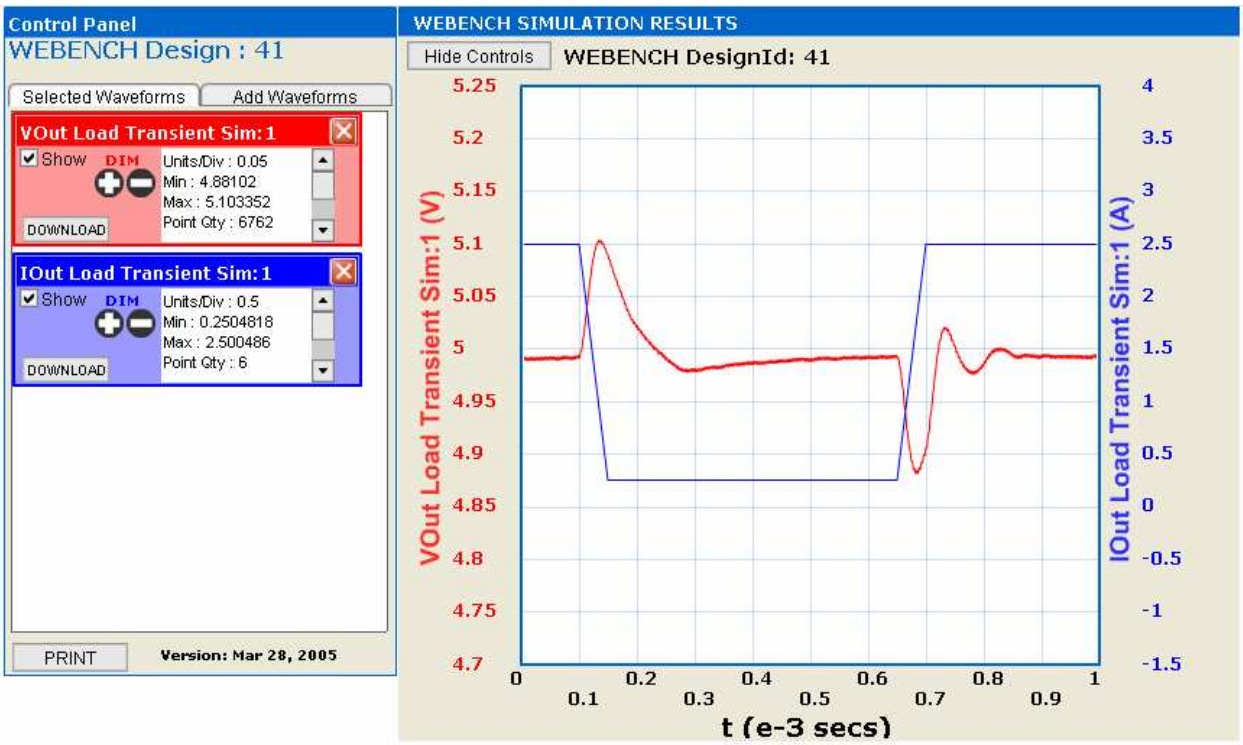
Bode plot for L1= 33 µH.



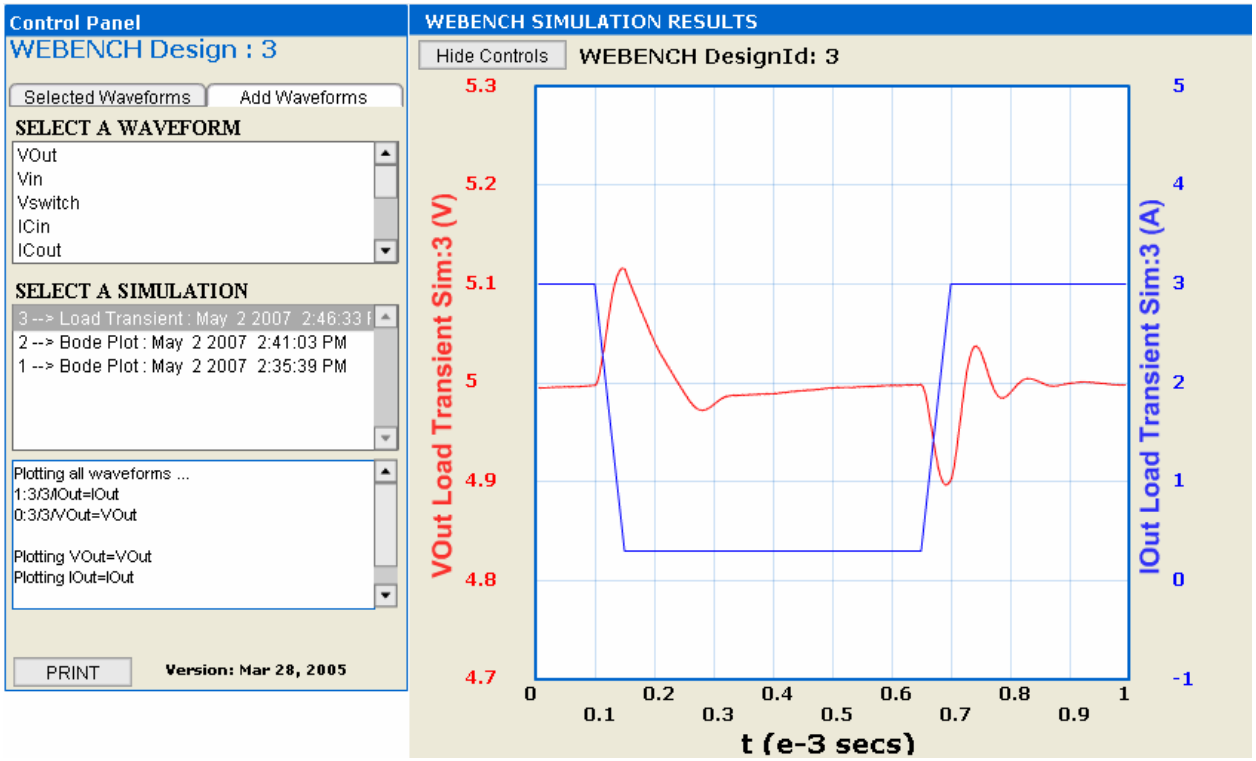
Bode plot for L1 = 47 µH



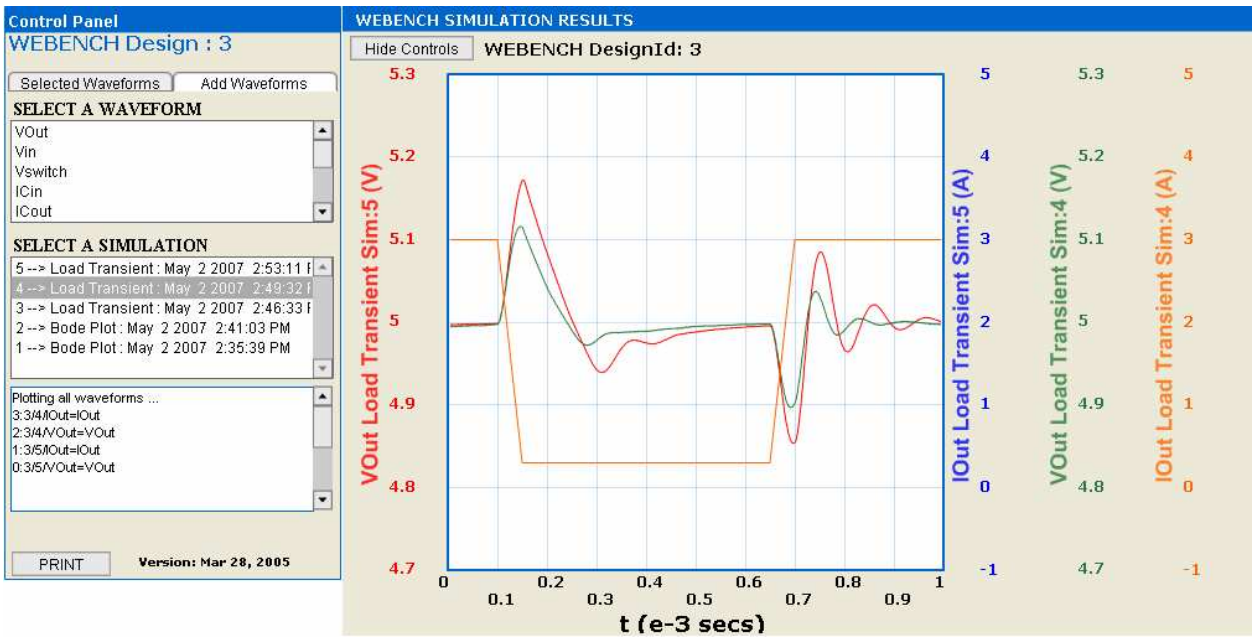
The red and blue lines correspond to the 47 µH while the green and orange to the 33 µH. The phase can be raised at the lower frequencies by decreasing the inductance. However, this may cause a problem with the peak switch current and V_{OUT} ripple.
Now, explore the effect on load transient for the two inductances.



Load transient simulation for L1 = 33 µH

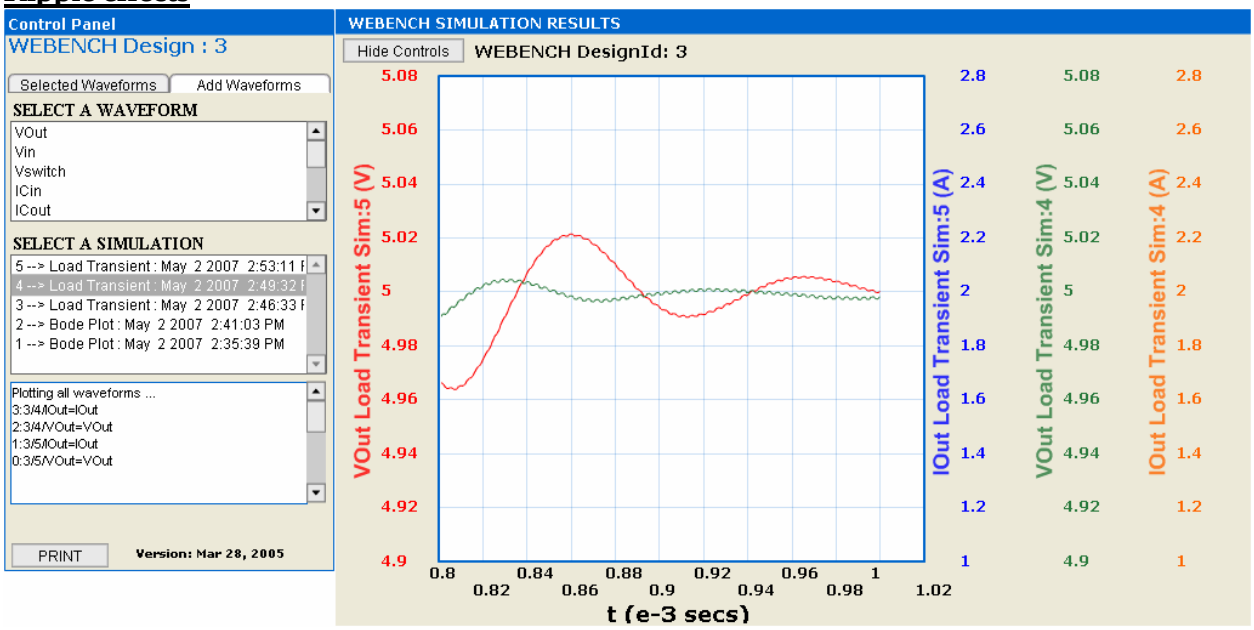


Load transient simulation for L1 = 47 µH



The load transient response is plotted for the two inductances. The green line corresponds to the 47 µH inductor while the red line represents the 33 µH inductor. For this design, the 33uH value results in less excursion during the load transitions.

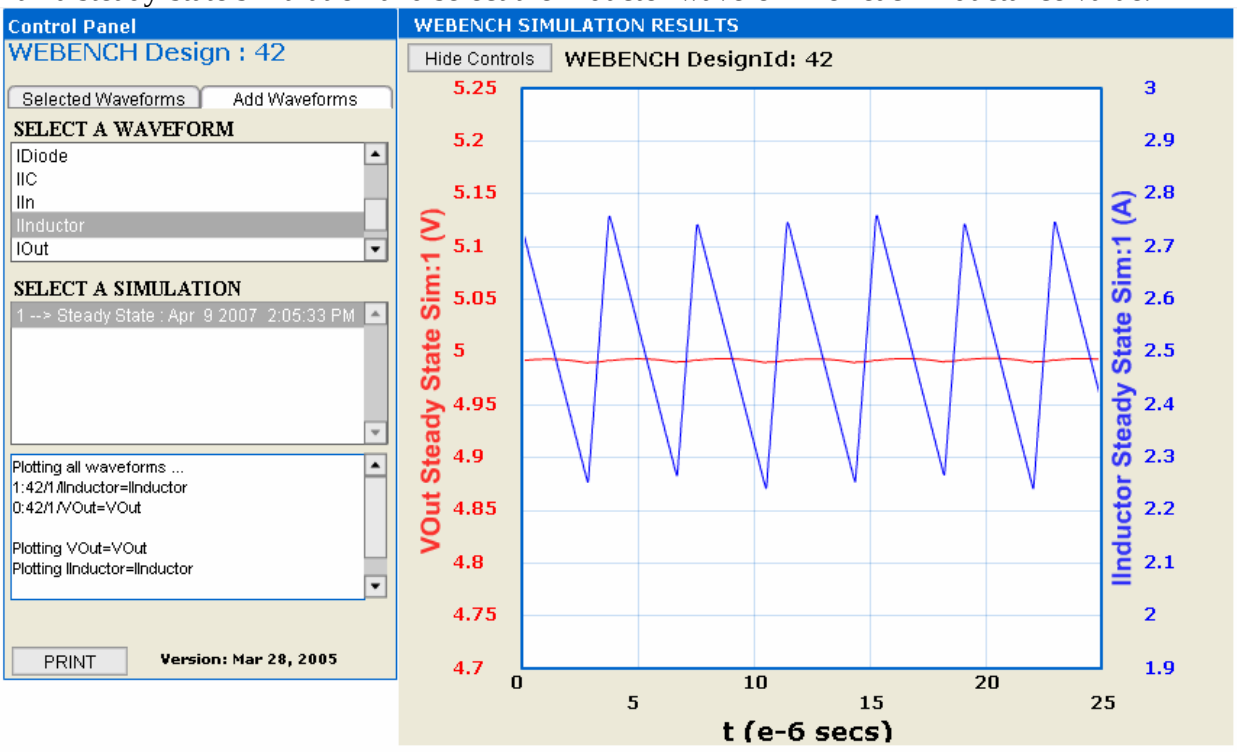
Ripple effects



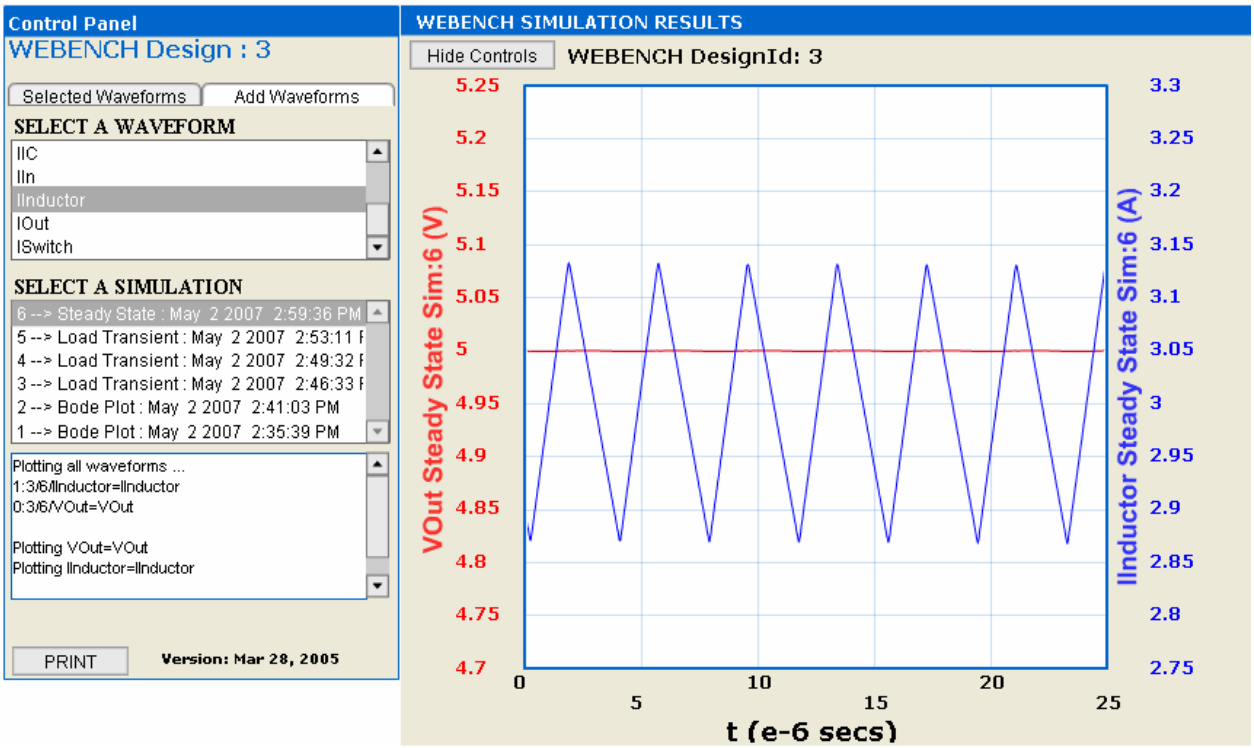
Effect of inductance on inductor/switch ripple current

Now, view the peak current across the inductor.

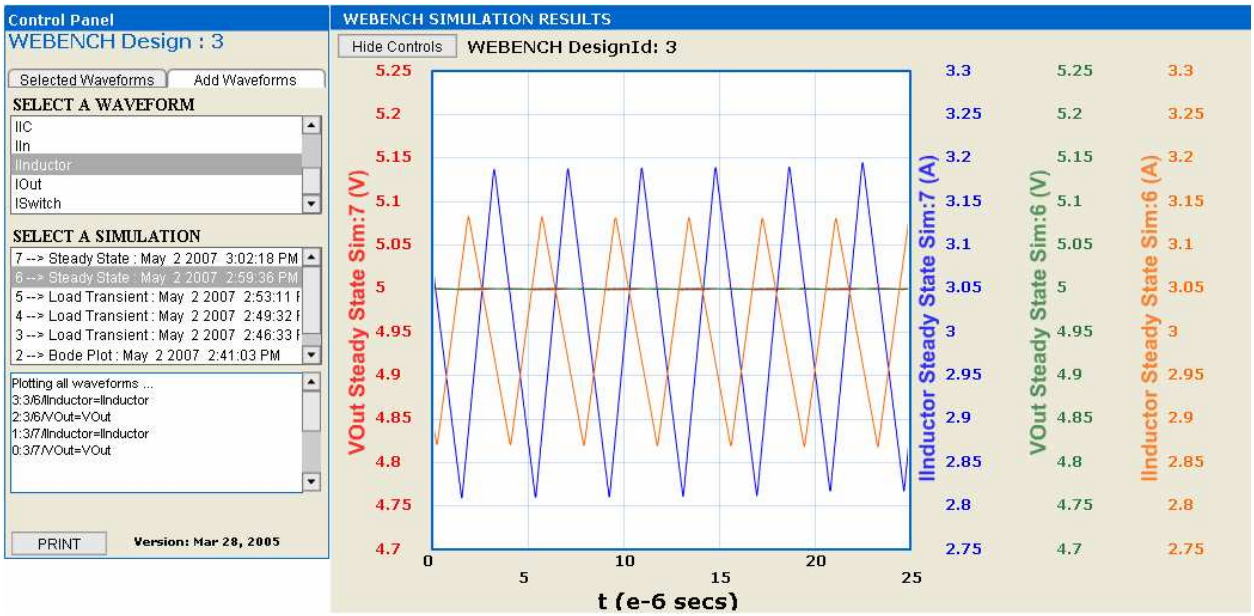
Run a steady-state simulation and select the Inductor waveform for each inductance value.



Inductor current during steady state for L=33µh



Inductor current during steady state for L = 47 µH.



Notice that the peak-to-peak inductor current, I_{LPP}, is reduced from .375A to .25A by increasing the inductor from 33µH to 47µH. The peak inductor current was also reduced from about 3.2A to about 3.125A.

This follows since:

$I_{LPEAK} = I_{LAVERAGE} + .5ILpp$ where $I_{LAVERAGE} = I_{OUT}$ (assume L is ideal).

Since V_{OUT} ripple = inductor ripple current * C_{OUT} ESR

Higher inductance means a lower V_{OUT} ripple. The trade off is a larger footprint and a higher cost.

Question/Problems

Design a power supply with the following specifications.
V_{IN} max = 18, V_{IN} min = 8, V_{OUT} = 5, I_{OUT} max = 2.5

Select the LM2673-5.0
How much does the IC cost? _____
Compared to other similar devices? _____
What is the operating frequency? _____
What is the current rating? _____
What is the typical efficiency? _____

Investigate the effect of C_{SS} on your design
Use alternate C_{SS} components and comment on the effects of V_{OUT}?
Css1: Capacitance: _____
Range in cost: _____
Manufacturers: _____
Time to reach V_{OUT}: _____

Css2: Capacitance: _____
Time to reach V_{OUT}: _____

Use start-up simulation and show each C_{SS} simulation on the same plot.

How does changing the capacitance of C_{SS} affect V_{OUT}?

Investigate the effect of ESR on your design.
Use the Load Transient simulation to display the load transient pulse and the voltage output response.

Comment on the change in voltage during the rise and fall of the current pulse.

What is the peak-to-peak voltage output ripple at full load?

Use the Bode Plot simulation to show the phase and gain vs. frequency.
What is the crossover frequency? _____
What is the phase margin? _____

Use alternate components for C_{OUT} to investigate effects of ESR.

Cout1:	ESR	_____
	Range of cost	_____
	Manufacturer	_____
	Crossover frequency	_____
	Phase margin	_____
	I_{OUT} peak ripple	_____
Cout2	ESR	_____
	Range of cost	_____
	Crossover frequency	_____
	Phase margin	_____
	I_{OUT} peak ripple	_____

Run Bode plot simulations for each C_{OUT}, and display on the same plot.

Comment on the effects of phase margin, the crossover frequency and bandwidth with various ESR's.

Use load transient simulations to see the effects of changing C_{OUT} has on the voltage output response.

How is the overshoot and undershoot effected?

Show the various simulations of each C_{OUT} on the same plot.

How is the voltage ripple affected?

Investigate the effect of inductance on your design.

L1_1:	Inductance	_____
	Manufacturer	_____
	Range in cost	_____
	IL_{PEAK}	_____
L1_2:	Inductance	_____
	Manufacturer	_____
	Cost	_____
	IL_{PEAK}	_____

Show bode plots for each inductor.
L1_1: 33µH

L1_2: 47µH

How is the phase effected?

Comment on the effects of the V_{OUT} load transient during the rise and fall times of a current pulse. How is the V_{OUT} ripple affected for various inductances?

Use the steady state simulation and display the current across L1 in steady state.

How is the peak current across the inductor changed? _____
How is the V_{OUT} ripple affected? _____

What should be considered when using alternate inductances? _____

How much does an LM2673-5.0 evaluation board cost? _____
How does this price compare to other switching regulators offered by *National* and competing retailers? _____

WRITTEN REPORT:

When writing the report, answer all questions posed throughout this lab.

Written Report shall include:

- Cover page
- Purpose
- Answers to questions
- All Necessary WEBENCH plots
- Conclusion