Lecture 50
Changing Closed Loop Dynamic Response with Feedback and Compensation

A. Closed Loop Transient Response Waveforms
   1. Standard Quadratic T(s) Step Response
      a. Q > 1/2 Oscillatory decay to a step
      b. Q < 1/2 Exponential decay to a step
      c. Q = 1/2 Goldilocks solution critically damped

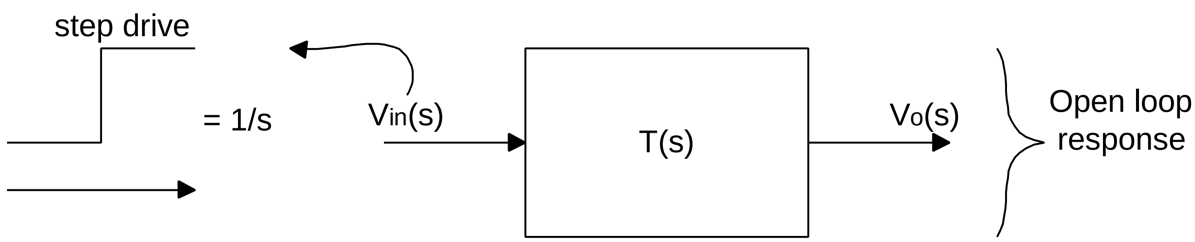
B. Feedback Review
   1. $(Z_{out})_{\text{closed loop}} = \dfrac{Z_o(\text{open loop})}{1+T}$, Z_{out} varies with f
   2. $(G_{vg})_{\text{closed loop}} = \dfrac{G_{vg}(\text{open loop})}{1+T}$, G_{vg} (f)
   3. Closed Loop Response Time
      $\Delta t = 1/2p\, f_c$ (T(s) cross over) f_C is at T(s) unity gain
   4. Limitations on Transient Overshoot
      a. V_{pk}/I_{pk} are f(Q) and Cause Damage
      b. Approximating Q for the two nearby poles T(s) Unity Gain Cross-over case
      c. ϕ_m Tailoring via $G_c(s)$

C. Compensation Networks To Tailor T(s)
   1. Overview of G_c (Alterations Tailoring)
   2. Lead Compensator in $G_c(s)$ PD Compensator

Lecture 50
Changing Closed Loop Dynamic Response with Feedback and Compensation

A. Transient Waveforms in Time Domain

1. Standard Quadratic System Response



$$T(s) = \frac{1}{1 + \frac{s}{w_o Q} + (\frac{s}{w_o})^2}$$

We find f_0(L-C resonance frequency) and f_C(unity gain of T(s) crossover frequency) of T(s) are sometimes related. Erickson shows that for a SPECIAL case of quadratic open loop gain $T(s)= 1/ s/\omega_0(1 +s/ \omega_2)$ we find that the two poles of T(s) are f_0 and f_2 and the crossover frequency of T(s) is related as $\frac{f_o}{f_c} = \sqrt{\frac{f_o}{f_2}}$.

For this case $Q=(f_0/f_2)^{1/2}$. In the low Q case there is no "Q peaking" but in the high Q case there is and $Q=f_0/ f_C$. Next we generalize.

a. Q > 1/2 Oscillatory Decay to Unit Step Input

For a general second order system as described above the unit step response (or transient response) of the closed loop second order system T/ (1+T) is such that both poles lie close to f_0:

$$\hat{v}(t) = 1 + 2Q \frac{e^{-w_c t/2Q}}{\sqrt{4Q^2 - 1}} \sin\left[\frac{\sqrt{4Q^2 - 1}}{2Q} w_c t + \tan^{-1}(\sqrt{4Q^2 - 1})\right]$$

v(t) is oscillatory in time for Q>1/2 and for Q<1/2 is exponential. For Q>1/2 the **peak value is 1+ exp(+/- p/ $(1-4Q^2)^{1/2}$ The peak V may cause problems for solid-state devices in circuits with**

T(s). That is even brief peak values can destroy devices.

b. Q < 1/2 Step Output of T/ (1+T) is exponential

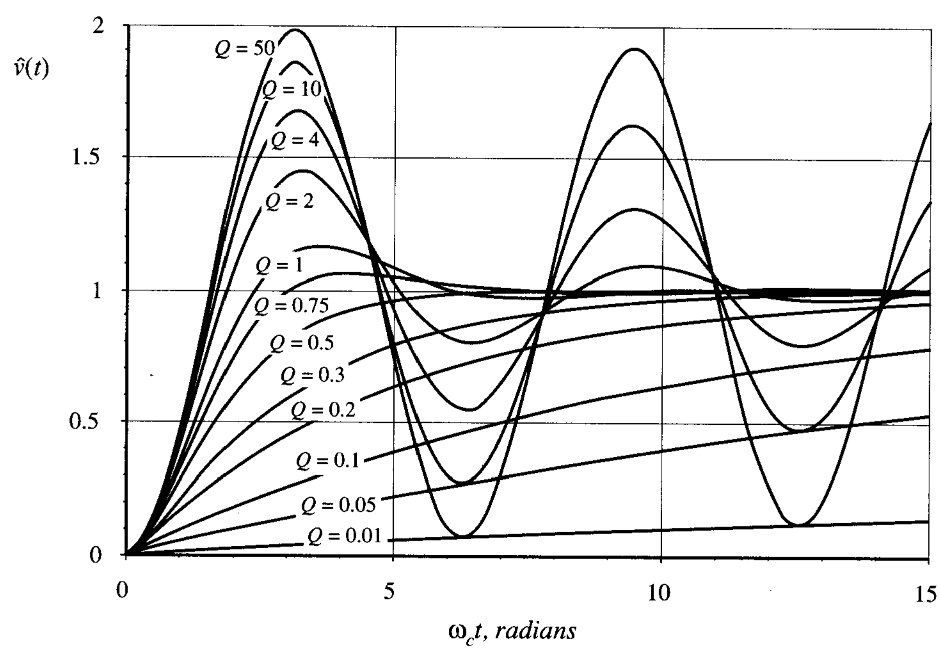
The poles of T/ (1+T) are well separated in frequency as compared to to the case for Q>1/2.

Roughly speaking we find: $\omega_1 = Q\omega_c = 2\pi f_C$, $\omega_2 = \omega_c/Q = 2\pi f_2$

$$\hat{v}(t) = 1 - \frac{w_2}{w_2 - w_1} e^{-w_1 t} - \frac{w_1}{w_1 - w_2} e^{-w_2 t}$$

$$w_1, w_2 = \frac{w_c}{2Q}\left(1 \pm \sqrt{1-4Q^2}\right)$$

The plots of the T/ (1+T) response to a step input are summarized below for your perusal. Note the oscillatory and damped conditions vary with the resulting "Q" of the original T(s).



c. For Q =1/2 the two pole locations of T/ (1+T) are roughly f_1 and $f_2 = 4 f_1$: Critically Damped Case

The critically damped case separates the two sets of transient solutions to T/ (1+T) of one, oscillatory sine waves and two, decaying exponentials. We term this the critically damped case. In the approximation that,$f_{lower} = 10^{-1/2Q} f_0$(of the L-C resonance $=1 / 2\pi (LC)^{1/2}$,we find the lower frequency pole location in the critically damped case to be.

$f_{lower} = f_0 / 10$ WHAT about f_{higher}??

. Below we consider three cases for Q in the open loop responseT(s) and the overview of the different closed loop transient responses. Q< ½ is considered OVERDAMPED and Q>1/2 is considered to be UNDERDAMPED.

Q < 1/2	**Q = 1/2**	Q > 1/2
$Q = \sqrt{\frac{f_o}{f_2}},\ f_2 \geq 4 f_o$	**critically dampe**d	Underdamped
	NO OVERSHOOT	$v_{peak} = 1 + e^{-p/\sqrt{4Q^2-1}}$

Q=1, V_{PEAK} =1.16 V_{IN}

$w_1 = Qw_0$ at low f causes slow response of the closed loop system

Q=2, V_{PEAK} =1.44 V_{IN}

for 3.3V Pentium Q = 2
V_{max} = 4.7V ok?
Any Problems for the IC???

$\Delta t = \frac{1}{2 f_o}$ for 82%

Δt= 1/ 2 $f_{CROSS-OVER}$

For 82% rise

$\Delta t = \frac{1}{f_o}$ for 98.6% of rise

$\Delta t = \frac{1}{f_c}$ for 98.6 % rise

Goldilocks solution of fastest response without overshoot, Dt = 1/ f_C

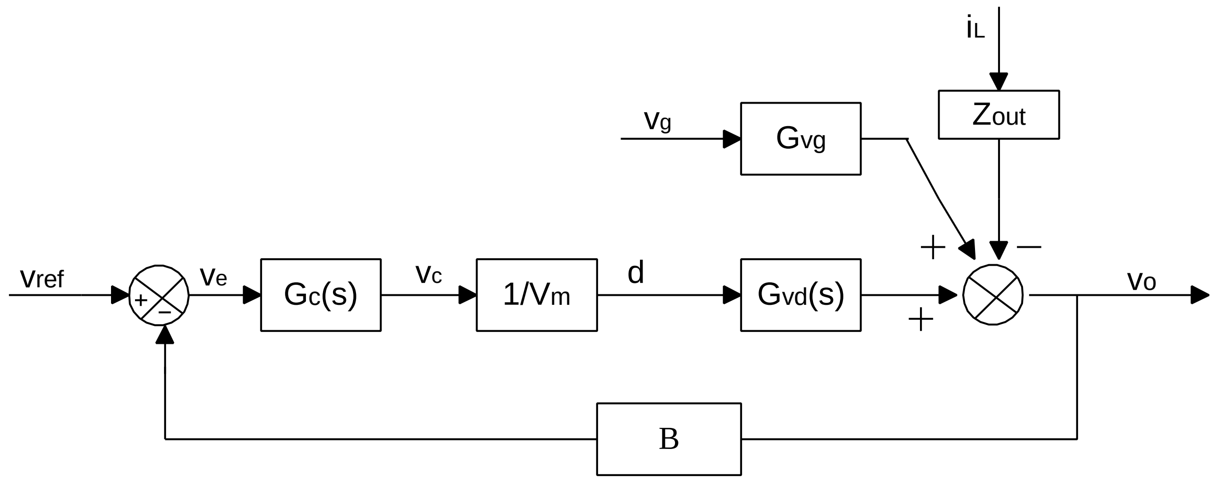
We term f_C as the unity gain cross-over frequency of T(s). It is easily measured or calculated from the model. **It also turns out to be the cross-over frequency, f_C, for both T/ (1+T) and 1/ (1+T). Hence f_C sets response time.**

We next consider the issues involved with open-loop T(s) in a general feedback loop and how we wish to tailor T(s) versus frequency to attain a variety of goals for the closed-loop system with feedback. In general we wish the highest f_C possible so that we have a quickly responding system to any transient disturbances. The practical limit to f_C is roughly 1/5 of thew switch frequency of the converter, f_{SW}. If we have f_C above this we may inadvertently amplify the switch ripple and cause instability.

B. Effects of Feedback on Converters: A Review

We place feedback around a converter with open-loop gain,T(s), in order to achieve a better converter. In particular we improve the output impedance by 1/(1+T), we improve G_{VG} by 1/ (1+T).

We can also improve the closed loop response, T/(1+T), by increasing the unity gain cross-over frequency of an already existing T(s). We do this by placing compensation networks in series within the loop gain. Hence the transient response in closed loop is made faster by compensation. We must be careful to tailor the "Q" of the new T(s) so that we do not cause too much overshoot or ringing during the transient response. Peak values can kill solid state devices rapidly. We also must also not cause closed loop stability problems by having too low a phase margin in new T(s) plots. This is an exercise in tradeoffs. Key to success of compensation networks is careful analysis of the old and new T(s) Bode plots as shown below. Compensation tailors the open loop response, T(s) to achieve the best set of closed-loop goals. Large values of T at the mains(50 –60 Hz and harmonics) frequencies will reduce G_{VG} (output to line voltage variations) as well as reduce the output impedance by a factor 1/ (1+T). That is the reduction occurs only when T is large. However, large T at low frequency might mean too high values of f_C causing inadvertent amplification of the switch frequency of too low a phase margin resulting in oscillation. We will see that as designed phase margins of 76 degrees are safe but we often push phase margin as low as 30 degrees due to temperature and aging effects. Even at thirty degrees the converter may break into periods of oscillation when large transients are experienced. The feedback converter is shown below with the associated variables and transfer functions.



$$\hat{V}_{out} = \frac{\hat{V}_{ref}}{b}\frac{T}{1+T} + \frac{\hat{V}_g\ G_{vd}(s)}{1+T} - i_L\frac{z_o}{1+T}$$

Where the open loop gain $T = b\dfrac{G_c}{V_m}G_{vd}$ in the control to output loop has contributions from the feedback ratio(β) the compensation network (G_C) and the control to output transfer function of the converter topology chosed(G_{VD}). **Note that G_C is a separate block containing the compensation network that will tailor T(s) from what it is without compensation to what it will become with compensation in order to achieve closed-loop capabilities**. It often employs an op-amp circuit.

1. Effect of Δi (load) over a frequency range: $f_{min}<f<f_{MAX}$

$$\frac{\Delta V_{out}}{\Delta i_{load}} = \frac{-Z_{out}(\text{open loop})}{1+T}$$

↓

↓ **if z_{out} (open loop) cannot be made small enough in a frequency range we want for our design then what ??**

Z_{OUT} specification. we seek over a given frequency range

Note now that by clever use of compensation networks, G_C we Can tailor the amplitude of T in specific frequency regions.

$f_{min} \leq f \leq f_{MAX}$ **increase 1+T by compensation of T(s) over f_{min} £ f £ f_{MAX}**

Usually we easily achieve low Z_{OUT} at f< f_C, but not at f>f_C. WHY?

2. Effect of DV$_g$(input voltage) on the Converter Output

Usually V_g is a very crude rectified ac, with lots of variations especially at 120, 180 Hz etc. Below we consider Europe or Japan where the mains power is at 50 Hz and the harmonic ripple is at 100 Hz. The effect of the ripple is reduced by feedback.

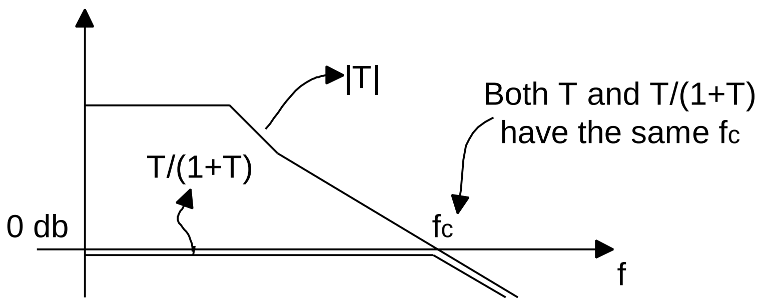
$$\frac{\Delta V_{out}}{\Delta V_g} = \frac{G_{vg}}{1+T}$$

$$\downarrow \qquad \downarrow$$

Usually the Spec of $\leftrightarrow \dfrac{G_{vg}(100)}{1+T(100)}$ is given as “x” % @ 100 Hz by the customer. If G_{vg} is considered fixed @100 Hz we need to tailor the open loop response T(100) to meet specification on G_{VG}/(1+T). For 10 % variation at the output due to V_G effects we need 1/(1+T) to be at least -20 db. For 1% variation at the output due to V_G effects we need 1/(1+T) to be - 40 db. Again to do this we need high T at the mains frequency, and all harmonics of the mains. An op-amp is ideal to achieve this high low frequency gain. That is the gain of an op-amp at low frequency is > 10^5.

3. Desired Closed Loop Response Time to a Large Disturbance

We term f_C as the unity gain cross-over frequency of T(s),**1/(1+T(s))** as well as T/ (1+T) as shown on the top of page 8. To verify this, just consider the two cases of T>>1 and T<<. Hence, if we modify the open-loop gain and change f_C we will also change the closed-loop f_C as well. This means we can use compensation to increase f_C to higher values to improve transient response. The **practical limit to higher f_C is 1/5 the switch frequen**cy.



In general the **transient response** of the closed–loop system will depend on the open loop T(s) cross-over frequency f_C according to the relationship.

$$\Delta t \text{ (response)} = \frac{1}{2p\, f_C}$$

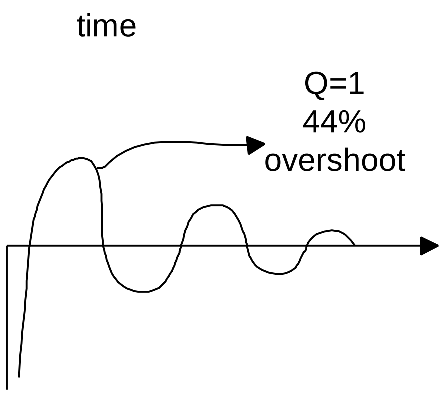
↓ Our spec for Δt ↓ Our design choice for f_c

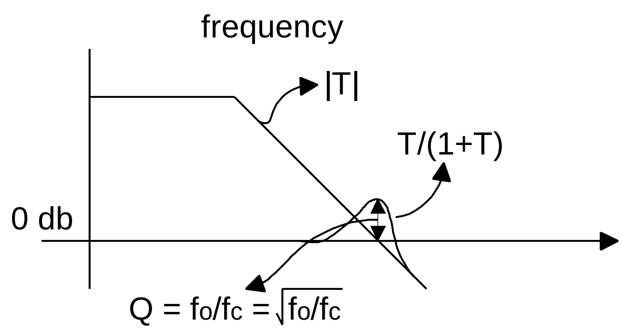
for Dt ¯ « f_c - is the trend

However, fast closed-loop response brings it's own problems like overshoot and ringing to the dynamic waveforms as described below in section 4. This is avoided by proper care of the phase margin at the unity gain cross-over of the open-loop T(s). Finally we repeat that f_C cannot exceed 1/5 of f_{SW} as an upper limit.

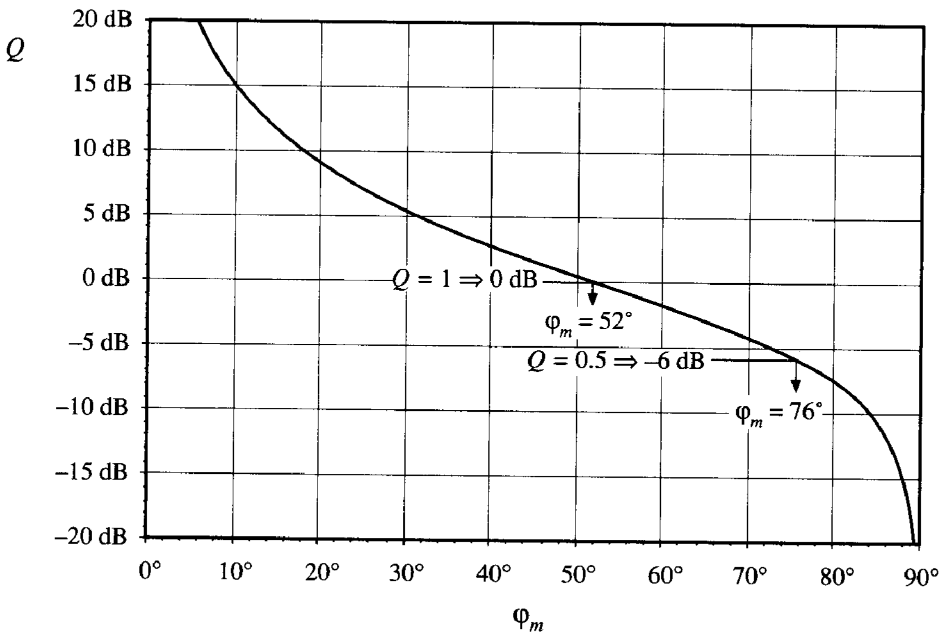
4. Allowable Overshoot Due to Solid State Limitations

In both the time and frequency domains we saw closed loop response overshoot occurs and was related to "Q" of the open loop, T(s). T/ (1+T) in particular was prone to "Q peaking".





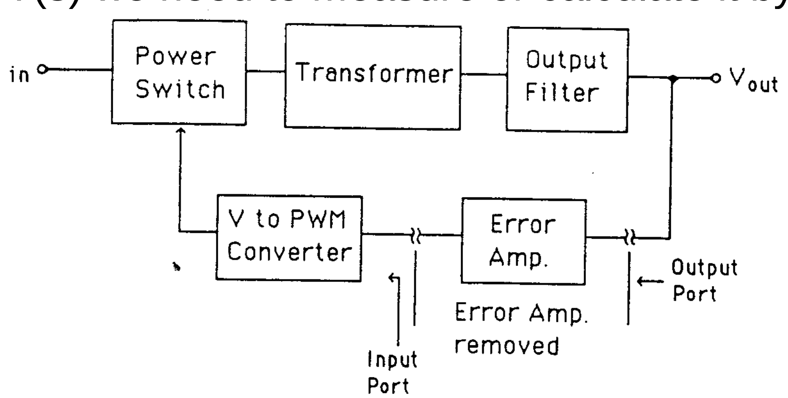
We can not always predict T/1+T behavior from T behavior alone. But for the special cases where T has a 0 db or unity gain cross-over via two isolated poles, we can relate the phase margin, ϕ_m , of T(s) to the closed loop "Q peaking" of ,T/1+T. This is summarized below.



Given a desired phase margin in the phase angle of T(s) = β G_c/V_m G_{vd}, what do we do to achieve it , especially if the original uncompensated T(s) is considered inadequate? Often the compensator box, G_C, is the only system box in the entire T(s) loop easy to diddle, with the goal of modifying T(s) to the desired shape versus frequency. In short to tailor a desired phase margin, ϕ_m, $\longleftrightarrow$ Use phase compensators in the G_c(s) box. Sometimes we apply compensation to make an unstable system stable. More often we apply G_C to make a better T(s) from an old T(s) that is stable but not optimum. We tailor the shape of the old T(s) by the G_C network alone. . **In our studies we will limit G_C(s) to four cases given below to balance load regulation versus transient response in closed loop.**

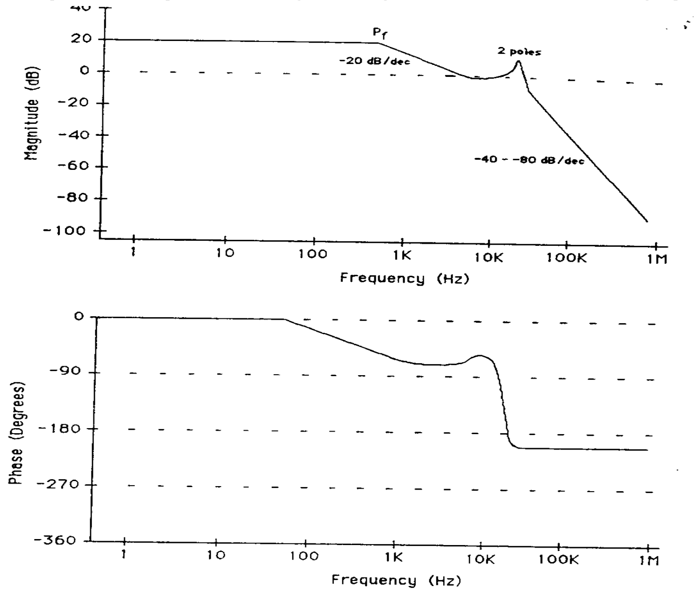
Compensation Type	Load Regulation	Transient Response
Single-pole	Good	Poor
Single-pole with in-band gain limiting	Fair	Good
Pole–zero	Good	Good
2-pole–2-zero	Good	Good

The use of an op-amp in the compensation network insures a pole at DC in the G_C frequency response which is very useful for achieving low values of G_{VG} (load regulation) at mains frequencies via the 1/ (1+T) factor. More on compensation networks and the use of Op-amps later. In summary, use of feedback in PWM converters has some clear goals, several of which are in competition with each other and tradeoffs need to be made in T(s) shapes. We will be able to tailor different portions of the original T(s) with G_C(s) to achieve most goals simultaneously. To know T(s) we need to measure or calculate it by breaking the loop.

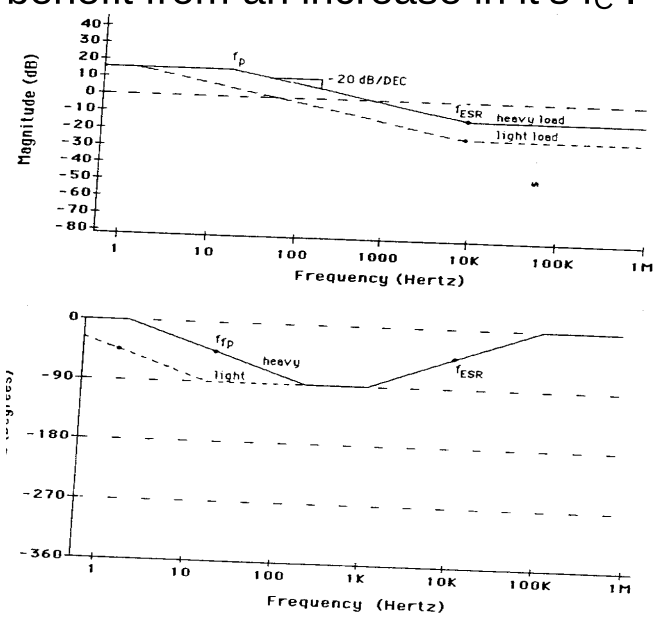


Once we have open loopT(s) we can carefully inspect it to see how to improve it by the addition of compensation. For example on page 11 we plot two T(s) plots and show in general why we would employ compensation to improve the old T(s) to create a new T(s) with improved properties. The first T(s) is one that has three poles and too a small phase margin at unity gain. It needs phase compensation to be stable under closed loop operation. The second has a single pole and will always be stable under closed loop conditions. Unfortunately its cross-over frequency is too low resulting in a sluggish transient response. It may not be able to correct fast transient disturbances. We can change that.

The T(s) below is not acceptable because it's phase margin is not adequate, possibly negative, insuring positive not negative

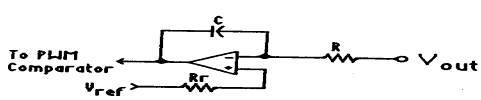


feedback. How would you fix it? The next T(s) while stable would benefit from an increase in it's f_C . How would you achieve this?

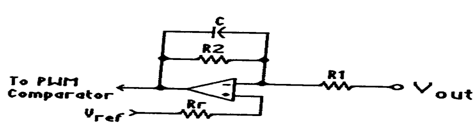


The single pole in the above T(s) arises from the load in parallel with the filter capacitor. Since $f_P \cong 1/\ R_{LOAD}$ we also see that the G_{VD} pole location depends on the loading. That is T(s) will shift with the load. Finally in the above plot we see the appearance of a zero in T(s) from the ESR of the output capacitor. These details

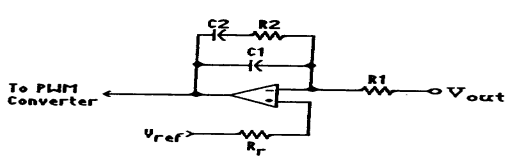
are crucial to proper compensation design, and do not always appear clearly to the new engineer. In summary we see that compensation is not limited to unstable T(s) and its use is more likely to arise to improve closed loop response. Looking ahead to section C there will be two broad classes of compensation networks, G_C. One, lead compensators or proportional differential (PD) compensators and two,lag or proportional integral (PI) compensators. Each will tailor a different portion of the original T(s) to create a new and better T(s). However, there will be undesired effects from one type of compensation on the T(s) shape in a different frequency region that we will have to carefully monitor and design around. In addition we need to realize that the converter transfer function poles and zero locations may also depend on loading conditions and the existence of parasitic elements. We will see examples of both in this lecture. Four separate G_C networks with op-amps are shown below.
a)-single pole G_C, b)one pole with gain limiting G_c)pole-zero



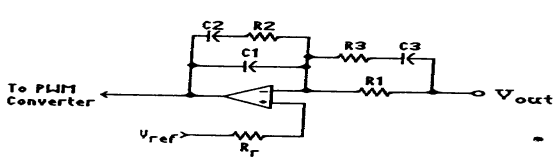
(a)



(b)

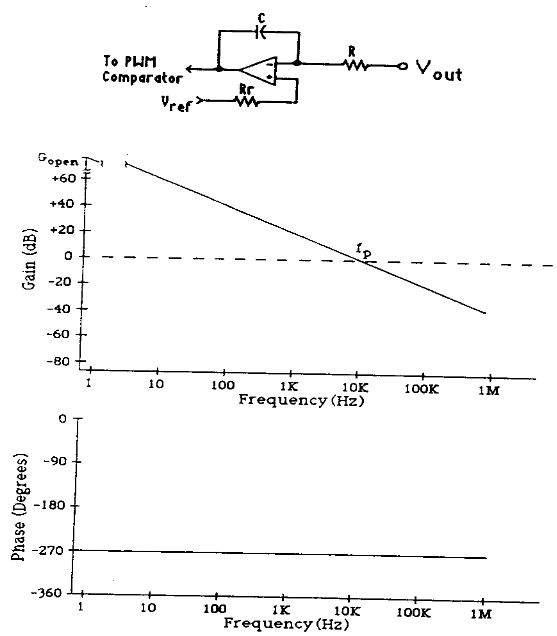


(c)

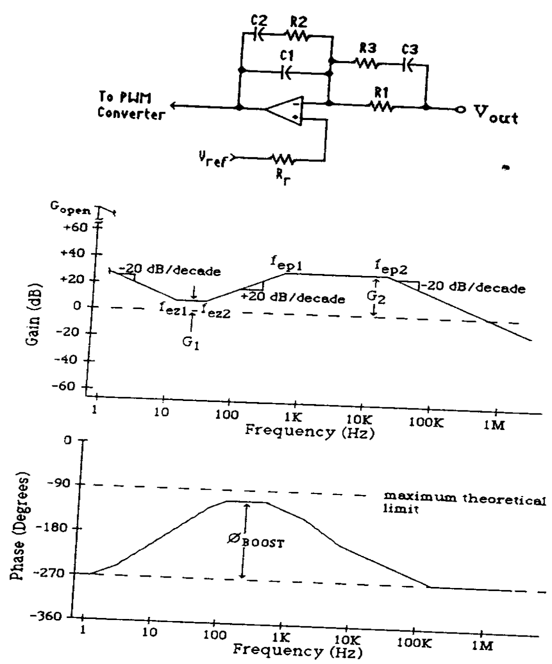


(d)

compensation,d)2-pole and 2 zero G_C compensation. The one pole G_C Bode plots are given below. Note the constant phase.



What about the double zero/ double pole G_C network with op-amp?



We will find use for these G_C networks in " improving T(s) response" to achieve better closed loop response in Lecture 51.

C. Compensation Networks

1. G_c and its use for Alterations/Tailoring of Open-Loop T(s) to Achieve Closed-Loop System Goals

In a loop gain $T = b \frac{G_C}{V_m} G_{vd}$ $G_c(s)$, the compensator, is in the low power portion of the loop where it is <u>easier to manipulate and diddle with</u>. We are diddling G_C for several reasons**. One**, to improve ϕ_m of T(s) so that either $\frac{T(s)}{1+T(s)}$ or so that $\frac{1}{1+T(s)}$ has the desired DYNAMIC or TRANSIENT characteristics. **Two**, so that 1/ (1+T) has the desired characteristics in some specified low-frequency range, usually around the AC mains low frequency region, so as to achieve low sensitivity to input voltage changes.

Illustrative Goal	$G_c(s)$ Solution
i) $\phi_m \uparrow$ @ f_x or to increase f_c of T(s)	1. Add a <u>zero</u> to $G_c(s)$ at $f_y < f_x$ so $\phi_m(f_x)$ is larger and so is $f_c \uparrow$

This is termed a PD compensator network.

ii). Increase low f loop gain to insure that the $\frac{\Delta V_o}{\Delta V_g}$ spec @ f_x met via 1/1+T	2. Add an <u>inverted</u> zero to the loop gainT(s) @ $f_y > f_x$ so that 1/1+T is smaller at f_x is

This is called PI a compensator network.

iii). We can try to do <u>both</u> 1 and 2 to the same T(s) via a combined PID G_C network. We must be careful because extra phase margin at one frequency does NOT GUARANTEE the proper phase margin at another frequency, where undesired instability may occur. Tradeoffs are required.

iv) We usually employ an operational amplifier with feedback as the lynchpin element of the compensation network. Clearly the op-amp frequency response must be high enough to exceed the location of any compensation pole or zero or the G_C block , when employing an op-amp, will not work properly.

Before we start the detailed discussion of compensation schemes we need to keep **four guidelines in mind** as we tailor open loop,T(s), for various converters to achieve closed-loop goals.

a. T(s) phase should be less than –300 degrees whenever the open-loop gain exceeds o db. ϕ_M = ???

b. The closed loop f_C should be high, if a fast transient response is desired. However f_C should never exceed 1/5 of the switch frequency, $f_C < f_{SW}/5$. Why is this??

c. T(s) should have as LARGE value as possible in order to make T/(1+T) be dependent only on passive elements in H(s) and no other factors.

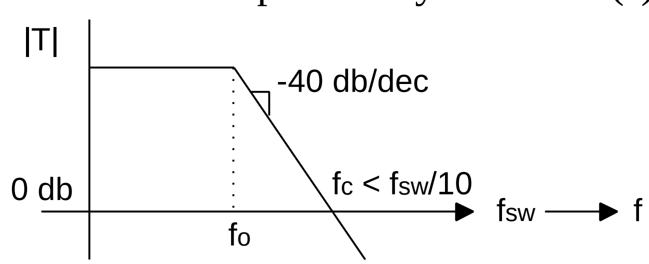
d. For reliable closed-loop stability it is best for T(s) to cross unity gain at –20 db /decade if possible.

In the following three sections we will cover lead (section C2 lecture 50) lag (lecture 51) and lead/lag (lecture 51)

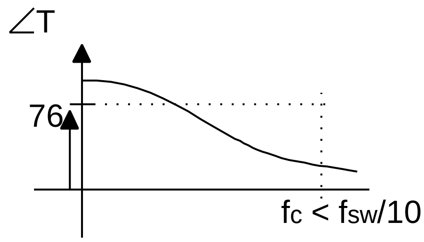
2. Lead Compensator in G_c(s)or PD Compensator

This G_C increases f_C of T/(1+T) thereby improving transient response but it also increases ϕ_M ,which can improve the closed loop stability, reduce overshoot and improve reliability. Consider a no-brainer T(s) below that under proper conditions crosses unity gain with TOO big a phase margin.

If we start with a potentially unstableT(s) as shown



original two pole system that oscillates closed loop where f_c is chosen << f_{sw}



Worst case two poles cause $\phi_m \rightarrow 0$ far from desired $\phi_m > 76^o$

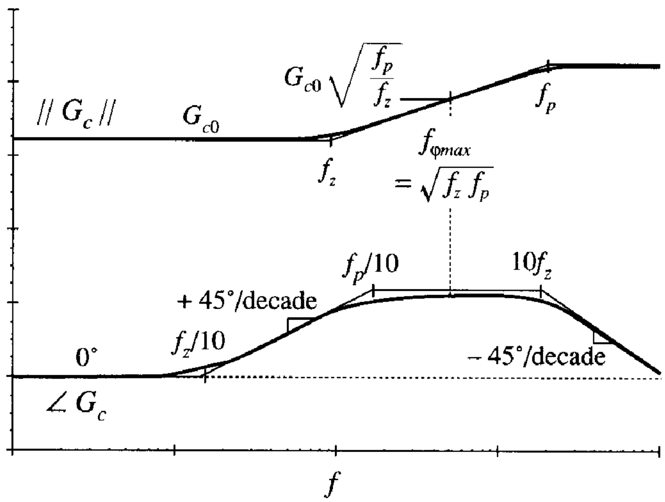
The above T(s) exhibits a double pole filter response characteristic of, for example, the voltage controlled DCM flyback converter. We can via $G_c(s)$ add a term to the open loop response, T(s) to improve things. Specifically a zero placed at or below the DOUBLE POLE of the original T(s), in order to improve ϕ_M. At somewhat higher frequency another pole is placed in order to compensate for the zero at all higher frequencies of T(s). We wish our compensation of T(s) to make its effects felt only where needed. Clearly in general, for phase lead compensation $f_Z << f_P$. Full phase contribution from the zero starts at 10 f_Z whereas the full pole phase doesn't occur till 10 f_P. Hence we insert phase over a limited frequency range. In short,

$G_S(s) = G_{co} \dfrac{(1+s/w_Z)}{1+s/w_p}$ →the zero is located below f_c of original T(s) to increase ϕ_m and f_P lies above original f_C of T(s).

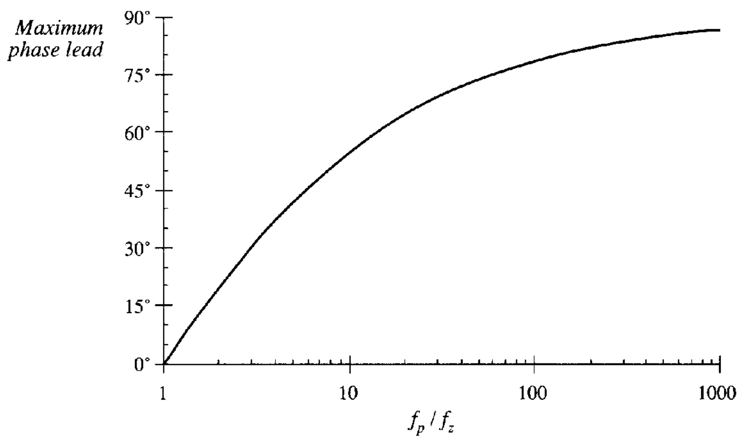
Again we always want $f_p << f_{sw}$ as well as below the maximum frequency response of the operational amplifier used in implementing G_C. We are seeking positive and increasing $\phi_m \uparrow$ @ $f = f_c$ so we design G_C carefully:

(1) Choose w_z and w_p locations such that maximum phase from $G_c(s)$ occurs @ f_c the original cross-over of uncompensated T(s). Intuitively f for ϕ_{max} $f = \sqrt{f_Z \ f_p}$ But value of ϕ_{max} is complex

Clearly the extremes are $f_z = f_p$ $f = 0$, $f_p >> f_z$ $\phi \rightarrow 90^o$



Graphically we plot the phase contribution fore various f_P / f_Z ratios using the relationship $\mathrm{Sin}(\phi) = (f_P - f_Z) / (f_P + f_Z)$. We find ϕ_{MAX} =55 degrees for $f_P / f_Z = 10$ and 75° for $f_P / f_Z = 60$ as shown below.

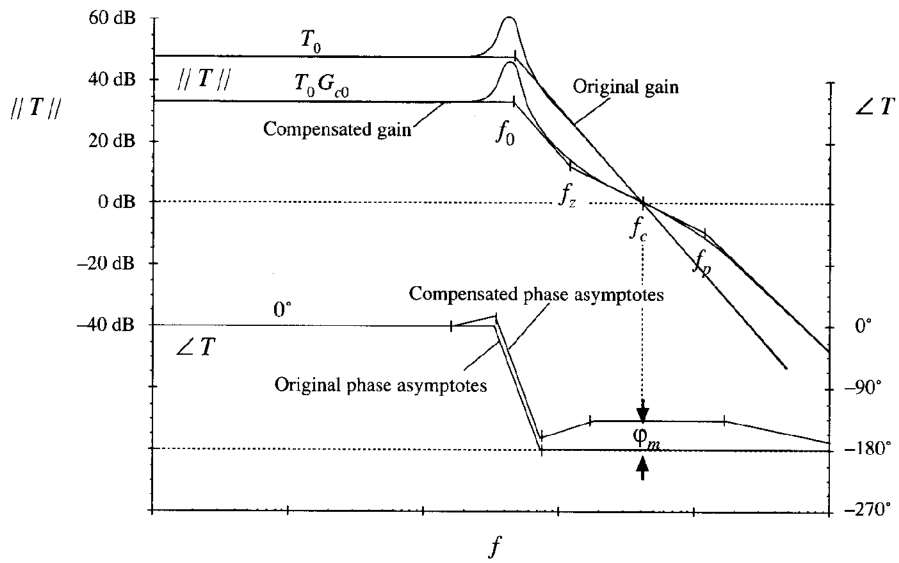


To better employ the ϕ_{max} chart to insure that we place maximum phase lead at $f_c = f_{\phi max}$ do the following in the G_C design.

1. Choose ratio f_p/f_z from the desired phase we want to introduce to T(s) to achieve the closed-loop goals.
2. From the desires Max ϕ we get both f_Z and f_P locations

$$f_Z = f_C \sqrt{\frac{1 - \sin f_{max}}{1 + \sin f_{max}}} \qquad f_P = \sqrt{\frac{1 + \sin f_{max}}{1 + \sin f_{max}}} \; f_C$$

This sets the two frequencies in the G_C network. The uncompensated and compensated T(s) are shown on page 18.

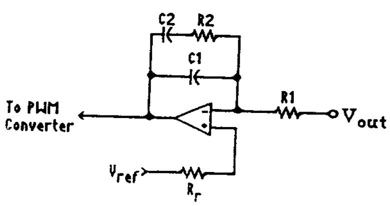


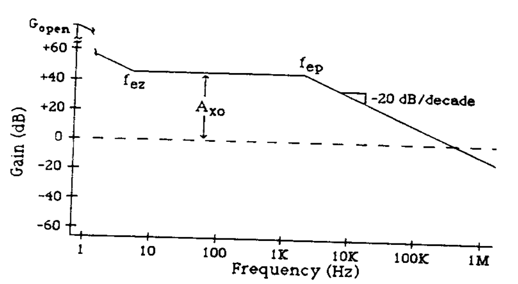
The case above G_{co} was purposely set to $\sqrt{\frac{f_z}{f_p}}$ so that the lead compensator inserted unity gain at f_c and thus the crossover frequency of the open loop was **unchanged as compared tto that of the open-loop gain even with the addition of the compensator**. We need not be so picky. Sometimes we even wish to increase or decrease f_C to achieve faster/ slower transient response. Other G_{co} choices are sometimes employed as shown below:

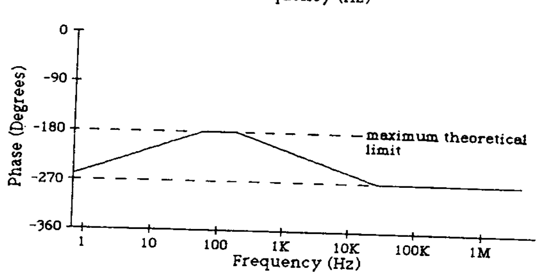
$G_{co} < 1$	$G_{co} > 1$
less open loop |T|, less -db	1/1+T more |T|, more -db for the 1/1+T factor
lower f_c	larger f_c
Slower transient response	Faster transient response

In summary lead compensation increases phase margin the original T(s) at f_C but it can also introduce increased gain to the new T(s) and also alter the f_C of T(s) if we so choose. We must carefully pick G_C component values such that G_C introduces no new gain at f_C to keep the f_C and transient response the same. The op-amp circuit to achieve this is shown on page 19. The

inherent DC gain of the op-amp usually has a pole at DC or low frequency that provides higher T(s) values near the mains frequencies and it's harmonics. A zero is introduced just below the double pole of the L-C filter in order to provide as much as 90 ° of phase compensation at f_C , in order to keep ϕ_M positive and close to the desired value of 76°. That is the phase lag of the op-amp **decreases**, due to compensation, between f_Z and f_P. The last pole rolls off the T(s) gain at high frequency, BUT it ALSO counteracts the inevitable extra zero arising from the capacitor ESR in the output circuit of any PWM converter. The pole-zero compensation achieved with an op-amp and one set of feedback R-C elements is shown below in the G_C(f) plots. For HW #4 can derive the pole and zero locations for G_C only in the op-amp circuit below. Show circuit element conditions for $f_Z < f_P$ to occur.
For HW #4 please derive f_Z and f_P expressions for the G_C plots shown:







Use your knowledge of op-amps from earlier courses.

A simple lead circuit design in a G_C network is next. We show how G_C design in determining a new T(s) from an old T(s) is an iterative process. It requires patience to see the changes we cause. We start with a T(s) that has too small a phase margin, causing a METASTABLE system that sometimes under strong transient disturbance will break into oscillation. We need to "tweak" the original ϕ_M to achieve a bigger value. The "old T(s)" around the cross-over frequency will be altered to achieve a better T(s). Not only will the phase margin be improved but the transient response will improve on the new T(s). What especially difficult about design is the cut-and-try nature of the process. For example here the addition of a phase lead will also increase the f_C of the new T(s) and we have to "guesstimate" it during design. Knowing f_C will increase also tells us we have to choose ϕ_M to bigger than what we think we need to accommodate the extra phase lag from the old T(s) at the new and higher f_C.

A simple R-C network to achieve phase lead is shown below. For HW # 4 show that the pole and zero locations are as shown.