Lecture 49

Danger of Instability/Oscillation When Employing Feedback In PWM Converters

A. Guessing Closed Loop Stability From Open Loop Frequency Response Data

1. T(s) versus
$$\frac{T(s)}{I + T(s)}$$

2. Phase Margin Test for T(s)
a. Unconditionally Stable
 $\phi_m = 90^\circ$ for 1 pole T(s)
b. Conditionally Stable Case
1. Two Near-by Poles
 $T(s) \ crosses \ 0 \ db}$
 $T(s) \ crosses \ 0 \ db$
 $T(s) \ crosses \ 0 \ db$

B.Problem 9.5 of Erickson C.Closing Tidbits on an Unstable T(s)

Lecture 49 Danger of Oscillation/ Instability When Employing Feedback In PWM Converters

A. Guessing Closed Loop Stability From Open Loop Frequency Response Data

1. T(s) versus $\frac{T(s)}{1+T(s)}$ If we make loop gain, T(s),

arbitrarily large we benefit via 1/1+T factors in the reductions in Z_{out} or G_{vg} for the closed loop response ,as compared to the open loop response. On the other hand employing feedback brings the possibilities of system <u>INSTABILITY</u> once we close the loop. That is, even if all poles of $T(s) = \frac{N(s)}{D(s)}$ are stable and in the left-hand

plane, that does nothing for guaranteeing that the poles of the two closed loop factors T/(1+T) and 1/(1+T) are also in the left-hand plane. They may not be as we show below.

$\frac{\mathrm{T(s)}}{\mathrm{1+T(s)}}$	$= \frac{N(s)}{N(s) + D(s)}$	\Rightarrow	Same poles but not
$\frac{1}{1+T(s)}$	$= \frac{D(s)}{N(s) + D(s)}$	\Rightarrow	the poles of T(s)

Let's illustrate the point! Take a stable cubic T(s) in open loop, that suddenly goes unstable in closed loop due to the application of feedback. This is the downside or darkside of feedback- it's dirty little secret revealed that we will cover today.



 $\frac{T(s)}{1+T(s)} = \frac{100}{s^3 + 3s^2 + 3s + 101}$

Use an HP 48 root solver to find right half plane poles are formed in T/ (1+T) as soon as we close the loop on T(s).



Instability with right-hand plane poles occurred with a feedback loop closed, even though the original T(s) has only left half plane poles. Is there any way to predict from the open loop T(s) whether or not the closed loop will be unstable so we prevent unpleasant suprises??

2. Phase Margin Test

We will examine below the relation between the open loop phase margin and the CLOSED LOOP "Q". For large closed loop "Q" can bring dynamic problems like overshoot toi devices and components. From the Bode plots of the open loop gain, T(s), we will be able to predict stability of $\frac{1}{1+T(s)}$ or $\frac{T(s)}{1+T(s)}$. Intuitively, we expect when |T(s)| = 1, the phase shift term or phase of T(s) cannot be 180° because

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this will turn good stabilizing negative feedback into bad destabilizing positive feedback. But how far from 180° can we get when the magnitude of T(s) is unity and still be stable. The amount of angle separating the phase of T(s) and 180 degrees is termed the "Phase Margin" ϕ_m . Positive phase margin is a stable leading indicator but negative phase Based on prior margin is an unstable leading indicator. experience we state ϕ_m of 76° in the open loop T(s) is a desired rule of thumb for always achieving stable closed loop situation with low enough "Q" to also avoid overshoot problems! Lets look at several T(s) amplitude and phase plots and see what we mean. In general we will find that increasing the positive phase margin of the open loop T(s) reduces the "Q" of the closed loop functions T/ (1+T) and 1/(1+T) and results in no transient overshoot and ringing in the closed loop responses. A small phase margin in the open loop T(s) means a high Q in the closed loop functions, such as T/ (1+T), with a transient response that both overshoots and rings. Lecture 50 will detail the transient response of the closed loop functions versus "Q".

We will first at first be dealing with VOLTAGE CONTROLLED converters operating in the CCM mode, later in Chapters 10 and 11 we will also include DCM dynamic response and add current control loops respectively. Clearly transformer isolation within converters will primarily change only the DC response, unless transformer parasitic's play a big role. The control to output open loop characteristic of voltage controlled converters, T(s), is the behavior of the converter with the error amplifier removed as shown below.



Common topologies for this feedback approach include buck, half and full bridge as well as half-forward and push-pull. T(s) versus frequency can either be calculated (never works) or measured (the safe way). We break the voltage feedback loop at the input to the error amplifier since it has such high input impedance. The point where the output voltage enters the error amplifier's negative input is considered as the output port for T(s) measurement or calculation. The full circuit diagram of a **forward converter** with it's T(s) under test is given in the diagram below. Note the ESR of the filter capacitor, which is a parasitic element that will introduce an important zero to the open loop T(s). Note also how the error amplifier in it's own feedback loops is removed for open loop T(s) measurements or calculations. Later in Lecture 50 it will be compensation networks that we will introduce into the open loop gain that will "fix" the problems in the original open loop gain leading to system oscillation or poor transient response. For now we will be content in "birddogging" the problems from the T(s) plots.



We can "guesstimate" the T(s) behavior for the forward converter as follows. The DC gain will be $V_{in} / \Delta V_{error}$ which will be equal to the buck circuit D(on duty cycle), which could be as large as unity. Hence in db the DC gain could be as large as 20 db to start. The L-C output filter will contribute a DOUBLE pole at $f_{P}= 1/2\pi (L_0 C_0)^{1/2}$. Hence we expect after f_P the amplitude plot of T(s) will roll-off at 40 db per decade. We assume that the zero from the ESR of the filter capacitor will occur at a frequency much higher than f_P due to the expected low value of the ESR resistance. Specifically, f_{ESR} =1/ $2\pi R_{FSR} C_0$. With this set of assumptions in mind we can plot both the amplitude and phase plots of T(s) as shown on the top of page 6. Typically, f_{ESR} (Tantalum capacitor) =20-30 kHz but the choice of an aluminum electrolytic capacitor could change f_{ESR} (Al electrolytic) = 3 kHz. Does the choice of a mere capacitor type change the open loop T(s)??



The above plots show how to measure the phase margin of T(s) for this case. Depending on details of component choices in the forward converter the T(s) indicates the possibility of oscillation occurring when we close the loop. We could get either stable or unstable behavior depending upon the sign and the magnitude of the phase margin.



On the left above the T(s) phase margin is +68 degrees and on the right above the phase margin is-50 degrees. Which is unstable and why? Several open loop T(s) cases present themselves as easy to determine closed loop stability, which we will deal with first. Later we will challenge more complex T(s).

a. Unconditionally Stable T(s) Case

An isolated pole or single pole always has $\phi_m = 90$ or more since the phase shift cannot exceed 90 degrees. This would be the choice for highly critical systems with feedback that we never want to go unstable. **The DCM flyback is an example of this T(s)**.

b. Conditionally stable T(s) Cases

A T(s) containing a pole located at low frequencies togeather with a second pole sufficiently far away from the first is a common situation. Depending on how far apart the poles are we get ϕ_m at unity gain from 180° to nearly zero. Many such T(s) are purposely designed so that the |T(s)| = 1 condition occurs at a T(s) slope of 20 db/decade. Only after the unity gain point occurs, does the second pole break.



$$\frac{T(s)}{1+T(s)} = \frac{1}{1+\frac{S}{W_o} + (\frac{S}{W_c})^2}$$

Compare to the standard two pole form $\Rightarrow \frac{1}{1 + \frac{S}{QW_c} + (\frac{S}{W_c})^2}$ $\Rightarrow W_c = \sqrt{W_o W_2}$, $Q = \frac{W_o}{W_c} = \sqrt{\frac{W_o}{W_2}}$

1. The low Q Closed Loop approximation

This case says the two poles are widely separated. Unity gain is crossed @20dB/decade and later the second pole breaks.

 $\omega_o = \omega_c Q$ lying well below ω_c in frequency

 $\omega_2 = \omega_c/Q$ lying well above ω_c in frequency



Higher f_c for $\frac{T}{1+T}$ implies we achieve a faster transient response with feedback employed than with open loop, due to reduced gain of T/ (1+T) compared to T.

2. High Q Closed Loop approximation

For Q > 1/2 f_2 decreases towards f_o and T(s) unity gain is now crossed @ 40db/decade which can lead to instability in the closed loop or oscillatory transient response.



"Big Q peaking" will occur in the T/(1+T) function as shown above, even though there is no "strong Q peaking" in the original T(s).

Value of $\frac{T(s)}{1+T(s)}$ @ f_c is Q above the asymptote. Q = $\frac{f_o}{f_c} = \sqrt{\frac{f_o}{f_2}}$. If f₂ \rightarrow f_o Q = 1 and the $\phi_m \rightarrow 52^o$ as shown on next page. Method is find f for |T| = 1 < T (f for unity) is evaluated and 180 - $< T \equiv \phi_m$. Clearly $\phi_m = f(f_o/f_2 \text{ or } Q^2) = \tan^{-1}(1+(1+4Q^4)^{1/2})/2Q^4)^{1/2}$ which we plot below on page 11.

The plot is only good for the two poles near f_c approximation.

A closed loop Q = 1/2 or -6 db has $\phi_m = 76^\circ$. A closed loop Q = 1 or 0 db has a $\phi_m = 52^\circ$ Likewise for $\phi_m \rightarrow 0$ Q for the closed loop then skyrockets



Above plot of Q versus the phase margin is good only for two close poles. It is not good for 3 poles near f_c . The Q versus ϕ_m above is also good for the case of T(s) crossing unity @ 40db/decade with an additional zero at f_2 just past the unity gain crossing as we saw occurred via the f_{ESR} for the forward converter.



See Pbm. 9.5 for more details on how to analyze this special case. There are other more interesting T(s) possibilities as shown below. What do we do with these cases?? Any suggestions?



FOR HW #4 explain what excess phase will do to the closed loop.

Voltage Controlled Flyback

Let's consider next the discontinuous mode flyback converter controlled by a voltage loop, which has a T(s) very different form the forward converter examined previously. In particular we will find that T(s) has **only a single pole**, rather than a double pole. The ESR of the filter capacitor still introduces a zero to T(s) at a frequency above that of the pole as shown of the Bode plots of a DCM flyback shown below .



The output filter pole in the voltage-controlled flyback operating in DCM DEPENDS on $R_L = V_{OUT} / I_{OUT}$, the load resistance. This means that as we change the load conditions (light versus heavy load) we are moving the pole location of the output filter around: $f_P = 1/2\pi R_1 C_0$

As load current decreases(heading to open load) the pole frequency decreases and vice versa. This makes error amplifier compensation schemes more challenging for the flyback.

B. PROBLEM 9.5 of Erickson

The forward converter system of Fig. 9.43 is constructed with the element values shown. The quiescent value of the input voltage is Vg = 380V. The transformer has turns ratio n1/n3 = 4.5. The duty cycle produced by the pulse-width modulator is restricted to the range $0 \le d(t) \le 0.5$. Within this range, d(t) follows the control voltage v_c(t) according to d(t) = $\frac{1}{2}$ v_c(t)/V_m with V_m = 3 volts.

- (a) Determine the quiescent values of: duty cycle D, the output voltage V, and the control voltage V_c.
- (b) Sketch a block diagram which models the small-signal ac variations in the system, and determine the transfer function of each block.
- (C) Construct a Bode plot of the loop gain magnitude and phase. What is the crossover frequency? What is the phase margin?
- (d) Construct a Bode plot of the closed-loop line-to-output transfer function magnitude

 $\frac{\hat{v}}{\hat{v}_g}$. Label important

features. What is the gain at 120 Hz? At what frequency do disturbances in vg have the greatest influence on the output voltage?



$$V_{o} = (\frac{n_{3}}{n_{1}}) DV_{g} \Rightarrow D = 0.332$$

$$\uparrow \qquad \uparrow \qquad \uparrow$$

$$28 \quad (4.5) \qquad 380$$



$$H(s) = 18.2/(18.2+81.8) = 0.182$$

V_o/V_{ref} ≈ 1/H
for T → ∞ V_o = 5.1/0.182 = 28V



PWM Flyback Model: Open loop with independent inputs: $\hat{V}_g,\,\hat{d}$ Forward Model:



For the flyback converter:

$$W_{o} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{500 \ 10}} = \sqrt{2} \times 10^{4} \frac{\text{rad}}{\text{sec}}$$
$$f_{o} = \frac{W_{o}}{2p} = 2.25 \text{ KHz}$$

$$QW_o = \frac{R}{L} \Rightarrow W_o = \frac{R}{L} \sqrt{LC} = R \sqrt{\frac{c}{L}} \approx 1.0$$

Zo element of control block

$$Z_{out} = R || \frac{1}{SC} || = \frac{SL}{1 + \frac{S}{QW_o} + (\frac{S}{W_o})^2}$$

↓ open loop

Op Amp section of control block



That is: $V_c(s) = G_c(s)[G_R(s) V_{ref}(s) - H(s) V(s)]$ Now isolate each contribution Op Amp relates <u>both</u> V_c/V_{ref} and V_c/V



input to op amp $V_{in}\approx 0$ so V_{ref} appears on Z chain from gnd.



 $G_R(s)$ for non-dc does have a from op amp.

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For HW # 4 Graduate students show:

 $G_{R} = \frac{R_{3} + \frac{1}{SC_{2}} + R_{1} ||R_{2}}{R_{3} + \frac{1}{SC_{2}}} = \frac{1 + SC_{2}[R_{3} + R_{1} ||R_{2}]}{1 + SR_{3}C_{2}}$ $G_r(0) \equiv 1$ for dc & V_{ref} only d.c. Other cases $V_{ref} = f(w)$ $T(s) = G_c \frac{1}{2 V_{res}} G_{vd} H$ Loop Gain: Break the loop @Ve and inject T(s) = $\frac{T_o(1 + \frac{W_c}{s})}{1 + S/W_oQ + (S/W_o)^2}$, $T_o = \frac{G_{c\infty}}{2V_M} G_{do}H = 0.96$ $T(s) = \frac{T_o(1 + \frac{W_c}{s})}{1 + \frac{S}{OW} + (\frac{S}{W})^2}$ Q < 1/2 and is 1.0 as calculated. Use Q1 for phase asymptotes. $10^{-1/2} f_0$ $\begin{array}{cccc} & & & & & & & & & \\ | \leftarrow ----- f_0 ----- f_0 ----- \rightarrow | \\ 712 \text{ Hz} & 2.25 \text{ kHz} & 7.12 \text{ kHz} \\ & \downarrow & \downarrow \\ & 90^\circ & 90^\circ \end{array}$ *10 f_o range for full 180° phase swing $f_{c}/10$ 220 Hz 45°/decade 45°/decade $\|$ *100 f_c for full 90° range



Of special interest is $\angle T(f = f_c)$ to evaluate ϕ_m



the combined plots.



C. Closing Tidbits

We hit on a few trends in T(s) plots at very high frequencies to close out lecture 49. We choose a "sick" open loop T(s) and prepare for Lecture 50 which will tailor the "sick" T(s) to achieve a healthy T(s) that will not oscillate when we close the loop around it

with feedback. Below we look at a measured open loop gain plot for T(s) of a voltage and current controlled forward converter and speculate on it's stability in closed loop. We also speculate how to add compensation to the open loop response to achieve closed loop stability. The voltage feedback provides for the single pole at around 1 kHz that presents no problems to closed loop stability.



The current feedback provides for a DOUBLE POLE at ½ the switch frequency, as we will see in Chapter 11. This puts a big dent in the T(s) plots as shown above. Especially note the possibility of NEGATIVE phase margin, which would guarantee system instability in closed loop. Atthough the frequencies employed in feedback loops and the converter models themselves are not valid at these high frequencies, if we make the closed loop gain too high this may cause instability problems at ½ the switch frequency in the closed loop response. For HW # 4 Of the four compensation schemes listed on page 21, which is best suited to achieve closed loop stability for the given T(s) above

and WHY.

Compensation Type	Load Regulation	Transient Response
Single-pole	Good	Poor
Single-pole with in-band gain limiting	Fair	Good
Pole-zero	Good	Good
2-pole-2-zero	Good	Good

Draw sketches of the expected optimum compensation scheme you choose.