LECTURE 40
Introduction to Converter Dynamics

A. AC Model Construction
   1. Actual Switch mode Non-Linear System
   2. Small AC Models by two Analytical Paths
      a. Circuit averaging over T_s
      b. State space Averaging over T_s
   3. Common Goal that Old time feeling of Linear System Analysis
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   4. Recap of $<>_{Ts}$ concept good only for $f \leq f_s$
   5. Why bother with state space
      a. Well established algorithm
      b. Very methodical
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B. Uses for Feedback in Converters
   1. Regulate output Voltage V_o versus Switch Duty Cycle d
   2. Regulate V_o versus I (control)
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   5. Design Proper Feedback Loops
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   to estimate Transient Response, $Z_{in,}$ and Z_{out}
      a. Valid only for f << fsw
      b. Model depends on the chosen DC Operating Point Linearization

LECTURE 40
Introduction to Converter Dynamics

A. AC Model Construction

1. Overview

We have finished the first 6 chapters of Erickson that outlined DC operation as well as power magnetics in chapters 12-14. We are about to start converter dynamics, which covers chapters 7-11 of Erickson. Let's motivate the next ten lectures or so by showing where we are heading. Consider the converter with feedback below.

Objective: maintain $v(t)$ equal to an accurate, constant value V.

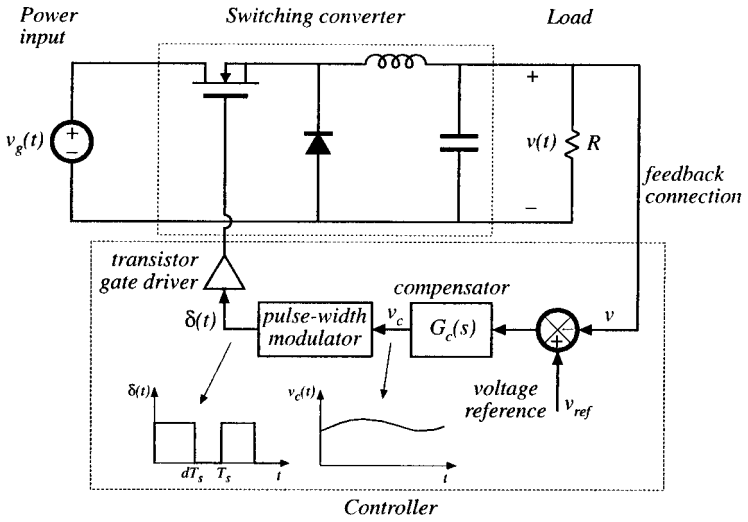
There are disturbances:

- in $v_g(t)$
- in R

There are uncertainties:

- in element values
- in V_g
- in R

A simple dc-dc regulator system, employing a buck converter



We want to predict the transient response of the converter to disturbances, so we can design in the desired settling times and dynamic response to disturbances as well as predict any potential instabilities we might encounter when we employ feedback. These are familiar possibilities for normal linear systems, but are problematic for the switch mode systems because of the non-linearity's inherent in switching. Thus for example, the switch frequency, f_{SW}, introduces ripple. It also interacts with the low frequency modulation frequencies, f_M, in the duty cycle signal to produce side band frequencies. In

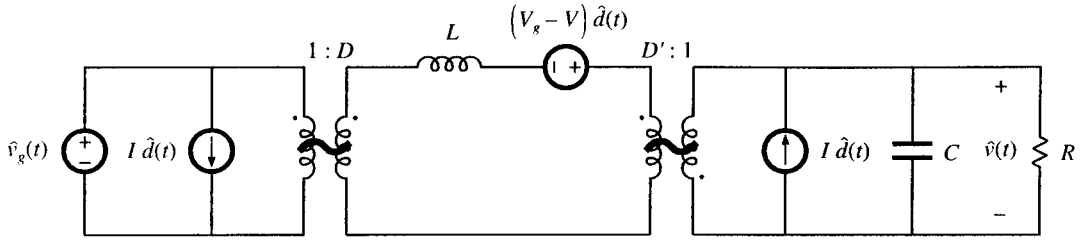
order to reduce these non-linearity's, to achieve a linear system, we need to remove the switching harmonics from our model. This will leave us with a valid low frequency model that is linear but no model at all for frequencies near and above the switch frequency. It's a price we pay in order to get a guiding linear model, which will allow:

- Predict how low-frequency variations in duty cycle induce low-frequency variations in the converter voltages and currents
- Ignore the switching ripple
- Ignore complicated switching harmonics and sidebands

Approach:

- Remove switching harmonics by averaging all waveforms over one switching period

Looking ahead to the success of this approach we will achieve a small signal model, valid only at duty cycle modulation frequencies well below f_{SW} such as that below.



buck-boost example

The above model can be employed in analyzing a variety of dynamic issues for converters, such as feedback loops and dynamic control of switch-mode circuits. To date we have examined in detail DC-DC converters as the primary application of switch mode circuits and as a second application we reviewed modern AC to DC rectifiers which allow for the input current to LINEARLY follow the input voltage in order to reduce conductive EMI. There is also DC to AC inverters, which we covered only briefly. In all of the above applications we will need valid AC models that are

linear, even if the price is a limited frequency range of validity.

Dc-dc converters

Regulate dc output voltage.

Control the duty cycle $d(t)$ such that $v(t)$ accurately follows a reference signal v_{ref}.

Dc-ac inverters

Regulate an ac output voltage.

Control the duty cycle $d(t)$ such that $v(t)$ accurately follows a reference signal $v_{ref}(t)$.

Ac-dc rectifiers

Regulate the dc output voltage.

Regulate the ac input current waveform.

Control the duty cycle $d(t)$ such that $i_g(t)$ accurately follows a reference signal $i_{ref}(t)$, and $v(t)$ accurately follows a reference signal v_{ref}.

This work on AC models, limited to $f<f_{SW}$ will guide us through chapters 7-11 as well as in resonant converters and modern rectifiers with active control on the input current.

Develop tools for modeling, analysis, and design of converter control systems

Need dynamic models of converters:

How do ac variations in $v_g(t)$, R, or $d(t)$ affect the output voltage $v(t)$?

What are the small-signal transfer functions of the converter?

- Extend the steady-state converter models of Chapters 2 and 3, to include CCM converter dynamics (Chapter 7)
- Construct converter small-signal transfer functions (Chapter 8)
- Design converter control systems (Chapter 9)
- Model converters operating in DCM (Chapter 10)
- Current-programmed control of converters (Chapter 11)

What's the key to removing the switch ripple and associated non-linearity's? How would you suggest one accomplish this?

2. AC Model Construction

There are three major theoretical paths that lead to the same small signal models as described next. One is circuit based and very intuitive called circuit averaging, which we will cover in lecture 41. A second is a more general circuit analysis approach called switch averaging which we will cover in lecture 42. The third is state-space averaging which we will cover in lecture 43. We briefly review all three below

a. Circuit Averaging

We will model the PWM converter by linearizing about a DC operating point and using circuit waveforms to average over one switch cycle.

Average over one switching period to remove switching ripple:

$$L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = \langle v_L(t)\rangle_{T_s}$$

$$C\frac{d\langle v_C(t)\rangle_{T_s}}{dt} = \langle i_C(t)\rangle_{T_s}$$

where

$$\langle x_L(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} x(\tau)\,d\tau$$

Note that, in steady-state,

$$\langle v_L(t)\rangle_{T_s} = 0$$

$$\langle i_C(t)\rangle_{T_s} = 0$$

by inductor volt-second balance and capacitor charge balance.

The resulting equations while linear are valid only for $f<f_{SW}$, that is low frequency modulation signals.

b. State space averaging

There is a second analytical path to achieve the same small signal models called state space analysis. It will comfort our doubts about the validity of AC models to get the same results several ways.

Why bother with state space averaging? It's an old established methodology using matrix mathematics

1. Classical Mechanics employed it for 200 years and Quantum Mechanics used it for 60 years
2. Matrix math methods are amenable to computer solutions

3. A very methodical way to model complex systems involving many variables

4. Learning curve is easy and it's easier to account for all the effects as we add them
5. Offers a second path up AC transfer function, T(s), mountain. It's just a kind of matrix accounting methodology. For details see lecture 44.

Either the prior circuit switch averaging or the new (for us) state variable approach. Both employ:

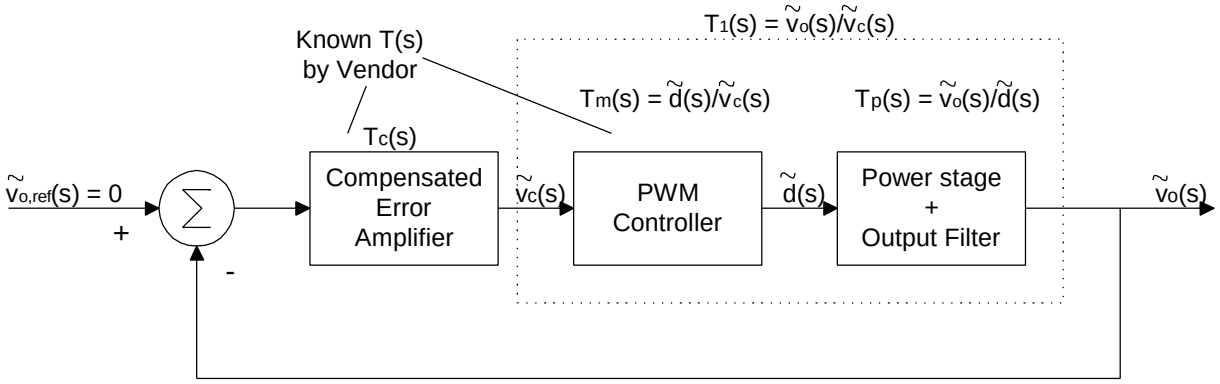
Averaging over T_s the switch cycle

Questionable Small - signal linearization of big switch signals.

Both approaches yield Quiescent DC and Small signal Ac models that are valid only for $f << f_{sw}$. This limitation of the linear models is a consequence of both approaches which provide the SAME small signal linear model for open loop gain of the switch mode portion of the system.

Goal : $T(s) = \hat{V}_o(s) / \hat{V}_c(s)$

Each block will have it's own unique $T_x(s)$



Again our second analytical path has the same goal - linear system transfer functions for a very non-linear switch mode circuit. Our goal is the AC transfer function $\frac{\hat{V}_o(s)}{\hat{d}(s)}$

Where V_o and D_o are quiescent conditions and $\hat{v}_o$ and $\hat{d}_o$ are

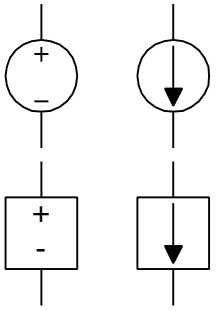
small perturbations around V_o, D_o respectively.

C. Switch averaging

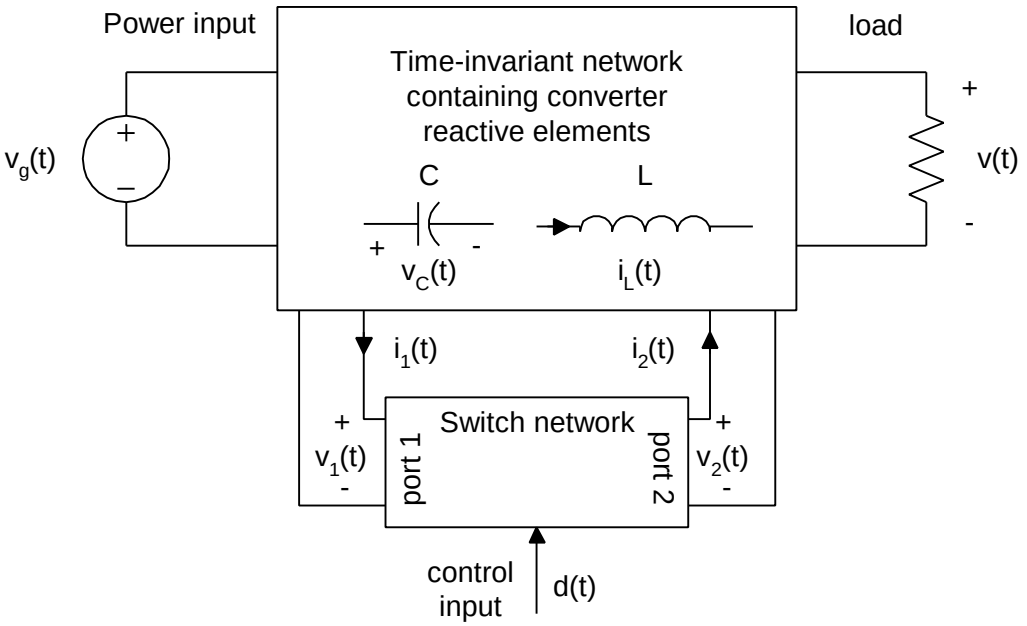
1. Overview

More general approach which gives both DC and ac equivalent circuits for PWM dc-dc converters. Remarkably, it replaces the switch network whose circuit topology varies with time into a box by itself, which is a time invariant. That is a two port box with four variables.. In the two port circuit averaged switch-box we will have:

Two averaged variables that are <u>independent</u>



Two averaged variables that are <u>dependent</u>



The prior time changing circuit topology is removed and is replaced by a two port time invariant switch network circuit model. However, In this approach the duty cycle d(t) will be composed of two parts:

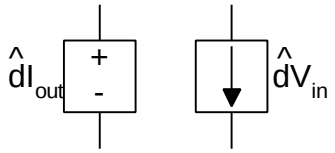
$$d(t) = D(dc) + \hat{d}(ac)$$

$\uparrow$ $\uparrow$

for dc trans-formers only — for ac sources only

D will appear primarily in the transformers while $\hat{d}$ will appear in the dependent sources as shown below.

Dependent input and output sources:



Looking ahead, this approach will successfully model both DC and AC transfer functions:

- Continuous Conduction Mode (CCM) where the dc transfer function is V_o/V_g = M(D, other loss) ← Erickson Chapters 2-4

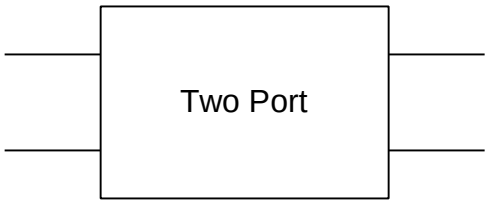
- Discontinuous Conduction Mode (DCM) where V_o/V_g = M(D, k, other loss) ← Erickson Chapter 5
  $k \equiv 2L/(RT_s)$ is a parameter describing when both diode and transistor switches are off in the DCM mode

- Current Programmed Mode (CPM) where a control current sets D ← Erickson Chapters 10-11

- Resonant Converters, Phase Control Rectifiers, Modern Low EMI rectifiers ← Erickson Chapters 15-18

2. History of Circuit and Switch Averaging

Researchers at Cal-Tech in 1970 first used it to model the right half plane zero we will meet soon in the small signal transfer function of the buck, boost, and buck-boost converters. Basic ideas for model creation is that four variables exist in a conventional two port network.



Choose two independent variables to correspond to KNOWN switched waveforms. This choice is intuitive and not always easy to justify. We average the independent variables over the switching or commutation period $\langle\rangle_{Ts}$

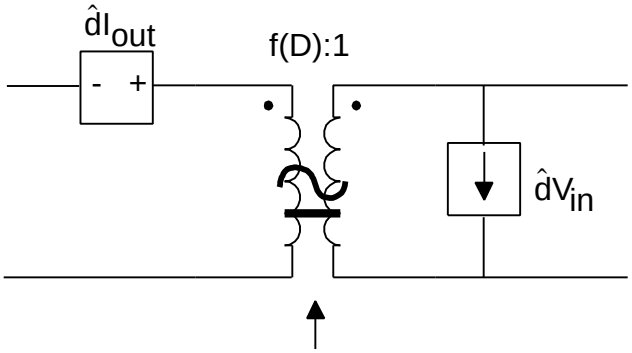
Express two dependent variables in terms of $\langle\rangle_{Ts}$ averaged independent waveforms. This gives a large signal model of the PWM converters, which we will later perturb and linearize for a small signal model. This will result in both DC and AC transfer functions for the converters.

Summary:

Take the large signal switch averaged $\langle\rangle_{Ts}$ model, perturb and linearize terms via standard small signal methods. Here d breaks into a DC and an ac term:

$$d(t) = D + \hat{d} \text{ and } d'(t) = D' - \hat{d} \text{ } \underline{\text{not}} \text{ } D' - \hat{d}' \text{ (why?)}$$

Neglect all higher order terms. This results in a linear time independent model. A prototypical form might be:



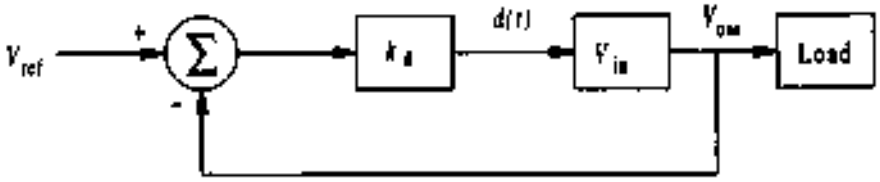
3. World of Bode Plots and Nyquist Criterion

Once we have all T(s) we can employ old familiar EE methods to characterize PWM converters that old time researchers Cuk and Middlebrook of CIT pinned for:

- Bode Plots to get open loop Gain and Phase Margin
- Employ Nyquist theory to analyze expected system dynamical response and stability issues.

B. Review of Feedback Types and Uses

PWM dc-dc converters support automated control of the output. The switch duty cycles, D, adjust to maintain precise operation on a continuous basis despite external perturbations. The figure below shows the block diagram for control of a converter. Switch–mode operation is hidden.

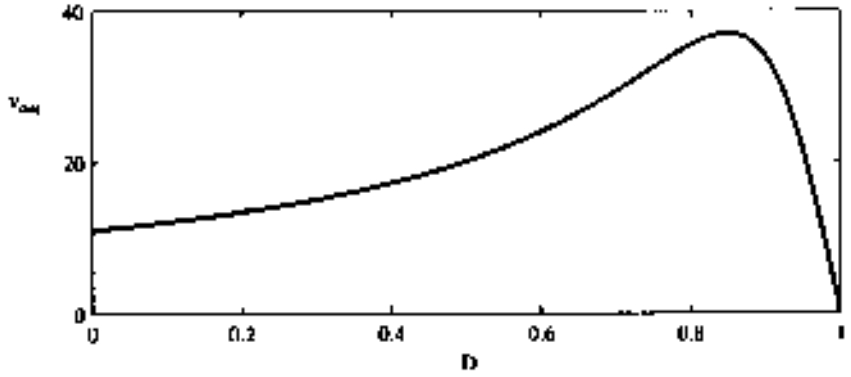


Output V_o is sensed and compared to V_{ref} and the error signal is amplified to produce a duty cycle command to the switches. D(t) is the control parameter and V_{in} represents an additional gain element. The open loop situation is $V_{out} = k_d[V_{ref} - Vout]V_{in}$.

While the closed loop unity feedback makes

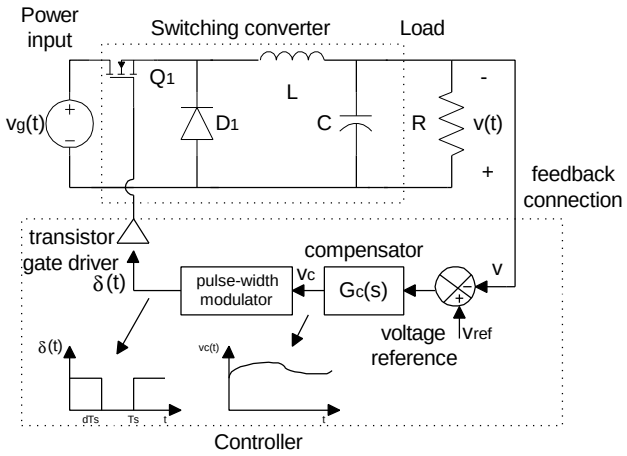
$$V_{out} = \frac{k_d V_{in}}{1 + k_d V_{in}} V_{ref}$$

If $k_d V_{in}$ is 100 then $V_{out} = V_{ref}$ to $\pm$1% and we also have active control to maintain this value. The control of V_o by duty cycle is workable only for single valued V_o versus D characteristics, even non-linear ones. **However V_o versus D sometimes is multi-valued when one includes static loss models for switches as we saw first semester**. The figure below is V_o versus D for a non-ideal boost converter.

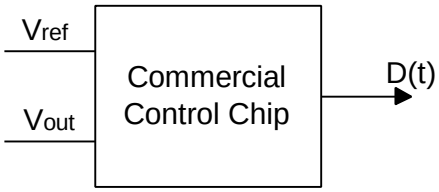


For D $\leq$ 0.85 the curve is single valued but for large duty ratios there are two D values for each V_{out}. A voltage mode control will experience a large D instability unless we implement a duty ratio limiter to keep D $\leq$ 0.85. This also occurs for other converters so a duty ratio limit control is good practice in any PWM converter that employs feedback. There are both voltage and current feedback loops. Each will be discussed below.

1. Regulate V_o via generated V_{ref} and measured V_o sensor via a commercial IC



A commercial control chip can be purchased to close the feedback loop.

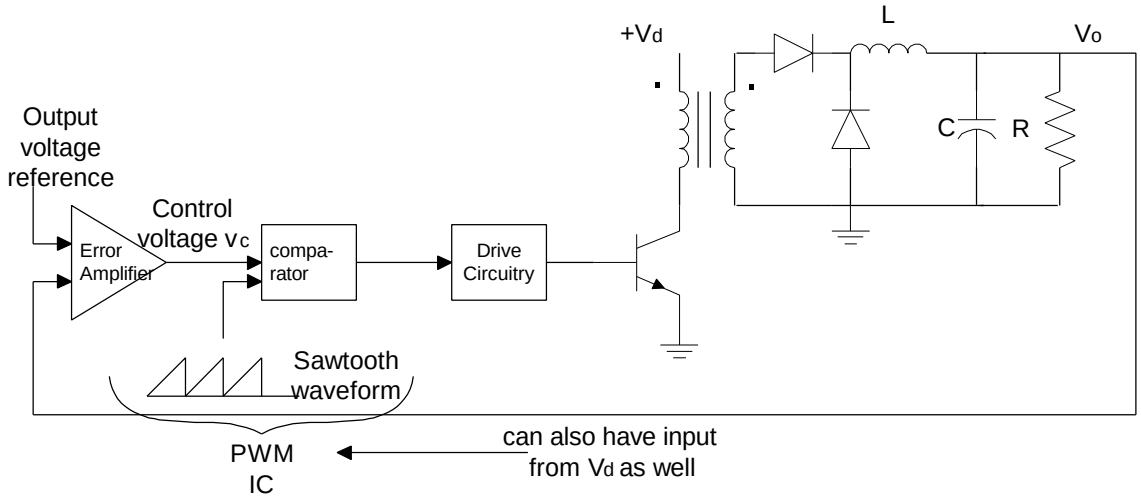


Transfer Function $V_o(s)/d(s)$.

Frequency domain plots will better allow us to estimate the range of frequencies that can be corrected effectively by the control. **Voltage mode control is useless for changes in V_{in} , however, because the change in V_{in} is delayed on its way to the output where it is finally detected**. We can improve the control by adding a current sensor, which monitors the source changes which otherwise are not subject to duty cycle control as shown below. This current sensor can also act to protect the switch from over currents. However, the control loop is now different as shown below . . Current feed control of output storage also has a BIG effect on the dynamical behavior of the negative feedback loop as we will see in section B2 and in more detail in later lectures on current control.

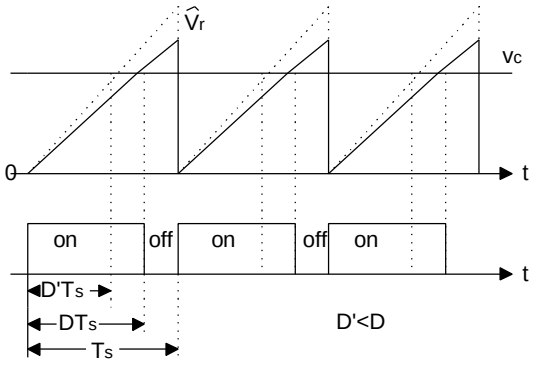
<u>Voltage mode feedback</u> is easy to visualize if you realize how easy a pulse width modulation occurs by comparing a sawtooth waveform with a control voltage as given in section C of this lecture. For now consider $d = V_c(t)/V_m$ where V_m is fixed and $V_c(t)$ varies. Noise on V_o @ f_{sw} may be fed back to PWM circuit. To avoid this we usually use a low pass filter in the V_o sense loop. We therefore ignore these effects below. Slowly varying $\Delta Vo\uparrow$ causes $d\downarrow$ which stabilizes Vo to

desired values. A typical voltage feedback loop is shown on the top of page 14 for your perusal.



Due to the slow response to changes in V_g(input), modern PWM control IC's also have a V_g feed-forward capability where ΔV_g changes both the slope and peak of sawtooth waveform in the pulse width comparator for faster response. If the amplitude of the carrier ramp is proportional to V_g rather than fixed at V_m then the switching function will depend on V_g variations also. This V_g feed forward method can be used by itself or in conjunction with V mode feedback

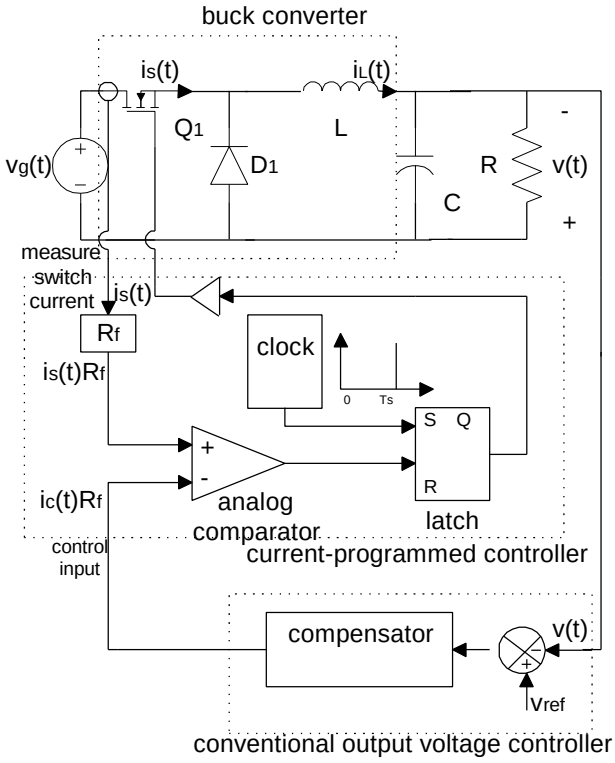
$\Delta V_d \uparrow$ yields $d\downarrow$ and provides inherent regulation for ΔV_d. For details see Erickson Ch. 11.



2. Regulate V_o via near source I control via I (transistor) sensor to vary switch duty cycle D

Current feedback is usually implemented in addition to

voltage feedback control. That is we have two feedback loops as shown below. . We have an ADDITIONAL control loop where V_c controls i_L directly which then feeds output storage V_o. In this way we get a faster response in the <u>inner</u> loop as we sense i_L immediately as compared to the L-C-R delayed V_d sensor.



switch

$I_{Tr} < I_c$ Tr

on

switch

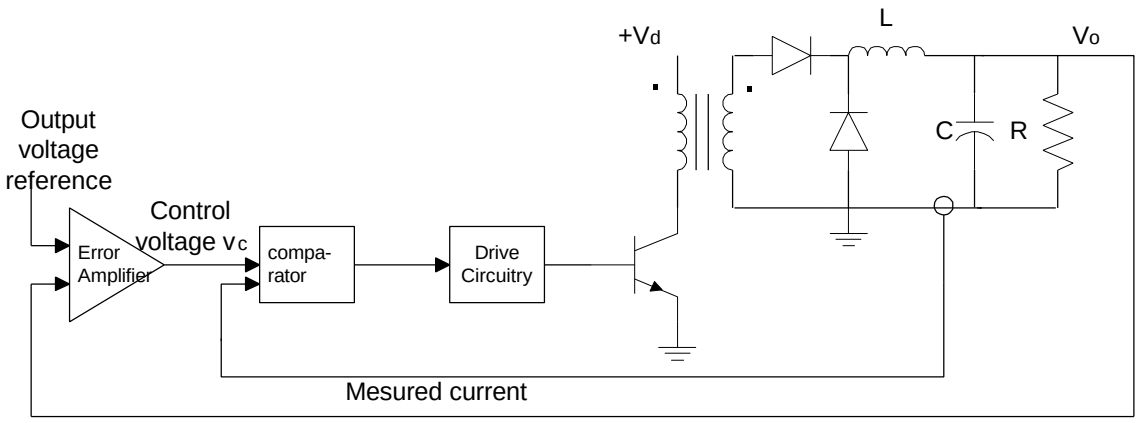
$I_{Tr} > I_c$ Tr

off

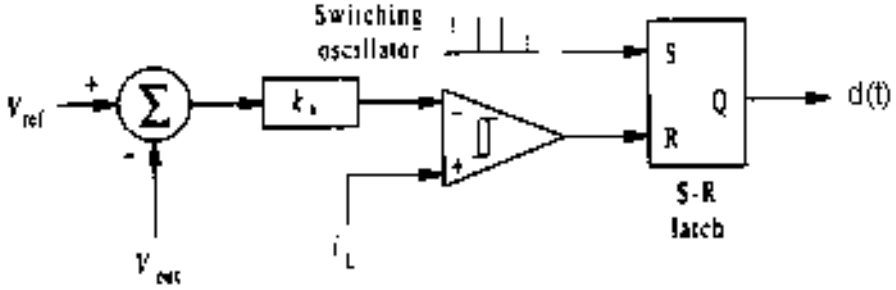
Ic set to peak spec of solid state devices "Save the Transistors" also occurs as a side benefit to current control.

Compare the feedback loop auxiliary circuitry for current mode control to that for voltage control feedback.

FOR HW# 3 explain the role of the RS-flip flop in the current control loop above as fully as possible. An alternative current control loop is given below on page 15.

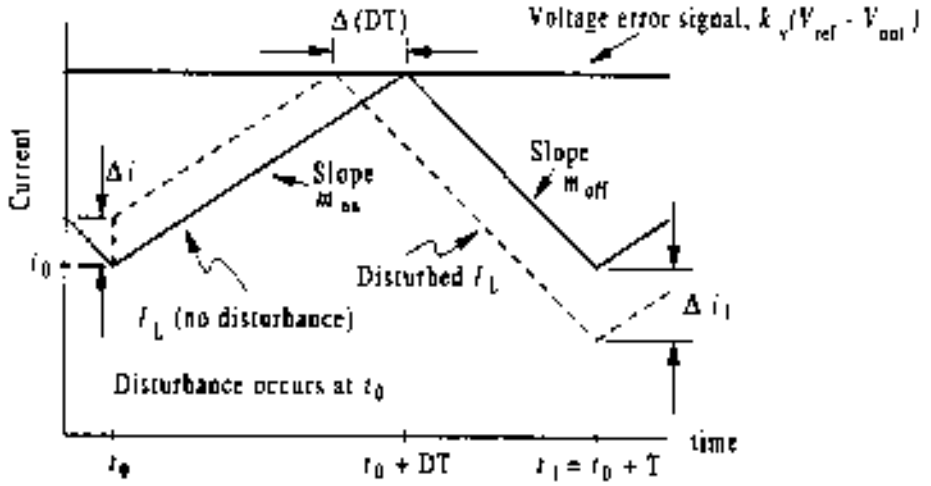


In this scheme either i_L or i_{sw} is measured and compared to the control voltage, V_c. Again V_c is generated in the external control loop. The key enabling control block for current control is in the figure below.



This approach is based on the established fact that i_L is a sawtooth or triangular waveform just like the PWM waveform put into the comparator to be compared with V_c to generate d(t). See section C of this lecture for details. We can then substitute i_L for the sawtooth carrier at f_{sw} ,**if and only if**, a triggering clock is provided separately. The clock pulse sets the digital latch at Z = 0 turning on the switch. As time progresses i_L ramps up to the point its signal is equal to $k_v(V_{ref} - V_o)$ and the latch is reset turning off the switch. Switch turn off sets i_L(max). If $V_{ref}\uparrow$ then $d\uparrow$ and raise i_L and vice-versa. If D exceeds 0.50 in current control an instability occurs for the Buck converter only as follows. The figure below compares i_L to a fixed error signal $k_v(V_{ref} - V_{out})$ at D = 0.5. **For HW #3 please fully describe this current mode**

control instability for the buck circuit and any way you suggest to avoid it. Would the addition of an additional dither signal do any good??



Some hints follow. Consider a disturbance Δi added to Z_o. Will Δi grow with time or decay out? In the Buck converter the positive di/dt slope is $m_{on} = (V_g - V)/L$ and the negative di/dt slope is $m_{off} = -V_o/L$. So at the switch turn-off time the on-time changes by $\Delta(DT)$ such that $m_{on} = \Delta i/\Delta(DT)$. The ramp down of i_L begins and at the end at t_o+T_s when the clock sets the switch back on the i_L difference is i_o(no disturbance) - Δi_1.

Now: $\Delta i_1 = m_{off}\Delta(DT)$

$$\Delta i_1/\Delta i = -m_{off}/m_{on} = -D/(1-D)$$

The negative sign arises because m_{off} is also negative. For stability D may not exceed 0.5. If D > 0.5 the initial Δi disturbance will grow and instability results. We will revisit this in Erickson Chapter 11 and replace steady V_c by V_c minus another ramp of slope m_r. This sets a new instability condition

$$\frac{m_{off} - m_r}{m_{on} + m_r} < 1$$

Which is always met for $m_r = m_{off}$. See Erickson Ch. 11.

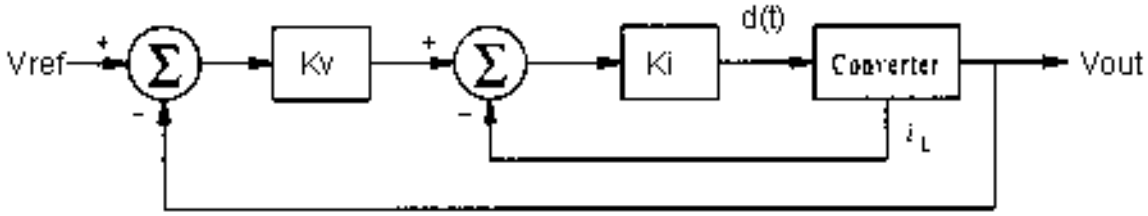
For HW#3 compare transfer Functions V_o/I_c versus $\frac{V_o}{\hat{d}}$.

Comparing the dynamical response in advance of results we will find LATER we state:

$\frac{V_O(s)}{\hat{d}(s)}$ has Two poles need to be careful about oscillation in negative feedback loops

$\frac{V_O(s)}{I_C(s)}$ has only One pole and is stable in any feedback scheme

Finally we can combine voltage and current feedback to obtain the two loop control shown in the figure below.



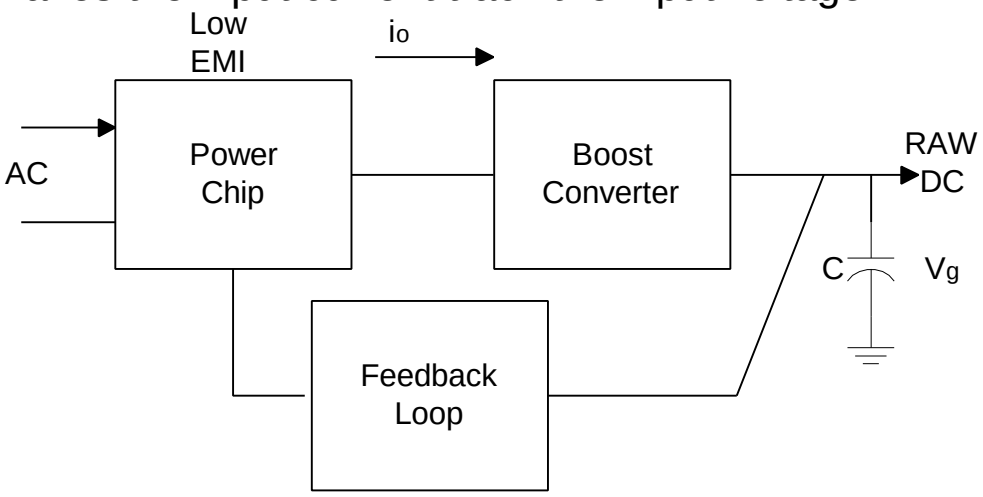
The error signal is $e(t) = k_v(V_r - V_o) + k_i(I_{ref} - I)$. The voltage error can be used as a virtual current reference. The two loop control has better dynamics than voltage mode feedback alone. The internal current loop can alter the duty cycle before V_o ever changes.

Next we consider another use of feedback with switch mode circuits, the modern rectifer with reduced conductive EMI.

3. Input Circuit to a modern power supply with low EMI to the mains ac

We want the input current to follow the input voltage over the full range of conduction angles, rather that have a sharp peak in the input current only for a small conduction angle as occurs in old-fashion rectifier

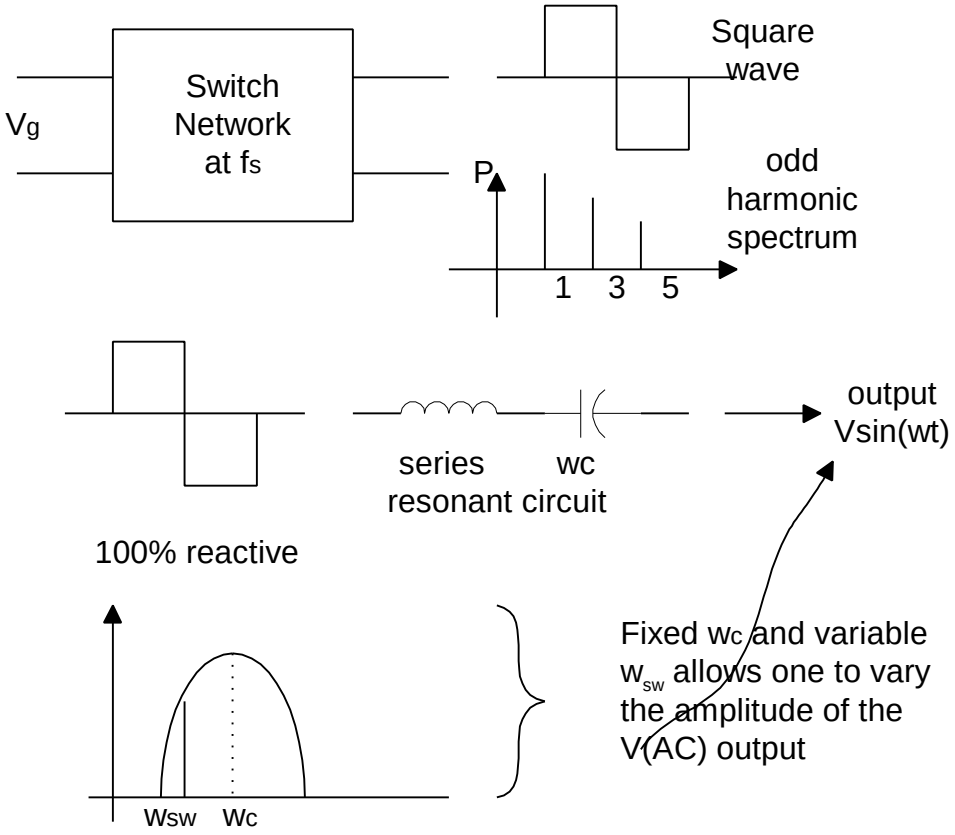
circuits. Below we outline the switch-mode circuit solution we have discussed before in first semester. We only schematically indicate the feedback loop, which makes the input current track the input voltage.



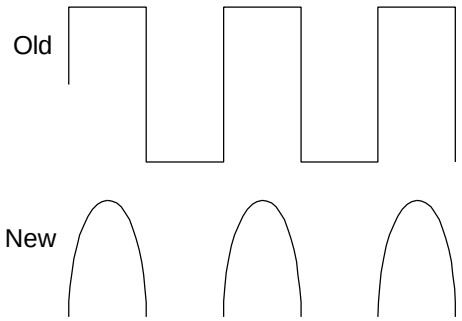
A feedback loop will ensure $i_g \propto V_g$ and no harmonics are drawn from the mains as occurs in prior art rectifers. By means of feedback loops as we will detail in chapter 15 of Erickson $\Rightarrow$ input port looks resistive to the mains ac for low EMI

4. Resonant Converters: dc ® ac

Resonant converters convert DC into AC at any arbitrary frequency and voltage level. We will show below the use of feedback circuits in switch-mode resonant converters to regulate the output voltage. This is another example of the need for good AC models of the switch mode circuits if we expect to be able to design-in the dynamical performance we desire.



We use feedback to vary f_{sw} and thereby vary $|V| \sin w_{swt}$ so one can also replace the above V_g (input dc) plus switch generating a square wave by a clever resonant switch cell that generates half-cycles with fewer harmonics.



Full voltage switching
$f_{sw} \approx 300$ KHz
Zero crossing switch on a Resonant Oscillator.

See IEEE Spectrum Dec 96 pgs. 33-39 for a very nice update! In this article $f_{sw} \approx 3$ MHz. Why so high a f_{sw} choice is made?

Higher f $\Rightarrow$ smaller L and C. But what is assumed here? We also note that low cost zero crossing control chips are commercially available. All of the above hopefully motivates the need for feedback control.

5. Open Loop Disturbances

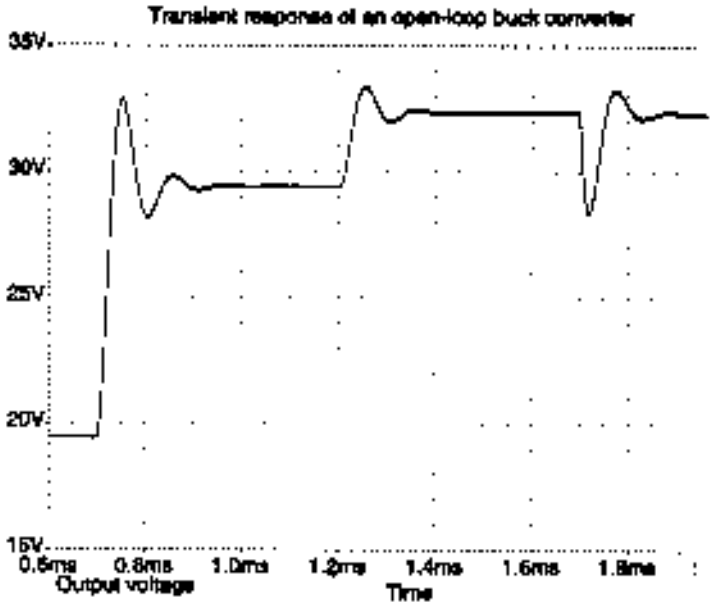
If not yet convinced of the merits of feedback, consider the open loop behavior of a buck and a flyback circuit to external disturbances as modeled or measured below. The two output versus time plots below shows buck and flyback circuits that experience three separate open loop tests which will be performed sequentially in time.

1. Switch D from 0.4 to 0.6 as shown below or at a low frequency modulation f<f_{SW}

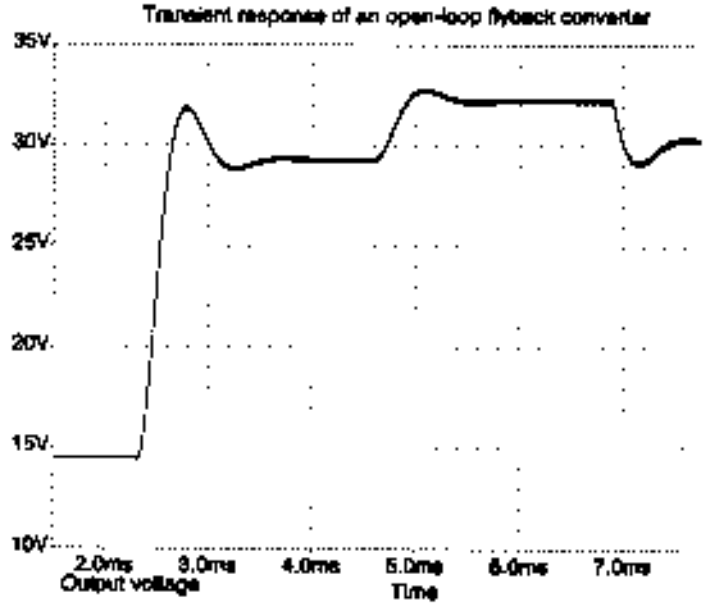
2. Suddenly increase V_{in} by five volts

3. Suddenly decrease R_L by 25%

We do the three sequentially in time starting with the buck converter circuit below



Next we do the same three open loop disturbances to the open loop flyback converter.



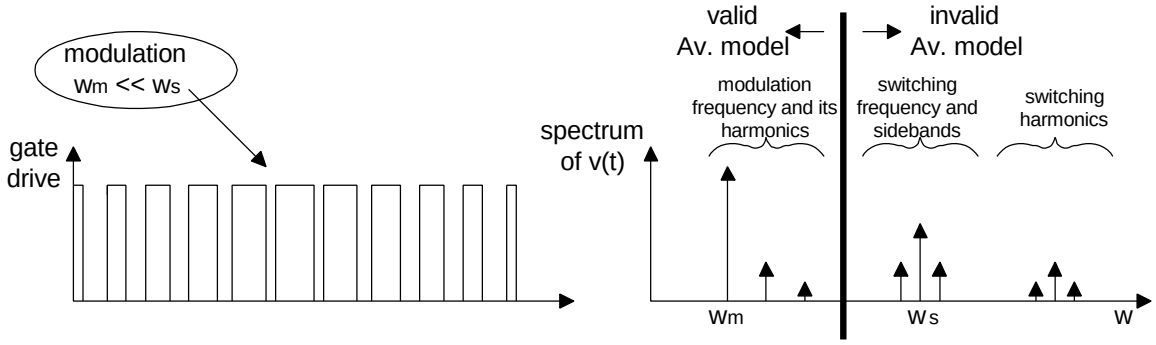
Feedback control of these two circuits would make these disturbances self-correct in a short settling time.. But feedback brings with it the danger of instability or oscillation. Nothing in the open loop response plots of output versus time that the two above systems are prone to instability, which they both are, nor that they are non-linear which they both are. This information ,however, is readily apparent from their closed AC response. We will learn to calculate and displaythe AC response which contains two poles as we shall see in later lectures.

6. Required data to design proper feedback loops.

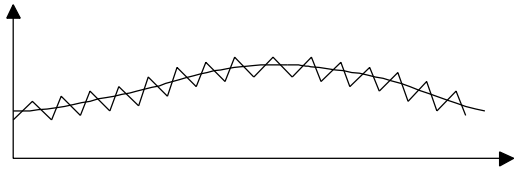
$$A_{CL}(f) = \frac{A_{OL}(f)}{1 + A_{OL}(f)\,b(w)}$$

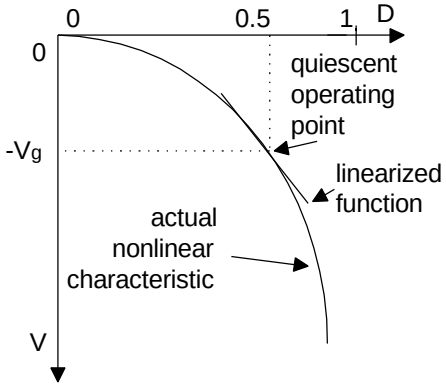
We need good ac models to obtain $A_{OL}(f)$ in the design phase to proper understanding of the closed loop

response with the use of feedback.
$A_{CL}(f)$ can be predicted from the open loop characteristics using linear system theory. We can then estimate the Transient Response for $A_{CL}(t)$ to insure that all transients do not exceed any system specification. We can also check to see from $A_{OL}(f)$ that Z_{in} high enough at all operating frequencies and that Z_{out} low enough at all expected frequencies. In the simplified AC model via $<>_{Ts}$ averaging we find only a limited range of frequency for validity but linear models allow use of all prior linear system tools. Our models will be valid only for $f << f_{sw}$.



This limited f range still allows for useful control. Key is use of operating point to linearize about quiescent values.





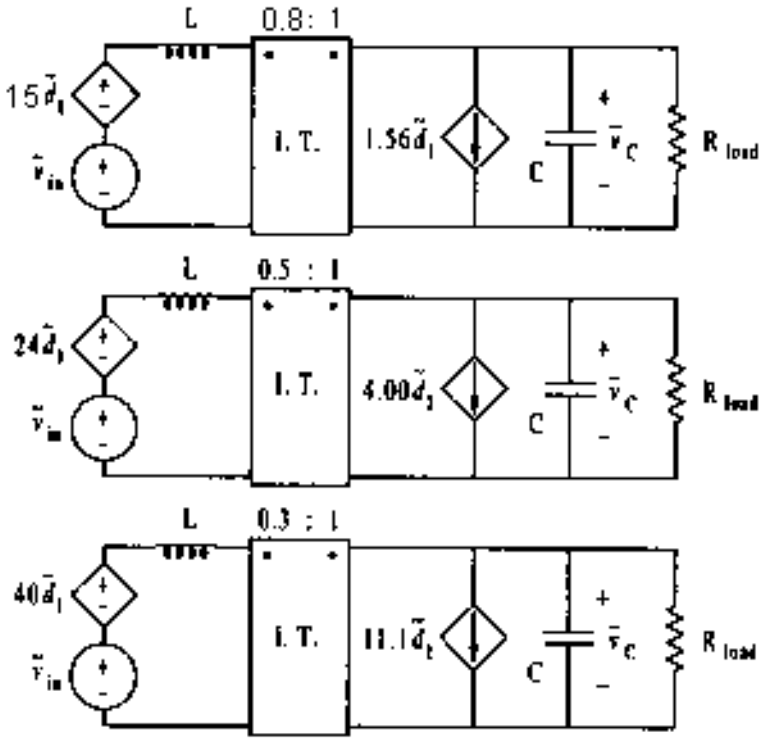
The problem is that the AC transfer function model values will change with D(DC) chosen as we will see in lectures 41 and 42. We anticipate these results below using a boost model:.

Consider a boost converter with 12V input and a 12Ω load resistor. The nominal DC operating points are in the table below and the AC models are different for the three DC cases.

Boost Converter Nominal Operating Points for D_1 = 20%, 50%, and 70%

D_1	$1 - D_1$	V_{out} (V)	I_{out} (A)	I_{in} (A)
0.20	0.80	15.0	1.25	1.56
0.50	0.50	24.0	2.00	4.00
0.70	0.30	40.0	3.33	11.11

The three corresponding small signal AC equivalent circuits for small signal analysis of the boost are shown below. Our point here is to emphasize that the AC models we will derive in lectures 41-44 will depend on the chosen DC operating point



We will end this lecture with a discussion of the pulse width modulator circuit introduced in first semester that plays a key role in voltage feedback schemes for switch mode circuits.

Finally, For HW#3:

1. Answer any Questions asked throughout lectures 40-44.
2. Chapter 7 Problems 1, 2, 3, 12 and 17(Buck-Boost only).