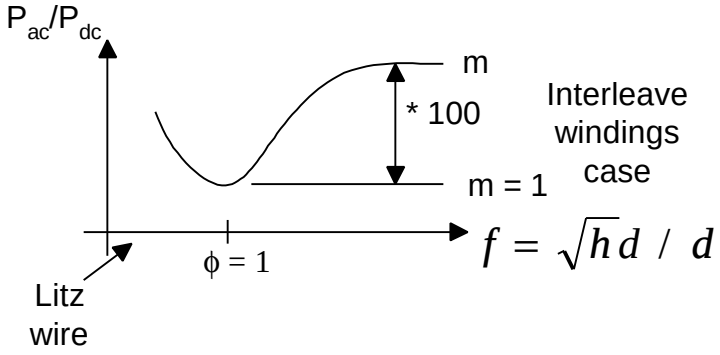
Lecture 29
Total Losses in Magnetic Components, the Heat Flow Balance and Equilibrium Temperatures

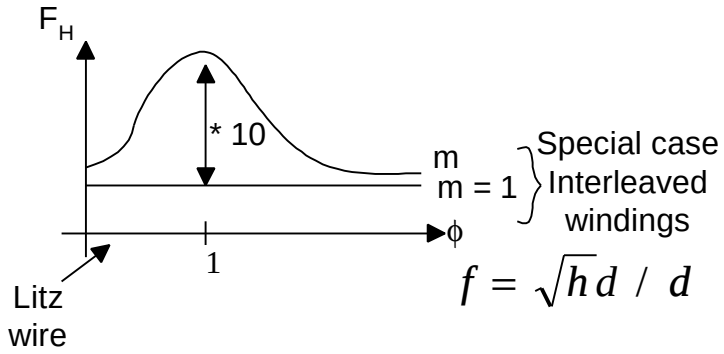
A. Review of Increased Loss in Transformer Wire Windings versus the wire parameter f and effective winding Factor M

1. Sinusoidal Current Excitation Losses in Wire Windings



Note at a wire parameter **f = 1 we achieve minimum loss for a winding**. For larger ϕ values wire losses can be 100 times greater.

2. Square Wave Current Excitation of Wire Windings: Effect of Harmonics on Wire Loss



Unfortunately we have increased losses in

stacks of wires at $\phi = 1$ for current waveforms with large harmonic content of from 1-10 times.

B. Parallel Windings at High Frequency

1. **Paralleled Layers:**
2. **Interleaved Windings**
3. **When does Wire Paralleling Succeed**
4. **Passive losses**

C. Introduction to Thermal Limits

1. **Overview of Thermal Issues**
2. Rule of Thumb: 100^{o}C Maximum Temperature
3. Thermal Loop Equations Via Illustrative Examples

Lecture 29
Total Losses in Magnetic Components, the Heat Flow Balance and Equilibrium Temperatures

A. Power Loss in Transformer Wire Windings For Sinusoidal versus Harmonic Currents

1. **Review of Method for Sinusoidal Current versus the Wire Parameter " f" and the Wire Winding Factor "**M"**.**

In short the enhanced wire winding loss due to eddy currents as outlined in Lecture 28 involves the following:

- Construct MMF Plots in core winding window versus "x" from CHOSEN primary/secondary winding design. This **sets the parameter M** in proximity effect loss nomographs. M is roughly proportional to the magnetic field and eddy current loss goes as V^2/R. Faraday's law shows V~B. Hence loss goes as M^2.
- Choose the wire size and calculate both **the Wire Parameter " f" and** J_{rms} in each layer of windings employed.

The preliminary wire loss per unit volume $J^2_{rms}\,\rho$

However, skin and proximity effects with multi-layer windings will increase the power loss depending on chosen wire parameter "ϕ" and M values as we learned in Lecture 28.

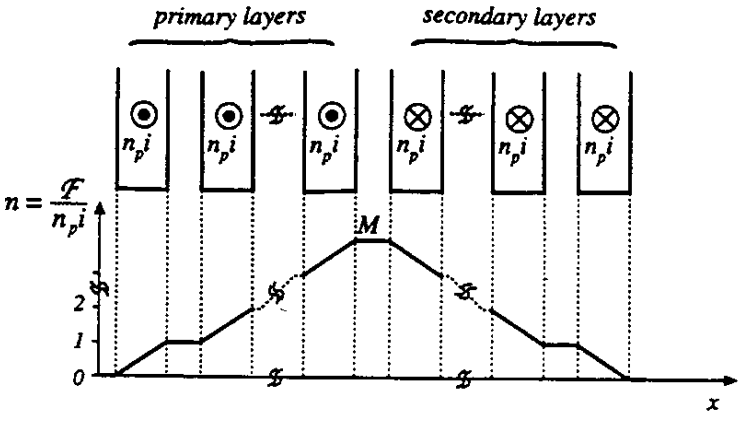
For achieving minimum wire winding loss per unit volume, $J^2_{rms}\mathbf{r}$ we must do three things in the transformer wire winding design:

1. Minimize the # of winding layers that are stacked on top of each (if we do not inter-weave other coils) so that the effective M is as small as possible.

2. By choice of wire size, make the wire parameter $\sqrt{h}\ \frac{d}{d} = f \rightarrow 1.0$. Due this by choosing the wire diameter d(wire) ≈ δ or less.

3. Interweave winding layers of primary and secondary so MMF is a minimum in the winding window due to canceling mmf. We can interleave coils for achieving : M = 1..

Consider below M layers of n_p turns each layer and plot mmf vs x in the wire winding window. We first consider the non-interleaved case of 3 primary winding layers followed by 3 secondary winding layers. First we stack 3 primary coils, followed by 3 stacked secondary coils as shown below. We have assumed below that the current flow in the wires occurs uniformly across the wire diameter, as would occur when the wire size exceeds the skin depth. **Hence, the H field inside the wire increases as we pass through the wire and slowly decays once outside the wire as 1/R.** We assume wires are wound tightly and R is small so the H field appears constant outside the wires to a first approximation.



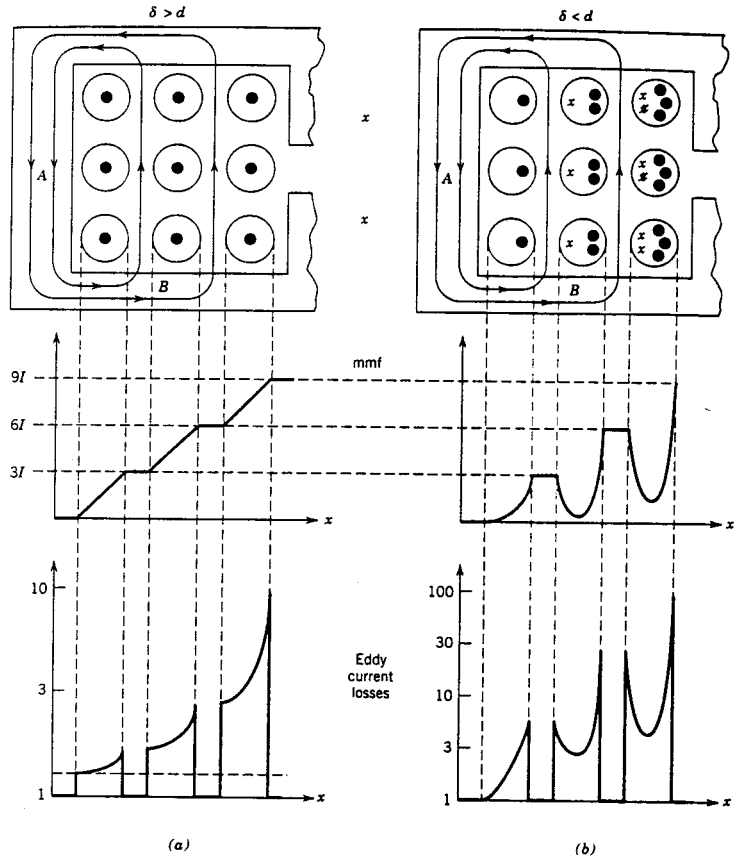
The increased loss factor F_R is obtained from Figures or nomographs of:

F_R versus ϕ and M.

$Q'(\phi,m)=(2m^2-2m+1)G_1(\phi)-4m(m-1)G_2(\phi)$

Note how H in the winding window versus x builds up as we have a stack of primary wires act collectively and then declines as we encounter a stack of secondary wires acting in the opposite way. On the next page we will contrast this MMF profile to that achieved when wire diameter is much greater than skin depth at

the applied frequency of the current flowing in the wire. On the



left is the uniform current density current flow in the wires for low-frequency current flows. On the right is the non-uniform current density plot for the high-frequency current flow case**. Note the 10x change in scale of the eddy current loss.**

We use Ampere's law to see that the MMF inside the wires is sharply peaked for the non-uniform current flow. Moreover the peaking increases as the wires see more total magnetic field. This is because the eddy currents in the wires are driven by the B^2 factor. The eddy currents decrease the current density on one side of the wire and increase it on the other as seen on the right – hand side current profiles. This increased surface current flow with associated mirror currents on opposite sides of the wire causes increased eddy current losses, even though the net current through the wire is unchanged as shown above.

The increased loss F_R factor varies for each choice of wire of diameter (d) and also for the wire insulation chosen(η) as well as for the sinusoidal operating frequency (f) through the F_R curves versus ϕ as obtained from the proximity loss curve below:

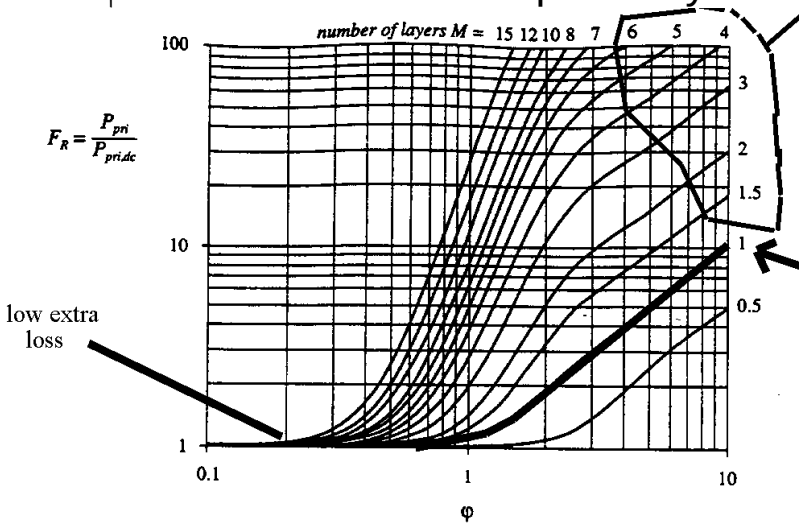


Fig. 12.35. Increased winding total copper loss in the two-winding transformer example, as a function of φ and number of layers M, for sinusoidal excitation.

Multi-winding with extra loss due to proximity effects which go roughly as M^2.

Low additional loss M = 1 case for interwoven primary and secondary windings

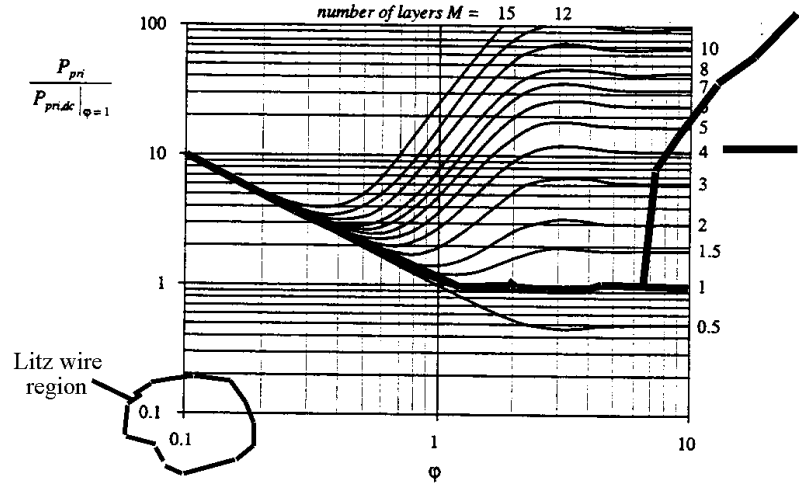


Fig. 12.36. Transformer example winding total copper loss, relative to the winding dc loss for layers having effective thicknesses of one penetration depth.

M = 1 interwoven primary and secondary winding case.
For the m = 5 case choose a conductor diameter at the operating frequency such that $\sqrt{h}\ \frac{d}{d} \approx 0.7$ on the "ϕ" scale to obtain minimum loss. If current is a square wave, the harmonics have higher "ϕ" and higher associated losses.

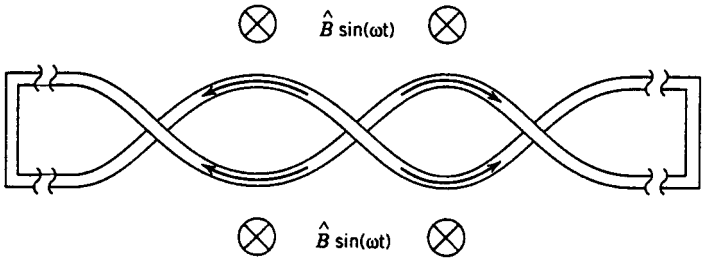
The loss graphs above are for sinusoidal winding currents only. In the first plot we considered only the increased AC losses only

and assumed DC current levels were small, as would be the case in a transformer. In the second plot we took into account the DC losses, such as may be encountered in an inductor. DC losses may be inadvertently increased it we only concentrate on minimizing AC losses. That is minimizing AC loss alone may require too low a wire diameter for the DC component, increasing it's contribution to overall loss. All of the above reviews the situation detailed in lecture 28 where we wish **to reduce AC loss without increasing DC loss**.

For overall DC plus AC minimum copper loss in the magnetic device we must:

1. Operate with "ϕ" = 1
2. Interleave primary/secondary windings so M = 1
3. Place Cu wire in the core window at spatial locations where mmf is minimum
4. Minimize the number of layers of wire windings, M

One way to achieve the elimination of eddy current losses and not increase DC loss is to employ Litz wire as shown below. Litz wire employs many strands of small diameter wire (less than the skin depth) to achieve an equivalent wire area for DC currents. The wire is twisted or woven as a rope so that each wire sees, on average less magnetic field. The induced eddy currents are in

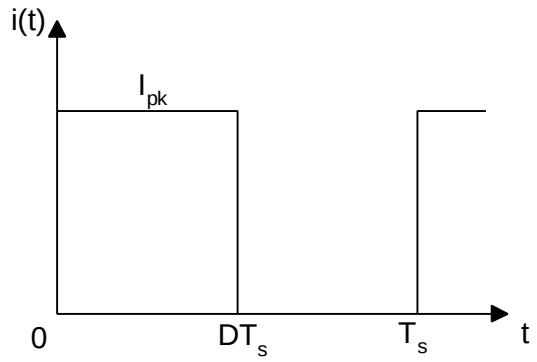


opposite directions in each half–twist of wire as shown.

What if the winding current is a square or triangle wave and not a sinusoid? These waveforms are more common in PWM switch mode circuits than sinusoids. How much further does the

loss increase due to harmonics? We will call this increased wire winding loss, the harmonic factor F_H.

2. PWM Current Waveforms: Square Wave Current Drive Case



The effective dc value of the square wave is $Di_{pk} = I(DC)_o$

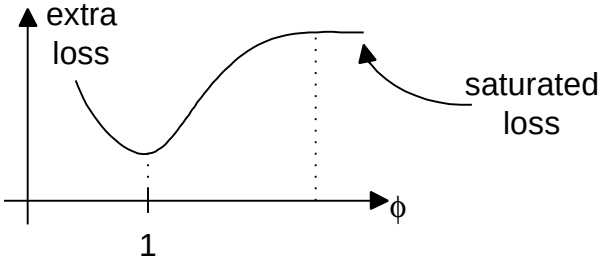
$$i(t) = I_o + \sum_{j=1}^{\infty} \sqrt{2}\, I_j \cos(jw\, t)$$

The harmonic spectrum of the square wave varies with chosen duty cycle of the square wave.

$$I_j = \frac{\sqrt{2}\, I_{pk}}{jp} \sin(jp\, D)$$

the amplitude of the j^{th} harmonic in the square wave goes as:
$I_j \sim 1/j$

Our extra proximity loss plots vs wire parameter $f = \sqrt{h}\ \frac{d}{d}$ for pure sinusoidal excitation have the general shape shown below versus when normalized by DC loss. That is around $\phi = 1$ we find a minimum in the expected extra loss factor due to proximity of nearby windings causing cooperative mirror currents to appear.



But "ϕ" equal to unity does not occur for the harmonics increasing the loss for all the harmonic components of the squarewave.

Case #1 If we choose wire size such that with sinusoidal drive ϕ (@w) = 1, then harmonics from square wave excitation have extra loss, as compared to the fundamental. This occurs because "ϕ" will increase above unity for all harmonics, drastically increasing total loss which includes the fundamental and all the various the harmonics.

Case #2 If we purposefully choose the original wire size such that with sinusoidal drive "ϕ "(w) > 1, then the addition of harmonic currents will have less of a change in total loss. Harmonics have little extra loss in this high ϕ case compared to the fundamental because loss saturates at high ϕ . Loss only increases between ϕ =1 and saturation.

In summary, the wire parameter, ϕ, for the j^{th} harmonic varies as:

$f_j = \sqrt{j}\ f_1$ but loss also depends on M, the effective number of a wire layers as well as the chosen duty cycle of the square wave. In short we define a new multiplicative loss factor F_H as:

$$F_H\left(\begin{matrix}\text{harmonic}\\ \text{loss}\\ \text{factor}\end{matrix}\right) = \frac{\sum_{d}^{m} P_j}{P_1}$$ - extra wire loss due to harmonics

Now including both the fundamental and harmonics the total increase in winding loss versus frequency for a square wave current with dc component, I_o, and fundamental square wave component I_1 is: $P\left(\begin{matrix}\text{winding}\\ \text{loss}\end{matrix}\right) = I_o^2 R_{dc} + F_H F_R I_1^2 R_{dc}$

F_H - depends on both the interleaved or non-interleaved winding choices as well as on the harmonic spectrum of the square wave which is primarly a function of the duty cycle f(D).

F_R – depends on sinusoidal loss curves vs the $\phi_1(w_1)$ wire parameter.

If we define Total Harmonic distortion of a waveform containing harmonics as:

$$\equiv \frac{\sqrt{\sum_{d=2}^{\infty} I_j^2}}{I_1} \equiv THD$$

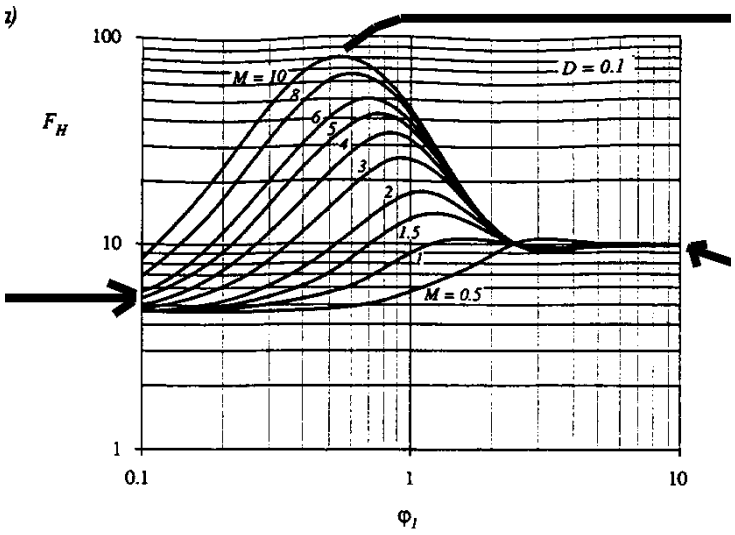
Then we find for square wave case of various duty cycles the following general trends:

D	THD	$1+(THD)^2$
.1	191%	~5
.3	76%	~1.5
.5	48%	~1.25

Graphically we plot the factor F_H for a square wave versus "ϕ " with M and D as parameters just below:

Case #3: D = 0.1 and THD ~ 200%

The F_H factor limit for low ϕ $1+(THD)^2$? 5



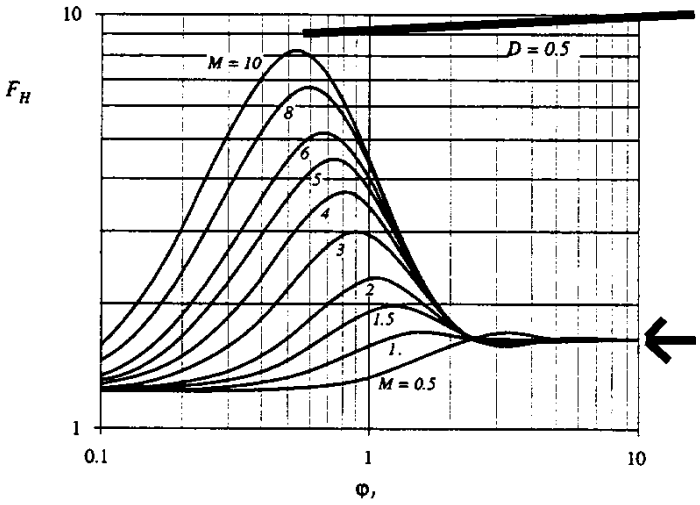
F_H peaks for $\phi_1(w_1)$ ~ 1 by roughly 10 times from high ϕ saturated value

For large ϕ_1 the F_H factor is saturated at *10

Note above for the desirable M=1 wire winding situation very little F_H peaking versus ϕ occurs.

Below on page 11 we will plot the case for D=0.5 and see a very different saturation value for F_H=1.5 , rather than F_H= 10 above. This emphasizes the complexity of wire winding losses for inductors and transformers employed in switch –mode converters.

Case #4
D = 0.5 and
THD ~ 50%



F_H peaks for $\phi_1(w_1)$ =0.6 by only a factor of10.

limit for low ϕ
$1+(THD)^2$
~ 1.25

For ϕ (w_1) larger than unity F_H saturates at 1.5

Choosing a high ϕ_1 value, via proper original wire choice, is the best route to achieve a low F_H factor at a given frequency. We first achieve high ϕ_1 by recalling the relation:

$$f = \sqrt{h}\ \frac{d}{d}$$

1. Using a larger diameter wire, d, compared to the skin effect dimension at the operating frequency, $\delta(f)$.
2. Interleave primary and secondary windings. So as to keep M small - say 1.0 to avoid F_H peaking versus "ϕ"as shown in F_H plots.

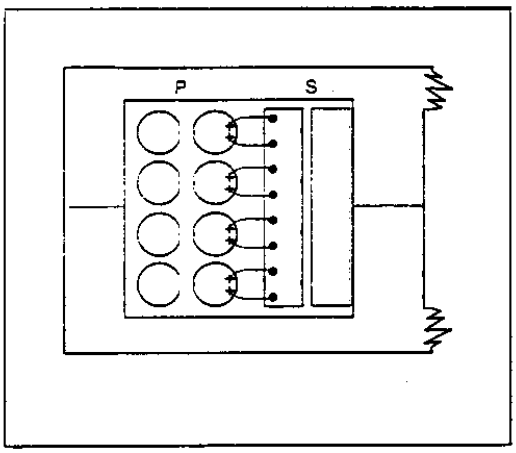
B. Parallel Wire With High Frequency Currents

This section (pages 11-18) is beyond the goals of the course it is optional and need not be read. It may give you nightmares if you are a novice transformer designer.

1. Paralleled Layers:

The transformer shown below has the wire winding layers reconfigured in parallel. A very shocking effect will occur due to minimization of magnetic energy in the primary and secondary coils that you may find unbelievable. Consider first the primary winding, with a

total current in the cross direction of 2 Amps. In the primary there are two parallel wires in each turn as shown on page 10. In the secondary there is a 1-turn, 8a secondary made again of two parallel wires. The intention is to have 1A in each primary wire that we paralleled and 4A in each secondary strip that we paralleled, but it doesn't happen that way unless the wire diameter is much less than the skin depth. We are not able to see our wiring paths followed by the high frequency currents when the wire diameter is chosen much larger than the skin depth at the applied frequency as we explain below due to proximity effects.



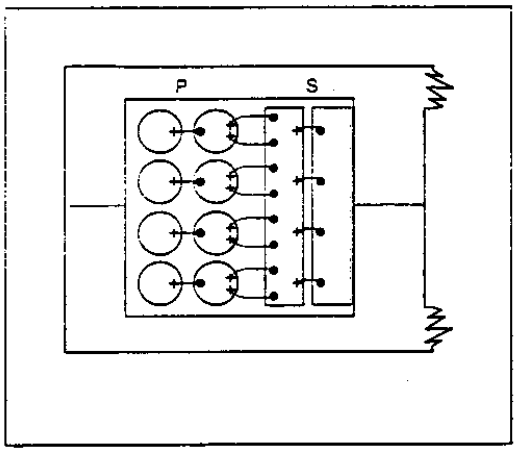
Paralleled Two-Layer Windings

Whenever windings are paralleled, alternative current paths are provided but the currents may not take advantage of the two alternative paths unless the current is at dc or low frequencies. At high frequency, the stored magnetic energy between wires becomes more important than I^2R* losses in the parallel paths. **To our great surprise, all *of the high frequency current components will flow on the inside surfaces of the inner layers directly facing each other as indicated above.***

The high frequency current flowing in the outer layers that we thought were in parallel is *zero-NADA.* Any current that tries to flow in the outer wire layers contributes to an additional magnetic field, between inner and outer layers, requiring additional energy be provided to force this flow. With series-connected layers the current has no alternative - it must flow in all wire layers, resulting in additional energy stored between layers as shown below. When there is an alternative current

path, as occurs with paralleled layers, the high frequency current will flow so as to minimize the total stored energy and current flow in one wire will cease. The leakage inductance between the windings when current flows in only one wire is also slightly smaller than it would have been if the current divided equally between the two parallel. Only a tiny fraction of the available parallel copper is utilized, making paralleling of wires useless.

The series connection and its current flows and magnetic energy storage fields is shown again below to underline the two cases.



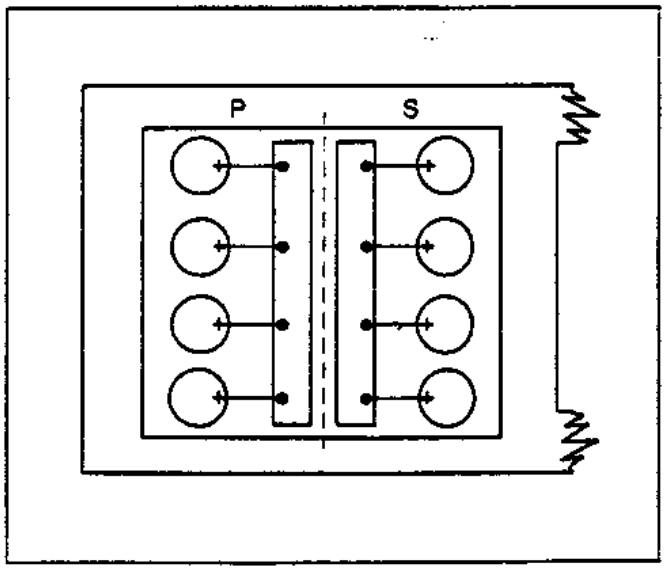
Two Layer Windings -- Series

Consider another mind boggling example: A low voltage high current secondary might use a single turn of copper strap, but the thickness required to carry the required rms current is 5 times the skin depth. It might at first seem logical based on our experience to date to parallel 5 thin strips, each one skin depth in thickness to achieve the required wire. The sad and now anticipated result is that all the HF current will flow in the one thin strip closest to the primary winding. The other thin strips will carry no HF current. If ac current were to flow in the other strips further from the primary, I^2R loss might be less, but more stored magnetic energy is required because the magnetic field energy is bigger (increased physical separation).

Rule: If you provide alternative current paths in parallel in windings do so with care.

2. Interleaved Windings:

There are two primary winding layers and two secondary layers in the interleaved windings shown below. However the magnetic field energy is split equally between the interleaved windings in this case. We must however, actually divide into two winding sections, as indicated by the dashed line between the secondary layers in the figure below. The boundary between winding sections is defined as the point where the total magnetic field goes through zero. Within each winding section below there is a 4 Ampere-turn field introduced by the primary due to current flow in the cross direction and this is canceled by the opposing current flow in the dotted direction in the facing secondary layer as illustrated below.



Interleaved Windings

At the dashed line between the two secondary layers, the total magnetic field is zero. Thus there is one primary layer and one secondary layer in each of two separate winding sections and in this case.

First level interleaving (2 winding sections at a time) is very beneficial both in terms of lowering eddy current loss and minimizing transformer leakage inductance. EMI is also minimized because the fields in each winding section are opposed to each other internally. **The**

only penalty for wire interleaving is increased primary to secondary capacitance. With further levels of interleaving, gains become marginal and the interwinding capacitance penalty is too high. Finally we note that a interleaved winding section structure (P-S-P-S) is often executed incorrectly. For proper balance, the fields should be equal in each of the winding sections. This requires the two interior winding portions have twice the Ampere-turns of the two outside winding portions:(P-SS-PP-S). Is there no possibility of putting wires in parallel for high frequency currents??

3. When does Wire Paralleling Succeed:

Paralleling succeeds when the equal division of high frequency current among the parallel paths results in the least stored energy. Paralleling fails when unequal division of current results in the least stored energy. High frequency current will always take the path that results in the least stored energy.

In the previous discussion, the primary and secondary layers were in series. But the two primary layers and/or the two secondary layers could be paralleled, and the high frequency current would divide equally between the paralleled windings. The field must divide equally between the two winding portions in order to minimize the stored energy = 1/2 BH* geometric volume. If the current and the field were to concentrate in one winding section, then in that one section H would double, and energy density would quadruple. If the field region volume is halved, but net energy would still be double. Therefore current and field will balance nicely in both portions, for minimum energy and (coincidentally) minimum I^2R losses.

To achieve acceptable eddy current losses, it is often necessary to subdivide a wire whose diameter is greater than the penetration depth into many paralleled fine wires. Simply bundling these paralleled fine wires together won't do. Twisting the bundle won’t help much either. Paralleled conductors within one winding section must all rotate through all levels of the winding, so that each conductor has the same induced voltage integrated along its length. A special wire winding technique to

ensure the proper division of current among the paralleled wires is used in the manufacture of Litz Wire.

Bear in mind that when a wire is subdivided into many fine wires to make the effective diameter smaller then the number of layers required correspondingly increased. For example, a single layer of solid wire replaced by a 10x10 array of 100 parallel fine wires becomes 10 layers when entering the loss diagrams.

4. Passive losses

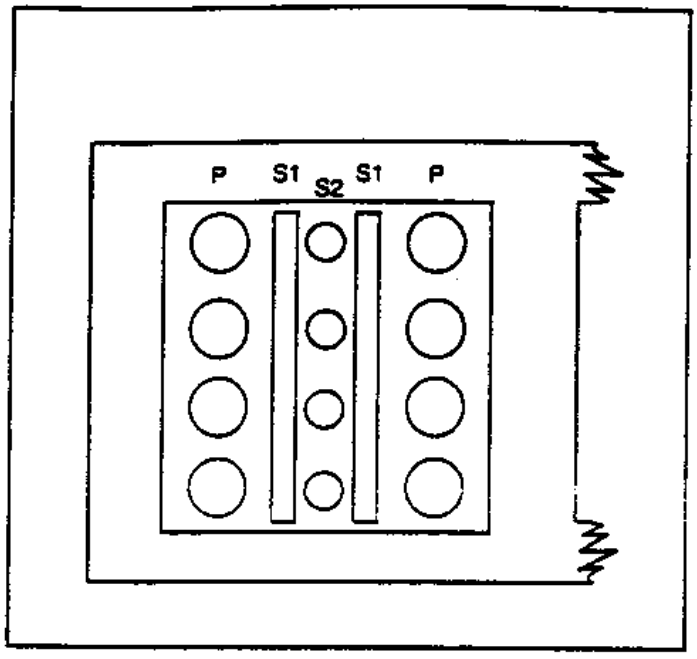
High ac losses can occur in wire windings that are carrying little or no current, if they are located in the region of high ac magnetic field intensity between primary and secondary windings in non-interleaved windings where MMF peaks. Situations of this nature include: Faraday shields inserted to lower EMI, lightly loaded or unloaded transformer secondaries, and the half of a center-tapped transformer winding that is not conducting current at the moment of time the other half is conducting current. The latter occurs in forward converters that employ transformers. If the "passive (no current flow) winding" conductor thickness is not substantially less than the skin depth, the magnetic field cannot fully penetrate the wires. Equal and opposite currents must then flow on spatially opposite surfaces of the conductors, in the passive winding to achieve a net zero current flow. Although the net current is zero in the wires, the mirror surface currents created can be quite high, causing significant additional winding loss even in windings that are not supposed to be carrying current during that portion of the duty cycle.

Passive winding losses can be reduced or eliminated by:

- Relocating the wire windings outside any region of high ac magnetic field intensity. This means fully understanding the MMF patterns in the wire winding core window.
- Reducing field intensity by interleaving windings and by using a core with widest possible wire window breadth to minimize H fields.
- Making conductor thickness substantially less than the skin depths at the operating frequency

Faraday shields may be inserted between windings to prevent electrostatic coupling between primary and secondary. Of necessity they are situated where the field intensity is highest. So they carry very little current, conductor thickness can and should be very much less than the skin depth.

With multiple secondaries on transformers as often occurs, windings should be sequenced so the highest power secondary is closest to the primary. This keeps the lower-powered secondaries out of the highest field region, and has the added benefit of minimizing the adverse effect of leakage inductance on cross-regulation. This winding hierarchy is more difficult to achieve if the primary is interleaved outside of the secondaries. One way of accomplishing this, shown below is to interleave the highest power secondary, S1, outside the lower power secondary(s), S2. The S1 sections (and/or the primary sections) can be either in series or parallel, whichever best suits the number of turns required.



Interleaved Winding Hierarchy

Center-tap windings on either the primary or the secondary side of the transformer should be avoided in wire winding losses are a major

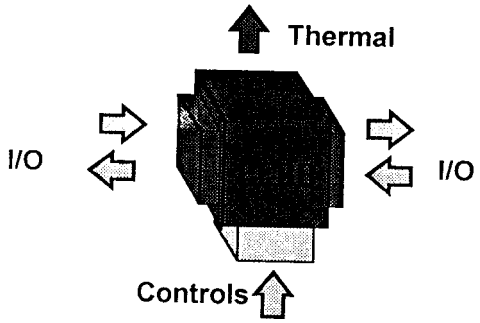
issue. It is usually not difficult to avoid center-tap windings on the primary side, by choosing a forward converter, bridge, or half-bridge topology. But with low voltage secondaries, the importance of minimizing rectifier drops usually dictates the use of a center-tapped secondary winding. We cannot avoid center-tapped secondaries and they usually carry higher currents. In center-tap windings, where one side is inactive (passive) while the other side is conducting, results in poor utilization of the available window area (compared with the single winding of the bridge configuration). The inactive side usually sits in the high magnetic field region between the active side and the opposing windings, thereby incurring large and undesired passive losses.

D. Introduction to Thermal Limits of Power Electronics

1. Overview of Thermal Issues

We need to remove all generated heat to operate a PEEB properly. This requires active thermal management. While information technology electronics carries much less total power the power density limits are similar to power technology electronics. Hence to achieve GHz operation of microprocessors with 10^9 transistors on a die 2x3 cm in cross-section, active heat management is crucial to the success of the chip envisioned. This is an easier task for power electronics as the PEEB building block has lots of room for heat sinks and forced air cooling.

A Power Electronic Building Block (PEBB) is:



Nevertheless thermal management also limits microprocessors.

As a rule we seek to avoid PEEB operation near 100°C for the reasons that follow. At this temperature magnetic cores lose saturation flux capabilities, wire insulation degrades, electronic devices hit the point where minimum doping levels are exceeded by the thermally generated free carriers, and all passive R-C components degrade in performance.

How do we insure this never occurs? Proper air based cooling is our first choice that takes away all heat generated. Water-cooling is not attractive because it complicates power supply design. We need an extra water connection.

- Heat in electronics is a recognized problem

"… Problems facing the industry include testing, validating and heat generation."

Dr. Andrew Grove

Intel President and CEO

—

What is the need for Thermal Management?

– The largest problem in power electronics

– Due to:

- Increasing component heat flux
- Increasing system packaging density
- Increasing market competition

In power electronics we have switches that may transfer 10kW of power with 1% loss for a heat flow of 100W being lost to the ambient in the form of heat. In the case of inductors and transformers heat is generated via both wire I^2R losses as well as core losses. This power input causes

the core/wire volume to heat up. Cooling of the core/wire volume is also provided via heat flow to the ambient. Due to wire winding and core losses the ambient temperature may well exceed 20^{o}C, further limiting the heat flow from the switch.

2. Maximum 100^{o}C System Temperature

The practical issues for T $\leq$ 100^{o}C in a PEEB are:

a. No steam generated in cooling lines, if we ever use water-cooling. Boiling of water causes possible vapor locks..

b. Plastic or varnish wire insulation degrades at T > 100^{o}C causing wires to touch electrically in undesired ways.

c. Magnetic hysteresis Core losses increases for T > 100^{o}C very rapidly or has minimum loss just at 100 ^{o}C.

d. B_{sat} decreases for T > 100^{o}C in the magnetic core materials causing possible catastrophic damage.

e. Si Semiconductor devices degrade performance when T $\geq$ 100^{o}C due to thermal generation of carriers which can dominate over low doping densities fouling-up device doping profiles required to operate switch devices properly.

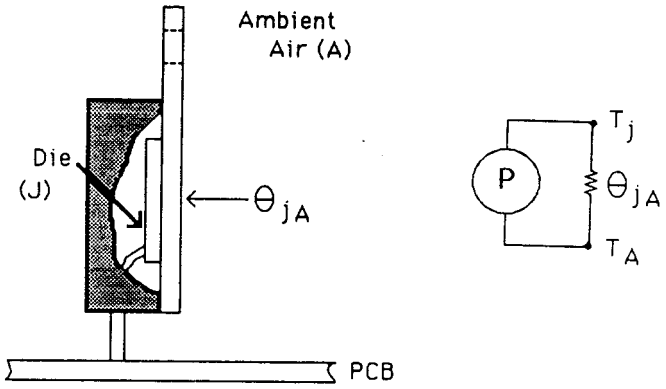
3.Thermal Loop Equations

We solve for thermal heat flows and equilibrium temperatures at various spatial locations via loop equations similar to electrical equations. Thermal analysis is similar to the solution of R-C circuits in the electrical domain. We make the following equivalencies between thermal and electrical quantities:

ELECTRICAL	**THERMAL**
1. Electrical Current	1. Heat Flow in Watts
2. Resistance	2. Thermal Resistance in ^{o}C/W
3. Node Voltage	3. Temperature at a Spatial Location ^{o}C
4. Current Loop	4. Thermal Loop
5. Ground Potential	5. Ambient Air Temperature

Several simple situations present themselves for heat flow and temperature calculations as shown below. For illustration purposes we will look at three solid state devices that generate heat loss. The same could be said of core-winding combinations but the equivalent thermal circuits would not be so clear as for the case of the solid-state devices. We also look only at steady state heat flow, which involves only thermal resistance's. We will, in Lecture 30, consider transient heat flow including thermal capacity as well as thermal resistance, but will avoid this for now.

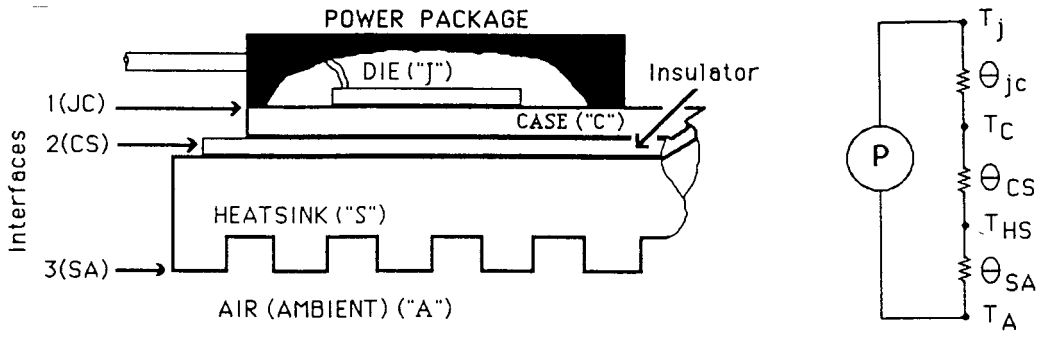
First consider the solid state device connected to a PC board and cooled only by the ambient air as shown below.



The thermal circuit employed to calculate the junction temperature as compared to the ambient temperature for a given heat flow is as shown above. $T_j=T_a+\mathbf{q_{ja}}$ **P(heat flow).** Note that heat flow will be in units of Watts and the thermal resistance, between two points a and j, will be $\mathbf{q_{ja}}$, in units of $^oC/W$. The product of heat flow,P, times thermal resistance will be in ^oC. The absolute ^oC at any location ,j, will be referenced to the ambient temperature as shown above. That is $T_j=T_a+T$(across the element).

In a more complex device, with a heatsink attached, the heat flows in the solid connection between the solid state die to the case and then to the heatsink where it is dispersed into the ambient. The three junctions involved are the die J to case junction, case to heatsink junction and heatsink to ambient junction. At each junction we will have an equilibrium temperature

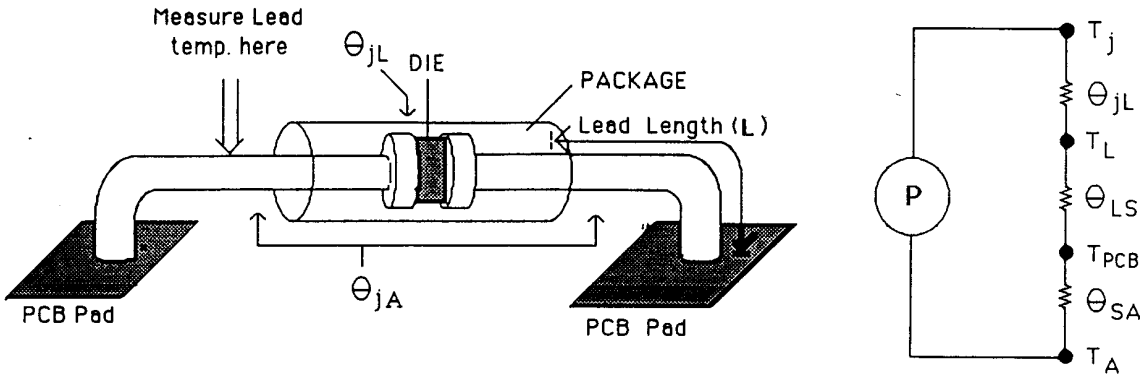
and corresponding thermal impedance connecting the two surfaces, θ_{xy}. The corresponding thermal model and the heat-delivering die are shown below. The junction temperature is given by the thermal loop relation depicted under the figure and the equivalent thermal circuit shown to the left of the figure.



$$T_j = T_A + (\theta_{SA} + \theta_{CS} + \theta_{jC}) \times P$$

Finally we consider the case of a power diode connected to a PC board by thick leads that also conduct heat from the diode to the PC board. S represents the PC board area, L the lead length and J the junction of the diode. In addition there is a parallel path for heat flow form the junction to the ambient air via the path θ_{jA}. Since θ_{jA} is considered so large we neglect it here compared to the heat flow through the diode leads as shown on page 23.

That is we will only consider the simplified series thermal circuit composed of $\theta_{jL} + \theta_{LS} + \theta_{jC}$. The corresponding temperatures are T_j, T_L, and T_A. The heat source representing the combined DC and switch power losses is represented by the term P.



For later reference air based passive thermal resistance's vary form 1 to 100 ^{o}C/W, so that for a 100W power flow at best we will get a 100 ^{o}C temperature rise from the ambient. This may or may not be acceptable.