Lecture 20

Bi-directional Switching Problem Solutions and Overview of Insulated Gate Bipolar Transistor Switches

A. Illustrative Bi-directional Current Problem Solution : Erickson's Problem. 4.1

1. Erickson's problem4.1: Current <u>bi-directional switching</u>

2. Limited quadrants of operation for real solid state switches

- **a.** Two quadrant illustrative problem
  1. **Voltage bi-directional switch example**

3. Four quadrant switch and example

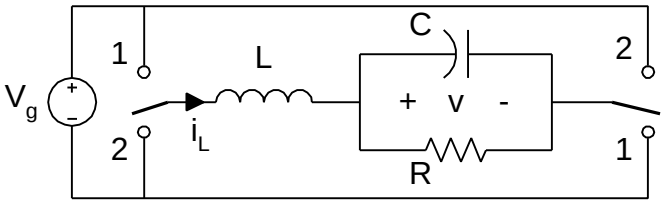
B. Introduction to the IGBT Switch Device Structure and I-V Characteristics

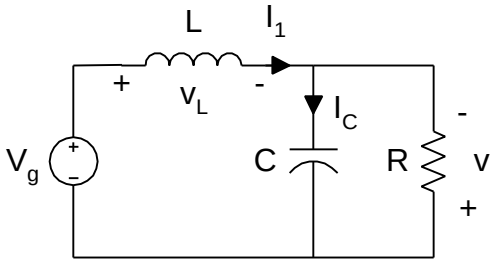
1. **Overview of the IGBT Device Goals**
2. **IGBT Device Cross-sections**
3. **SOA regions and long tail turn-off time of IGBT devices**
4. **Illustrative IGBT Energy loss during switching.**

A. Illustrative Problem Solution : Problem. 4.1

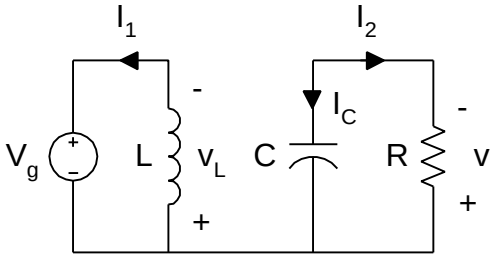
(1) Erickson's problem 4.1: Current <u>bi-directional switching</u>

For Chapter 2 of Erickson in problems #4 & #5 you solved for V_{OFF} and I_{ON} of switches leading to the transistor circuit. Follow the same procedure as your old homework.





SW1 on/SW2 off

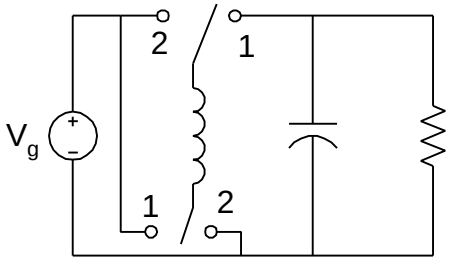


SW1 off/SW2 on

Time DT_s

$V_L = V_g - V$

$$I_C = I_1 - \frac{V}{R}$$



Time $D'T_s$

$V_L = -V_g$

$$I_C = -\frac{V}{R}$$

Volt-sec balance on L: $\langle V_L \rangle = 0$, $D' = 1 - D$

$$D(V_g - V) - D'V = 0 \rightarrow DV_g - Dg + DV_g = 0$$

$$DV = 2\,Dv_g - V_g$$

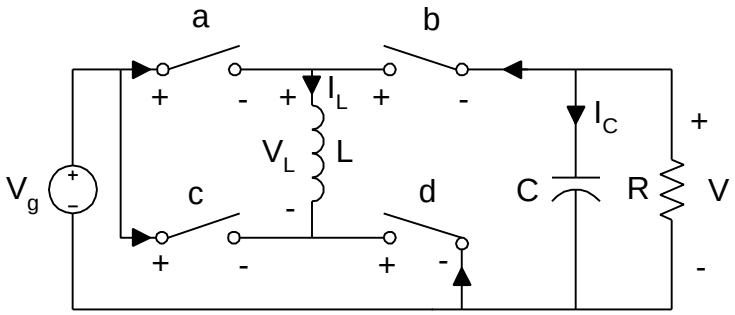
$$V = \frac{V_g(2D-1)}{D}$$ output voltage in steady state

Charge balance on the capacitor: $\langle i_c \rangle = 0$

$$D\left(I_1 - \frac{V}{R}\right) - D'\frac{V}{R} = 0 \rightarrow DI_1 - D\frac{V}{R} - \frac{V}{R} + D\frac{V}{R} = 0$$

$$I_1 = \frac{V}{DR} = \frac{V_g(2D-1)}{D^2R}$$

$D > ½ \Rightarrow$ Gives bipolar current
$D < ½ \Rightarrow$ when on

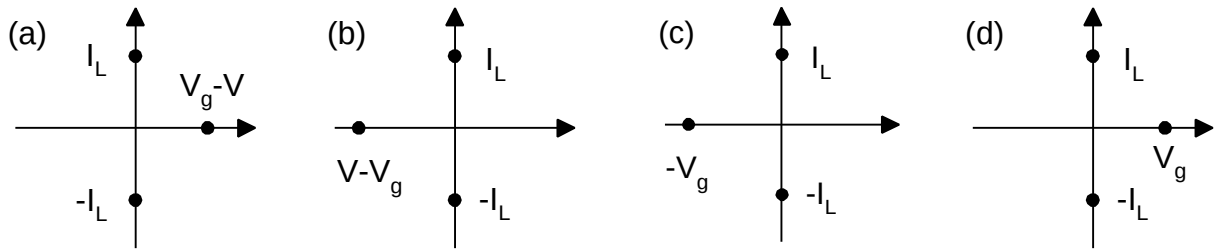


SW a $\rightarrow V_a = V_g - V$
$I_a = I_L$

SW b $\rightarrow V_b = V - V_g$
$I_b = I_L$

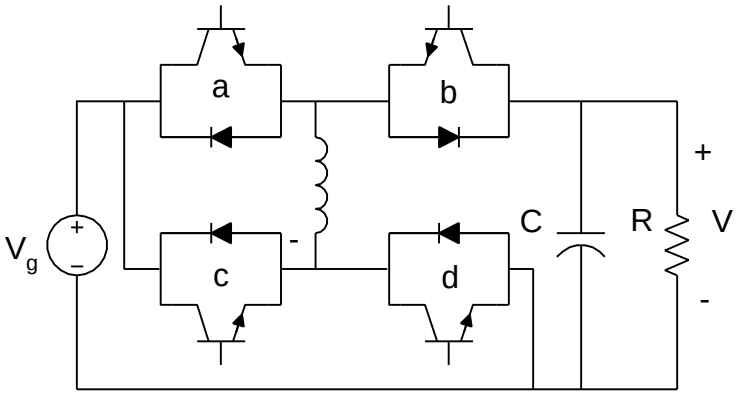
SW c $\rightarrow V_C = -V_g$
$I_c = I_L$

SW d $\rightarrow V_d = V_g$
$I_d = I_L$



KEY: Show why V_{tr}(OFF) is unipolar
$I_L = I_R$ is bipolar

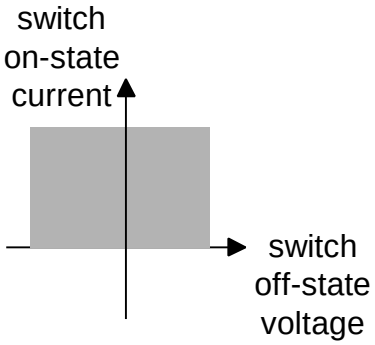
A bipolar implementation of the bi-directional current switch is shown below:



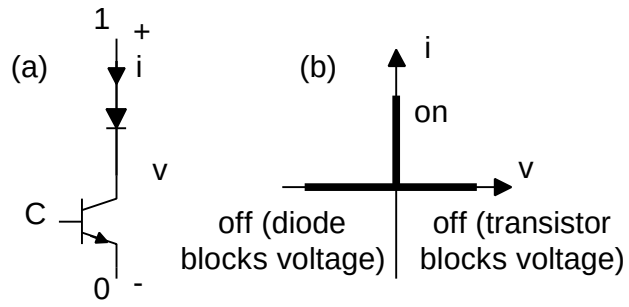
For **HW#4** you do Erickson Problem **4.5** another two quadrant example with bipolar current.

(2) Limited quadrants of operation for real solid state switches

a. Voltage bi-directional switch example

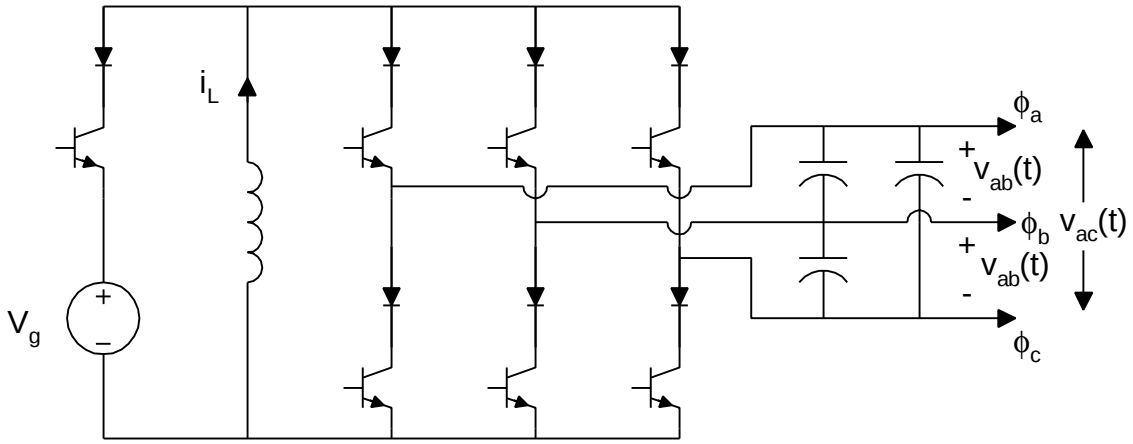


Ideal voltage-bi-directional 2-quadrant switch properties.



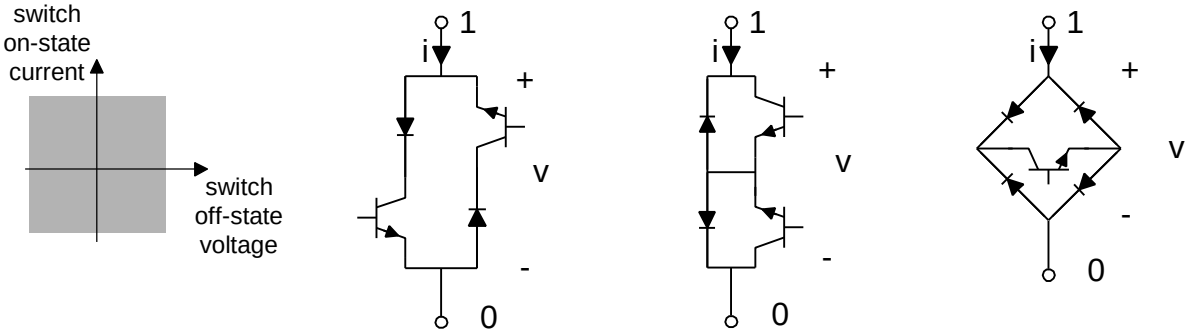
Realizing a voltage-bi-directional 2-quadrant SPST switch:
(a) implementation using a transistor and series diode, (b) idealized switch characteristics.

This voltage bi-directional switch finds use in various circuits such as the buck-boost DC to ac 3ϕ converter below.



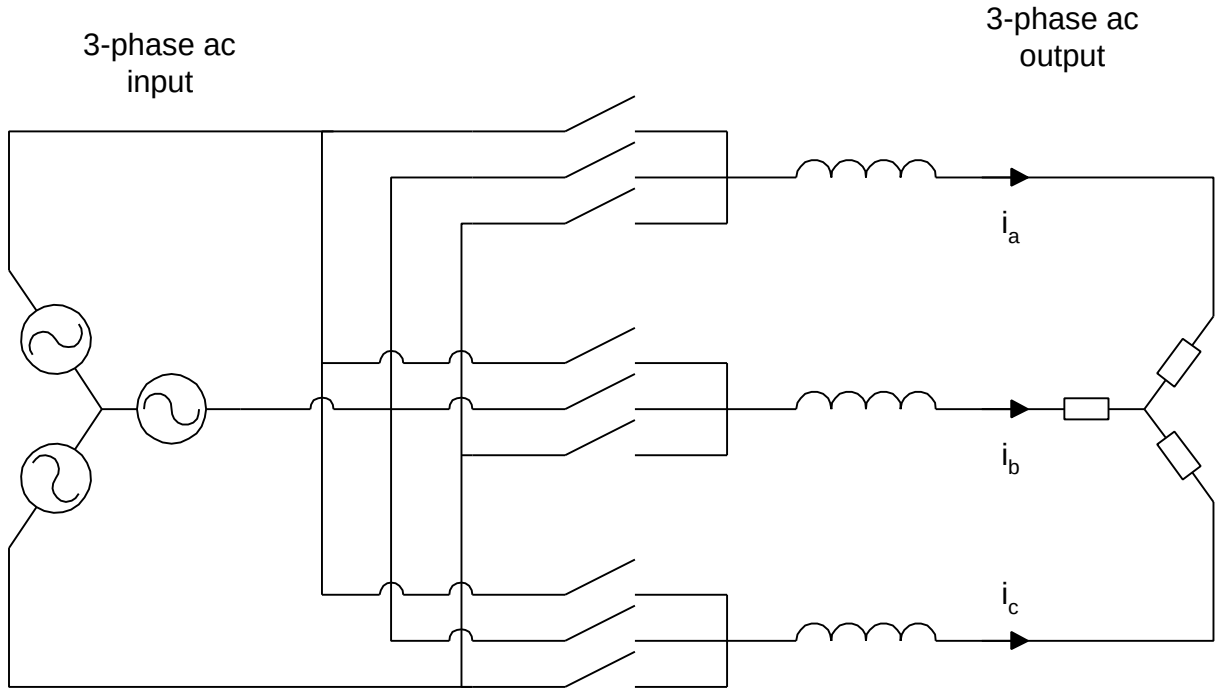
DC-3ϕ ac buck-boost inverter.

(3). Four quadrant real switches can conduct either polarity of current, and can block either polarity of voltage.



These switch topologies find use in 3ϕ mains to 3ϕ voltages @ other frequencies, in short 3ϕ f converters. These could be used for speed control of synchronous AC motors.

Below all v and i are ac therefore 4-quadrant switches are required as ac power could flow in either direction.



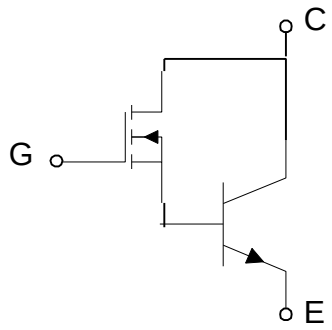
A 3ϕac-3ϕac matrix converter, which requires nine SPST four-quadrant switches.

B. IGBT SWITCH

1. Overview of IGBT Device Goals

Another solid state switch choice besides the bipolar transistor and the MOSFET is the insulated gate bipolar transistor (IGBT). This device was invented to capture the two separate advantages of each the bipolar and the MOSFET transistor in one device. Specifically, the IGFET has the high input impedance of the MOSFET input circuit with the high current and low impedance of the BJT. We will outline below the basic properties of the IGBT as a switch to achieve higher output switch current, lower input gate current and the ability to block both polarity voltages across the device.

Consider the circuit shown below which captures the intent of the device designer.



FET-BJT Darlington connection for low I_G drive power switching

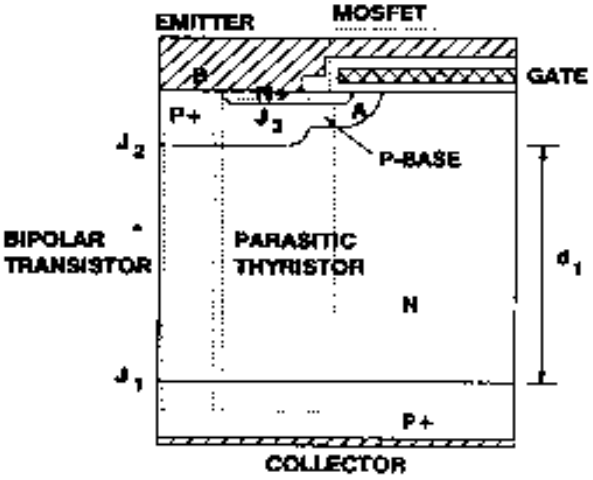
The Darlington combination of an input FET and an output bipolar allows for:

1. Convenient low current gate control on the FET driven by standard analog voltages.
2. Higher output current capability from the bipolar output drive.

The integrated form cross-section is shown below with a PNPN structure that also gives rise to an inadvertant parasitic thyristor(SCR).

2.Device Cross-sections

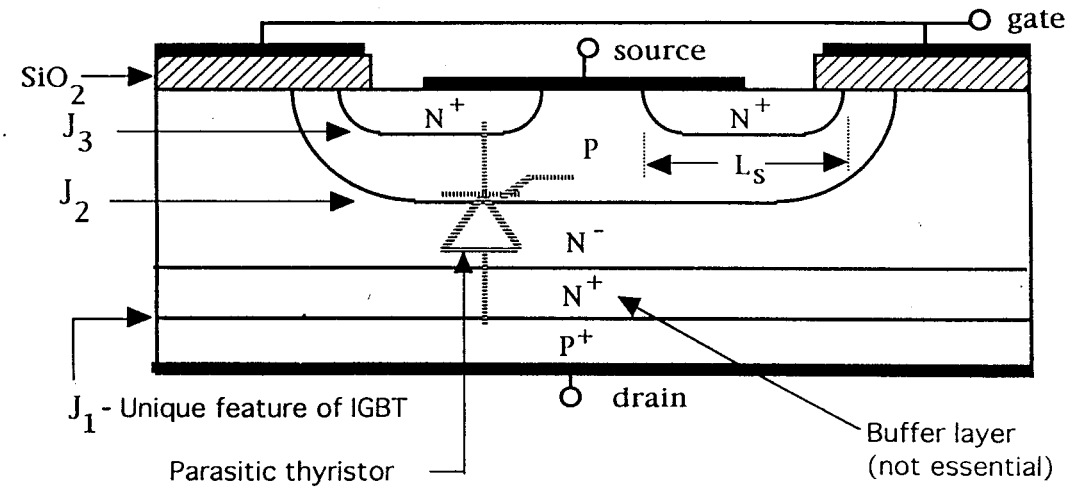
A brief sketch of emitter, collector and MOSFET locations .



IGBT cross section. (From B. J. Baliga, *Power Semiconductor Devices*. Boston: PWS Publishing, 1996, p. 428. Reprinted by permission.)

A little clearer device cross-section that better illustrates the parasitic SCR is shown below.

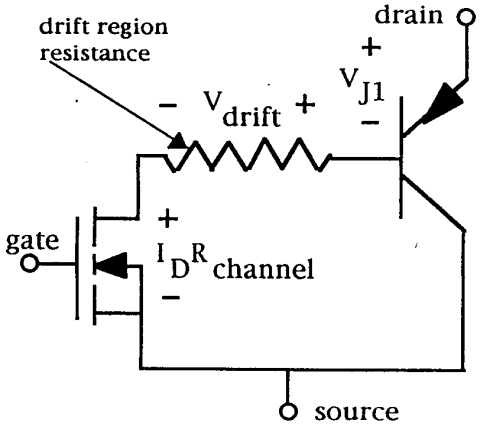
Cross-section of IGBT Cell



- Cell structure similar to power MOSFET (VDMOS) cell.
- P-region at drain end unique feature of IGBT compared to MOSFET.
- Punch-through (PT) IGBT - N^+ buffer layer present.
- Non-punch-through (NPT) IGBT - N^+ buffer layer absent.

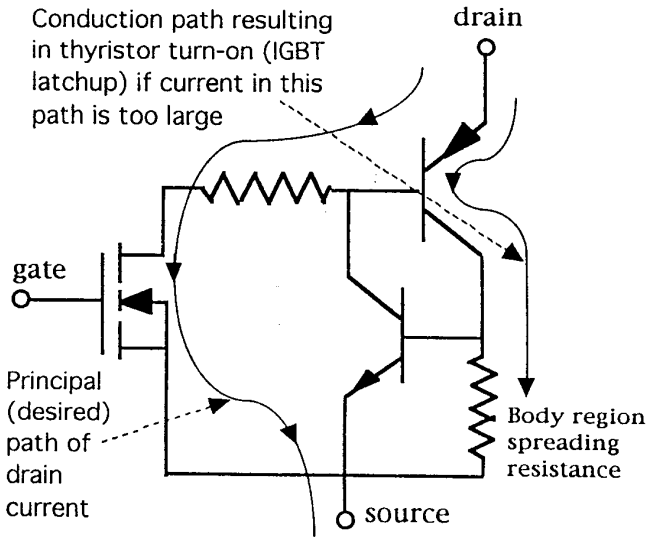
We next employ the dual transistor model of the SCR adding the device resistance in the emitter leg as shown below on page 9 to better explain dynamic performance of the IGBT.

Approximate Equivalent Circuits for IGBTs

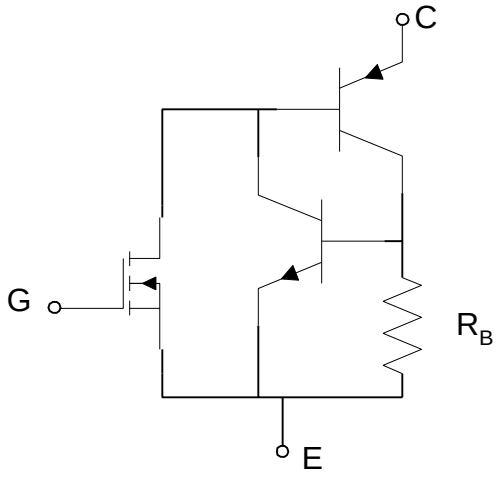


- Approximate equivalent circuit for IGBT valid for normal operating conditions.

- $V_{DS(on)} = V_{J1} + V_{drift} + I_D R_{channel}$



- IGBT equivalent circuit showing transistors comprising the parasitic thyristor.



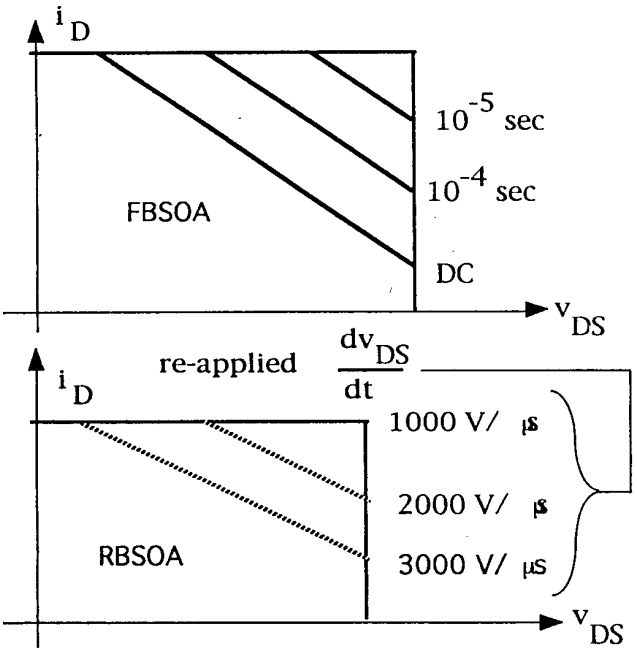
Simple multi-device model for IGBT

Avoidance of thyristor latch-up and avoiding inadvertent turn-on of the bipolar transistor are both important for proper IGBT use.

Also, unlike a pure MOSFET switch the IGBT can block voltages of either polarity. The safe operating area of the IGBT is shown below for both the forward and reverse mode.

3. SOA and long tail turn-off of IGBT

IGBT Safe Operating Area



- Maximum drain-source voltage set by breakdown voltage of pnp transistor - 2500 V devices available.
- Maximum drain current set by latchup considerations - devices reported that can conduct 1000 A for 10 μsec and still turn-off via gate control.
- Maximum internal temperature = 150 °C.
- Manufacturer specifies a maximum rate of increase in re-applied drain-source voltage in order to avoid latchup.

For this capability we pay a price in slow turn-off as shown below.

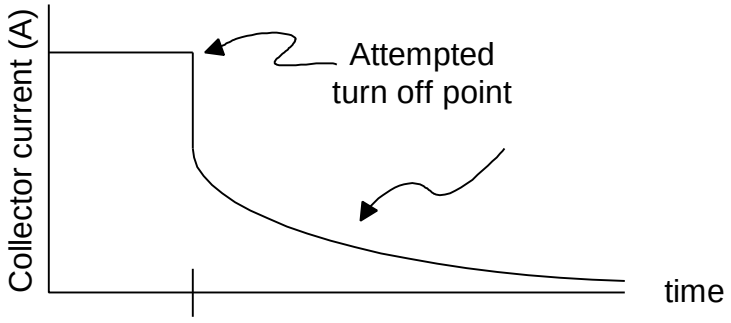
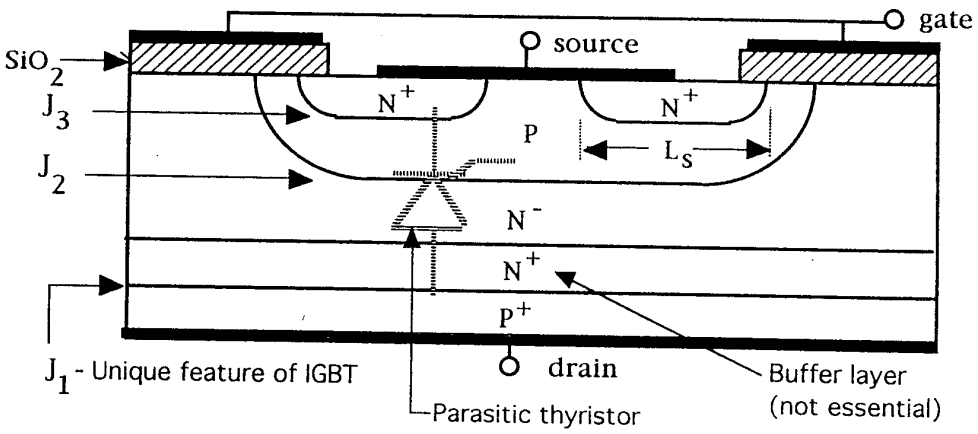


Fig. 13.47 IGBT long tail turn-off current.

The blocking capability and any problems that arise are best discussed after we look at the device cross-section below to see the various regions. Note the THREE JUNCTIONS from the top of the device down. Especially note the J_1 junction at the bottom that distinguishes the IGBT. Also note that the extended drain at the bottom of the cross-section and the two source regions at the top of the cross-section are separated spatially. This is accomplished by a large N^- region of low doping as shown, so we can achieve a LARGE stand-off voltage. Unfortunately, this also introduces the possibility of a parasitic SCR. A N^+ buffer layer speeds up the IGBT turn-off. Below is the cross-section for your perusal.

Blocking (Off) State Operation of IGBT



- Blocking state operation - $V_{GS} < V_{GS(th)}$
- Junction J_2 is blocking junction - n^+ drift region holds depletion layer of blocking junction.
- Without N^+ buffer layer, IGBT has large reverse blocking capability - so-called symmetric IGBT
- With N^+ buffer layer, junction J_1 has small breakdownvoltage and thus IGBT has little reverse blocking capability - anti-symmetric IGBT
- Buffer layer speeds up device turn-off

The static or DC model for the IGBT is a diode in series with a power MOSFET to better explain: forward voltage behavior, low gate current and reverse blocking ability as shown below.

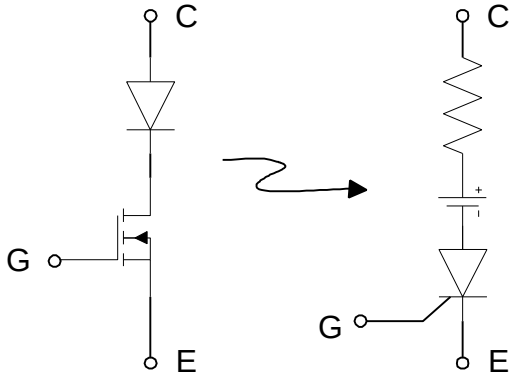
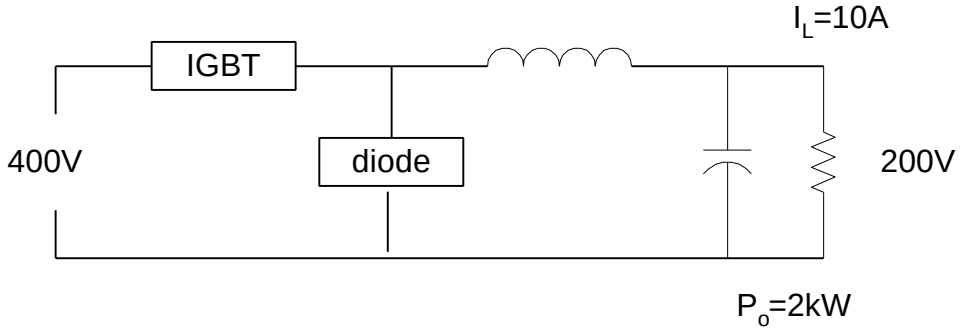


Fig. 13.48 Static model for IGBT

Tradeoffs are made in traditional IGBT manufacture between the static model V_{on} and the turn-off speed. You can get both small only with difficulty. Consider two IGBT specs.

Fast IGBT	**Slow IGBT**
V_{on} = 2.7 V @ 100 A	V_{on} = 1.5 V @ 100 A
W(switch) = 4mJ/switch	W(switch) = 12mJ/switch

When V_{GE} = 10V is applied to the IGBT the turn-on time of 500 ns is similar to BJT but slower than MOSFET's. To turn the IGBT off V_{GE} is set to zero allowing the CGS voltage to discharge to zero cutting off bipolar MOSFET conduction. The parallel bipolar transistor current however falls very slowly (1-20 μs) as carriers are eliminated in the base only by slow carrier recombination.



In summary, the IGBT device replaces the bipolar transistor or MOSFET primarily because with it we can achieve higher V and I switching characteristics by using an IGBT.

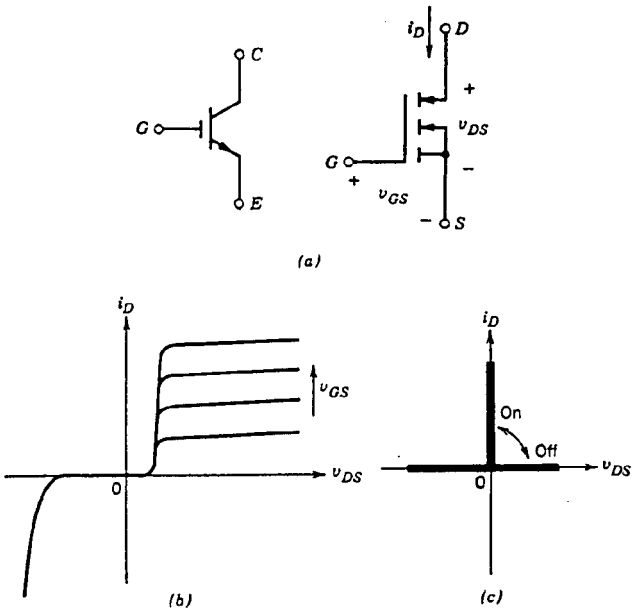


Figure 2-12 An IGBT: (*a*) symbol, (*b*) *i–v* characteristics. (*c*) idealized characteristics.

Instead of a base we have a MOS gate as input.

However, turn-off characteristics of an IGBT are very slow (typically 1-20 μs), causing additional switching loss.

Finally, we note in passing that **MODERN IGBT** device design employs **vertical trenches cut into the bulk silicon and to achieve**

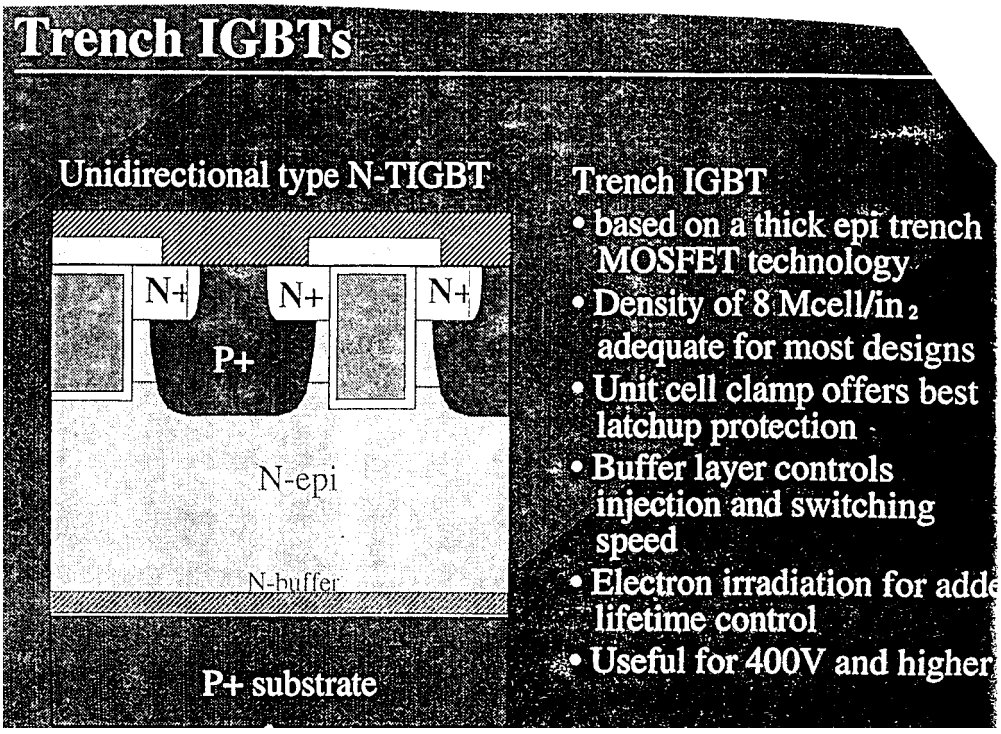
- **An increased density of IGBT cells per unit area because of more confined vertical current flow and less current spreading laterally**
- **Improved latch-up protection fron the parasitic SCR by better confining vertical current flow**

The modern trench isolated IGBT structure is shown on the following page. We will also note on page 14 two tricks to reduce the long turn-off time of conventional IGBT devices: a heavily doped buffer layer to recombine excess charge and post device fabrication irradiation of the device by MeV electron beams to create recombination centers in the bulk silicon and thereby

increase the recombination time for carriers.

- The N-buffer layer lies on the bottom of the device structure

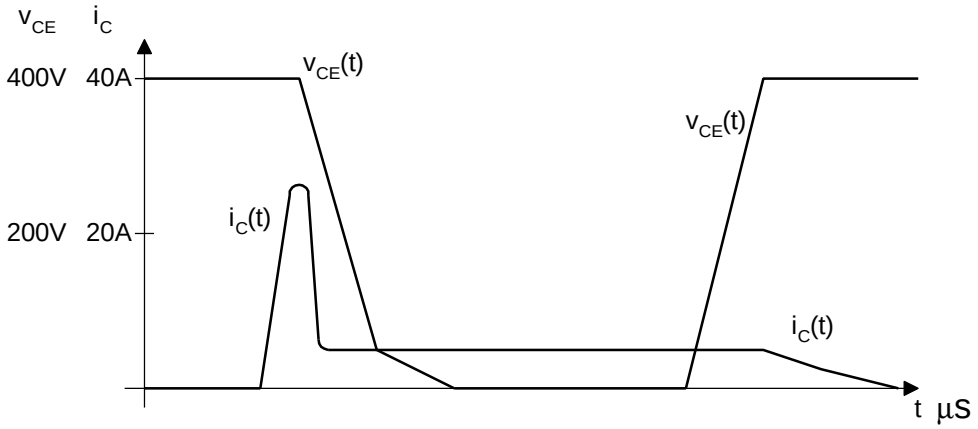
- The MeV electron irradiation is not shown, but it achieves increased carrier recombination times in the bulk silicon



We are now done with our brief overview of IGBT devices. **This review would be a good starting point for a term paper. Please feel free to do a term paper on modern IGBT Design or preformance**

4. Illustrative Problem for IGBT Energy lost during switching.

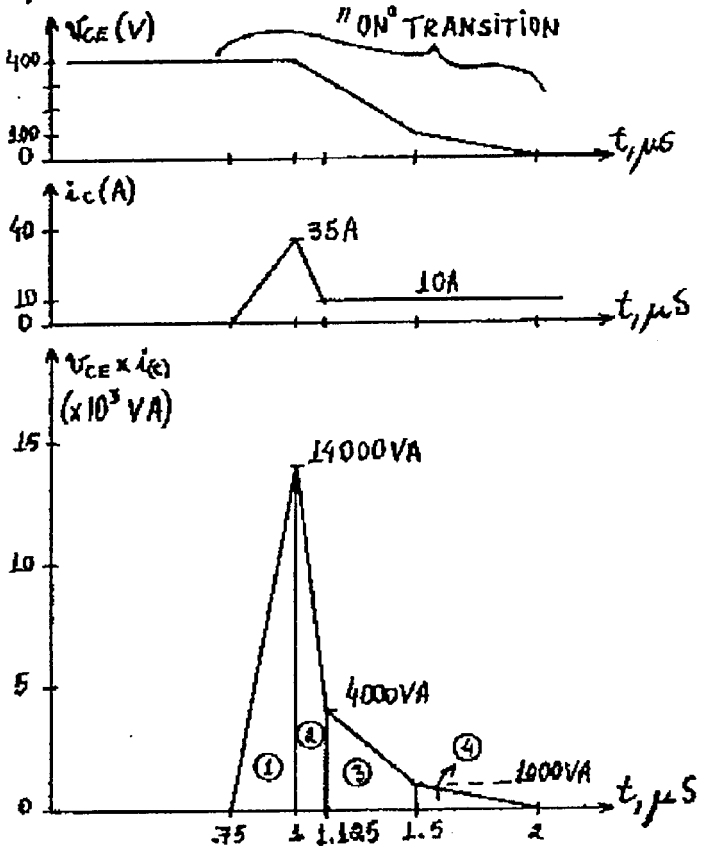
Below on page 15 are V_{CE} across IGBT and I_c out of the IGBT. Note the I_c possesses a long tail in time compared to the rapid change V_{CE} during turn-off. Also the IGBT has characteristic high current spikes**,** due to the internal diode, during turn-on. Both transients cause increased switching losses. Next we outline the solution to Erickson Chapter 4 Pbm. 4.7 which quantitatively illustrates all of the above points.



For a typical IGBT, two very different switching transitions occur in T_s: an on and an off transition as shown above with unique i_c - t characteristics for each.

(1) Given the measured “ON” transition below with current peaking find the energy to switch and the power lost.

a) BUILD DIFFERENT GRAPHS & MULTIPLY AREAS:



SUM AREAS ①, ②, ③ & ④:

① = .5·(14000)·(.25x10⁻⁶) = 1.75 mJ
② = .5·(14000 + 4000)·(.125 x 10⁻⁶) = 1.125 "
③ = .5·(4000+1000)·(.475x10⁻⁶) = 1.1875 "
④ = .5·(1000)(.5 x 10⁻⁶) = .25 "

W_{ON} = 4.3125 mJ

Assume DT_s period ends when V_{CE} returns to 400V.

Have to draw a piece-wise linear approximation to get the power curve.

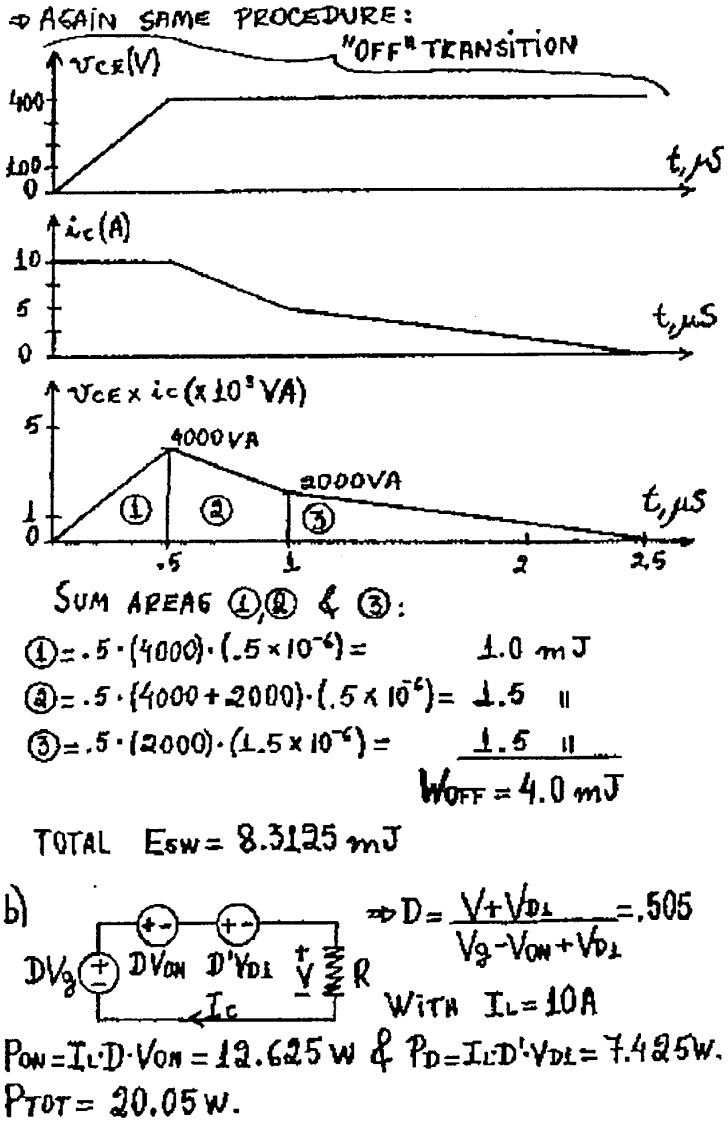
P_{ON}(sw. loss) = $W_{ON} * f_{sw}$

As f_{sw} ↑ so do dynamic losses

There are 4 time regions involved during IGBT <u>turn-on</u>. Each contributes a triangle of VA*time (energy) as shown above.

$\frac{1}{2}$ (VA) * $\Delta t = \mathcal{E}\Delta$

2. Turn off transition with current tailing



With a piece-wise linear approximation we divide IGBT current turn off into 3 regions

Power dissipated also has three regions contributing

$W_{on} + W_{off}$ = 8.3 mJ
Total switch loss
$P_{loss} = W_{sw} * f_{sw}$

b) For operation in a buck converter in steady state with V_{on}=2.5V for IGBT and V_{on}(diode)=1.5V find the DC switch losses.

We look at DC losses for the situation where V_D = 1.5V, V_{on} = 2.5V. But first we determine the D (transistor on time) and D (diode on time)

Volt-sec balance on L:

$-DV_g + DV_{on} + D'V_D + V = 0 \quad \Rightarrow \quad D = .505,\ D' = .495$

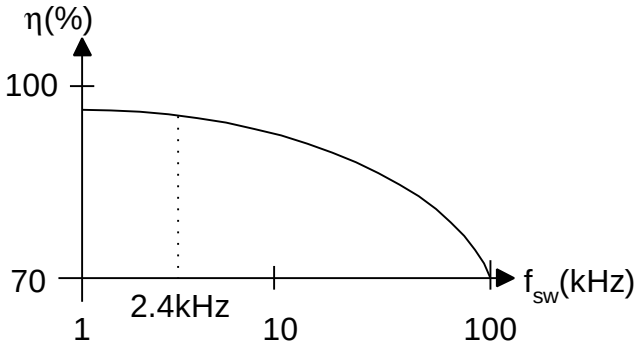
Then the two powers follow

Transistor: $P_{on} = (I_L = 10A)(.505)(V_{on} = 2.5) = 12.62$ W
Diode: $P_D = (I_L = 10A)(.495)(V_D = 1.5) = 7.42$ W

Next we get the buck converter total switching power loss versus switching frequency and see operating efficiency trends.

c) $P_{out} = 2000$ W = 10A * 200 V
but $P_{loss} = P_{DC} + f_{sw} * W_{sw}$

P_{DC} is fixed at 20.1 W



Consider the particular choice of switching when:

P(sw. loss) = P(dc loss)

This means a frequency given by:
$f_{crit} = P_{tot}/W_{sw} = 20.05/8.3125 = 2.412$
$f_{crit} \approx 2.4$ kHz which is far below a normal switching frequency, which is usually 50 - 500 kHz. Such a low frequency would mean large size L and C are required.

P_{AC}(loss) varies with f_{sw}

$W_{sw} = 0.083$ J

$P_{sw} = 0.083 * f_s$

@1KHz, $P_{sw} = 8.3$ W

@10 KHz, $P_{sw} = 83.0$ W

$\Rightarrow \eta = P_{out}/(P_{out} + P_{loss})$
$\Rightarrow \eta = 2000/(2000 + 20.1 + 0.083 f_s)$

Remember that in Erickson Chapter 4 you must do problems 2,4,5,and 6 as well as questions asked in the lecture notes for HW#4