Lecture 19
Real Semiconductor Switches and the Evolution of Power MOSFETS

A.. Real Switches: I(D) through the switch and V(D) across the switch

1. Two quadrant switch implementation and device choice example
   a. Current Bi-directional and one quadrant stand-off voltage switch case

B. MOSFET Evolution

1. Lateral MOSFET of Low Power VLSI Utility and Power MOSFET Curves
2. MOSFET Capacitance's
3. Vertical MOSFET For Achieving Both High Current and High Stand-off Voltages

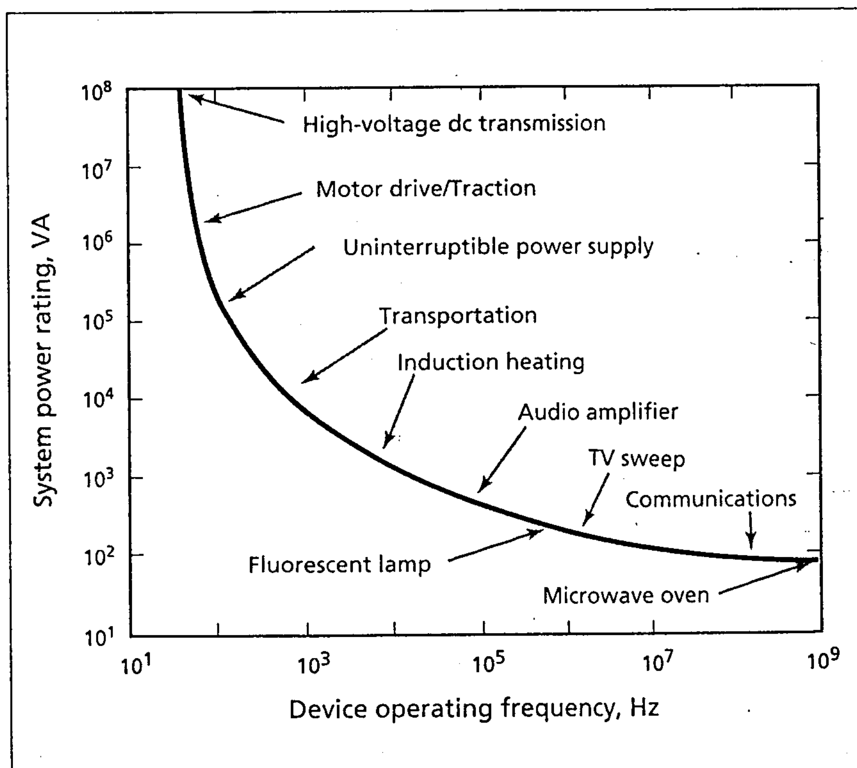
A.. Real Switches: I(D) through the switch and V(D) across the switch

We calculate from the circuit topology and switch positions the voltage across the switch, V(D), and the current through the switch, I(D), so that the required quadrants of switch operation are known. Then we look at various switch combinations to choose the best switch for the required needs at all duty cycles, D.

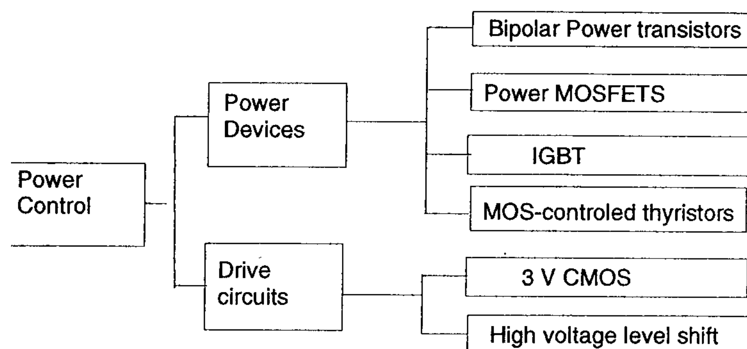
1. Two quadrant real switches

From our I(D) and V(D) analysis of the specific PWM converter there will be some switches that are required handle ± i but only one voltage. There are also switches that must handle ± V but only one current. We can construct the required switch from several established switches or we can use a new switch that has all the properties of the combination of older switches. For example, we will see that a bipolar transistor and a diode can replace a MOSFET and so on. The decision of what switch implementation to use is a tradeoff. We must consider:

- System power versus required operating frequency as shown on the next page
- Both the power device choice and the associated power device driver requirements as shown on page 3
- The available switches and power ratings available at the time of design as shown on page 4
- The devices you have available to you at the cost limits set by the product profitability



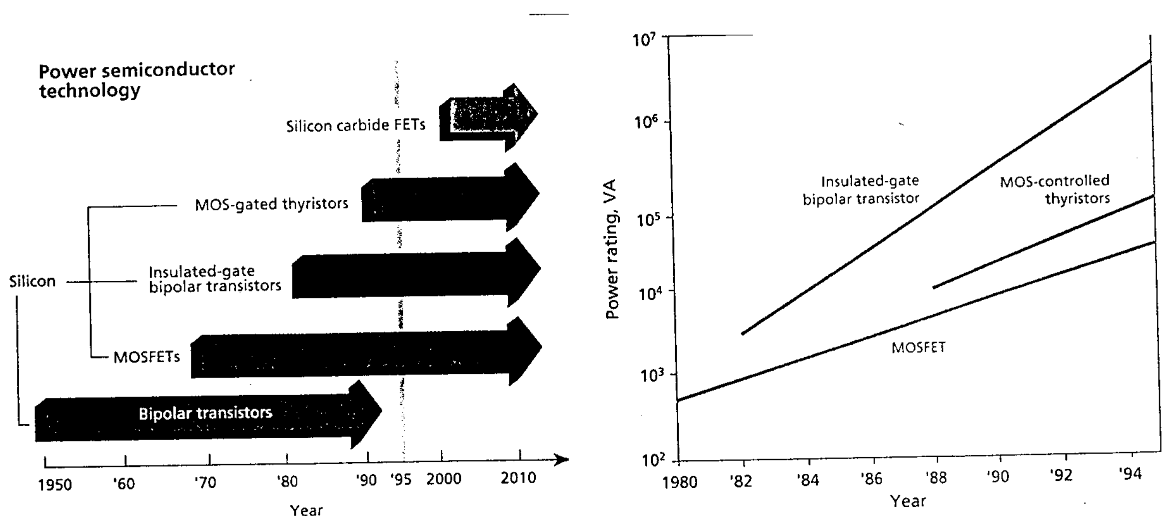
▲ Because of component limitations, the higher a system's operating frequency, the lower its operating power level. Power electronics systems for microwave ovens, for example, operate at about 1 GHz and have a rating of under 200 VA.



Note the curious hyperbolic power versus frequency relationship in application requirements for power electronic switches. We must also realize that at high power levels the switch drive required may be 1-10 % of the power switched. At the MW level the switch driver is itself a high power device.

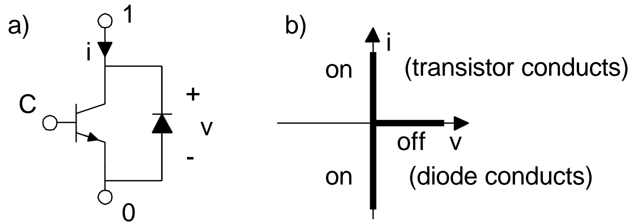
We look below at the time evolution of some possible power devices that we could employ as switches and their power ratings for the case of IGBT, MOSFET and THYRISTORS. These curves are a function of time and also operating frequency, but they are a crude guide to the choices we will have to make. Each power device will require a specific drive circuit specially designed for that switch and no other. Thus as part of our decision on the switch choice we must also consider the associated drive circuits.

We will use circuit analysis to determine the required quadrants of operation for a given switch and the absolute values of the voltages across, V(D), and currents through, I(D), the switch as a function of duty cycle, D. Then the artistic choice of the precise switch and what it is made of, in terms of combinations of other switches, begins.



(a) Current bi-directional switch with only one standoff voltage

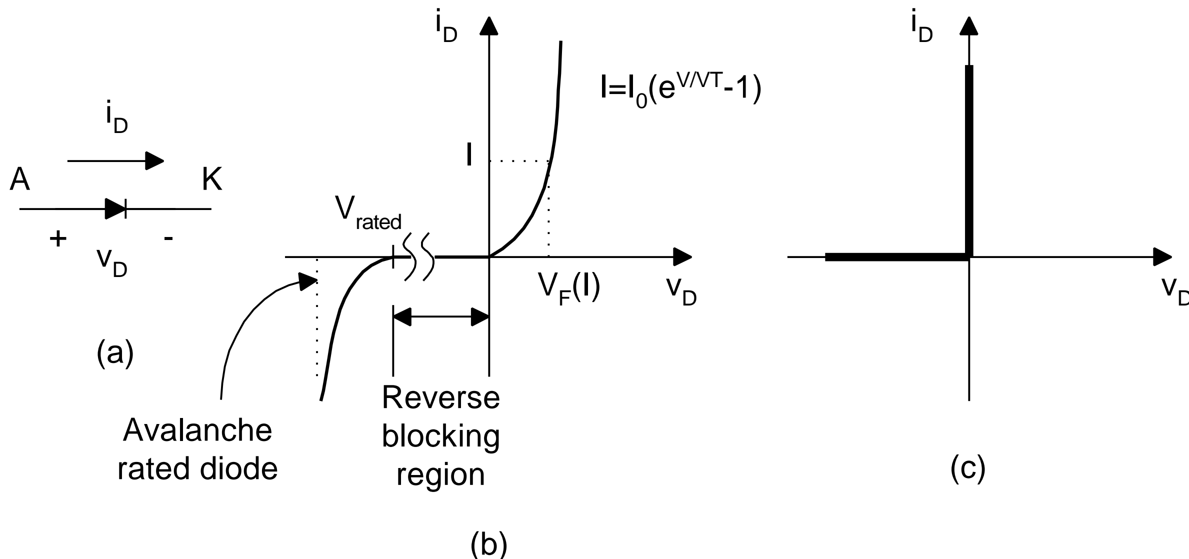
Consider first, a two device bi-directional switch made **solely of bipolar transistors and diodes.**



Current-bi-directional two-quadrant SPST switch: (a) implementation using a transistor and antiparallel diode. (b) idealized switch characteristics.

Note parallel diode around a bipolar transistor insures with v negative i flows to achieve a two quadrant current switch.

In lecture 22 we will look at bipolar diode and transistor characteristics in more detail when we cover thyristors but for now we just remind you of the of the I-V curves as shown below.



On the following page we place the bipolar transistor characteristics as well for your perusal and consideration.

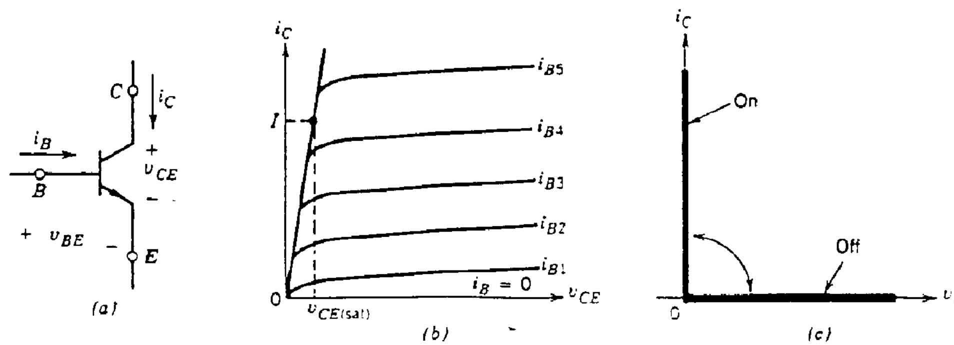
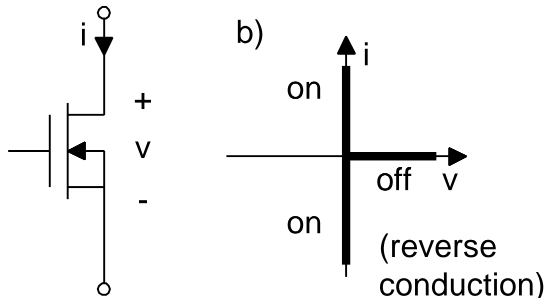


Figure 2-7 A BJT: (a) symbol. (b) i–v characteristics. (c) idealized characteristics.

For more details –see lecture 22. Here in lecture 19 we will short change BJT technology because MOS technology has replaced it so successfully. Consider that we are able to replace this two component, all bipolar, switch implementation with a single power MOSFET device. The single MOSFET device, we will see, has the operating characteristics shown below, thereby replacing two bipolar devices.

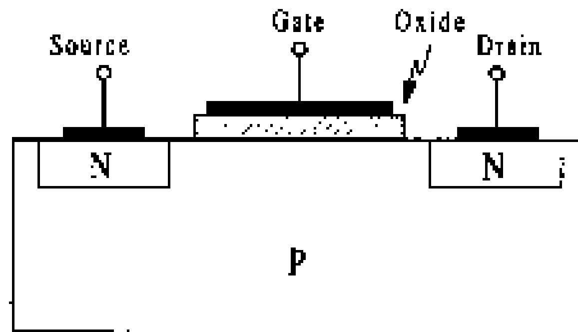


B. MOSFET Evolution

1. Lateral MOSFET of Low Power VLSI Utility

Consider the figure below for a low power VLSI type MOSFET and the inversion layer current channel under the lateral gate. This also shows, if the source is shorted to the body, the internal reverse p-n diode of a MOSFET. It also shows a big limitation. To scale to higher current we need a wider gate width and a smaller channel length. The latter is incompatible with high V_{DS} voltage. That is g_m ~ W/L, but small L means the MOSFET will not

withstand high blocking voltages. Moreover, large W means we take up a large amount of chip area and cannot get as large a cell packing density of paralleled MOSFET'S. What to do???



Power MOSFET cross-section in p-type substrate body.

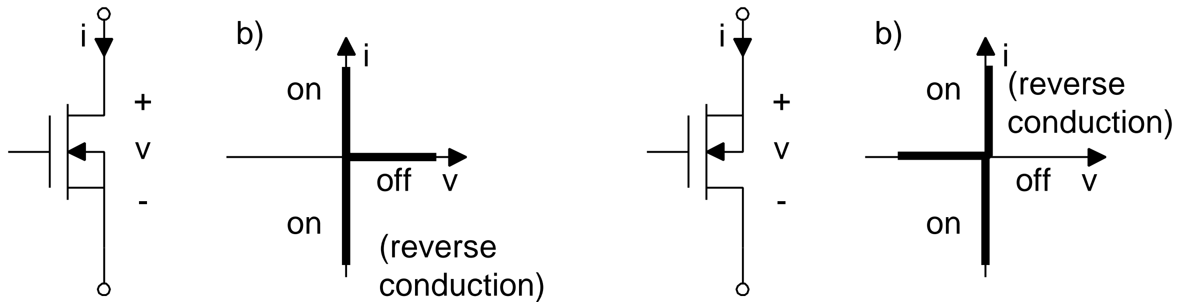
Parallel to the MOS channel there is a parasitic NPN bipolar transistor, with no circuit connection to the p-base. However, parasitic capacitive currents cause by high dv/dt in the off state. That is i = Cdv/dt, can create base current. To avoid this unintended parasitic bipolar action possibility the four terminal power n-channel MOSFET (gate, drain, source and body) has the body shorted to source to create a three terminal device. For p-channel MOSFETs the n-type body is connected to the p-type source. This short creates a p-n pair from source (via body) to drain called the reverse body diode. This diode allows for bi-directional current to flow with performance similar to the MOSFET.

Unique to MOSFET's is both the low R_{on} and the speed of switching because no bipolar storage time is present:

$10 \leq \Delta t_{sw} \leq 100$ nsec. Switching speeds can be fast compared to T_{sw}. Switching speed depends only on the gate current.

MOSFET's are voltage controlled devices.

N-channel CMOS transconducts $\pm$ i. This is explained as follows on page 8 below.



n-channel current flow is normal from source to drain. Source terminal is negative, drain is ground.

Blocks +V

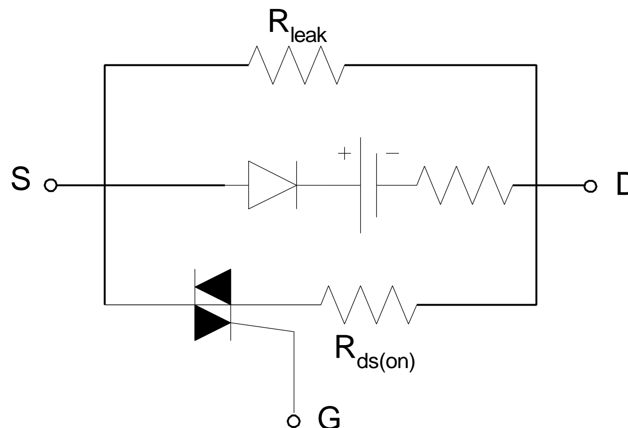
conducts +i downwards

MOSFET can operate backwards. n-channel current flow is opposite from drain to source if drain terminal is negative and source is ground.

FET blocks -V

conducts +i upwards

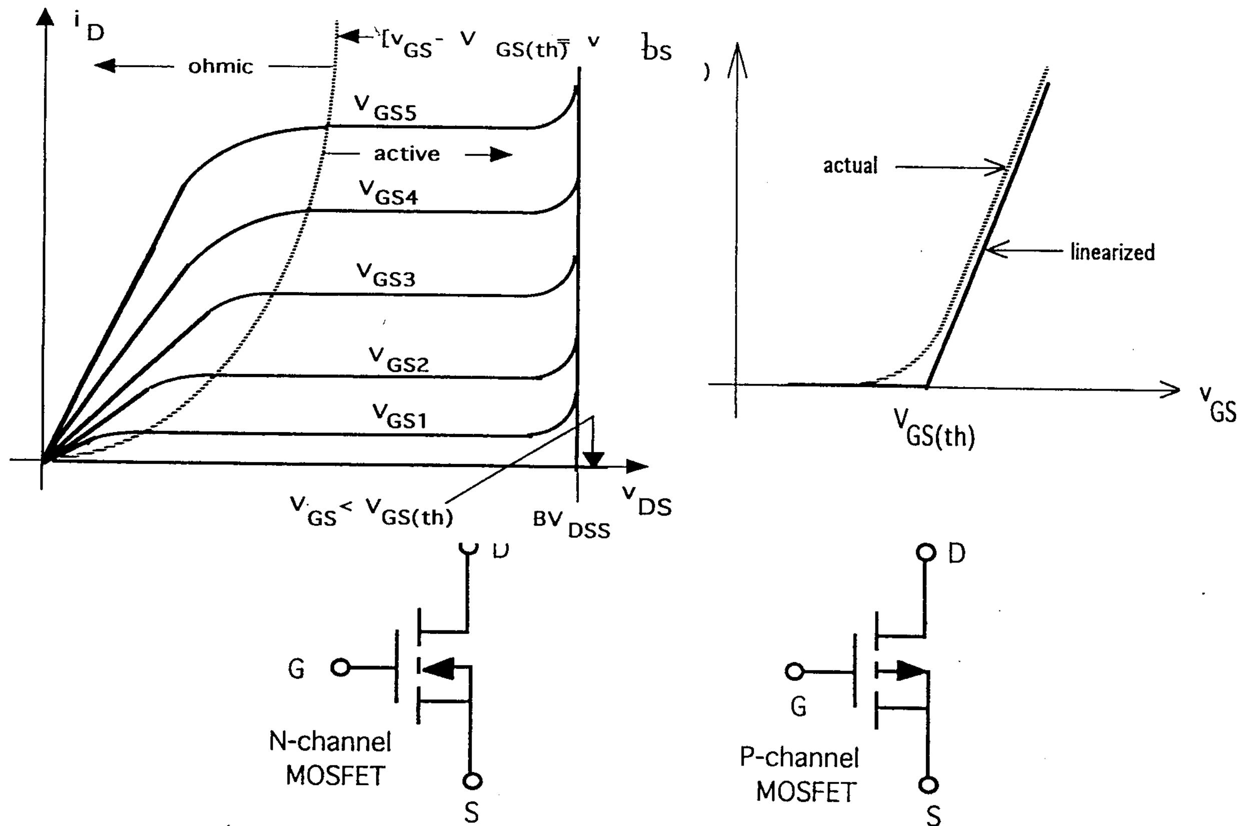
The static model for a VLSI MOSFET involves the following four values.



Static model for MOSFET. The leakage resistance R_{leak} is usually mΩ.

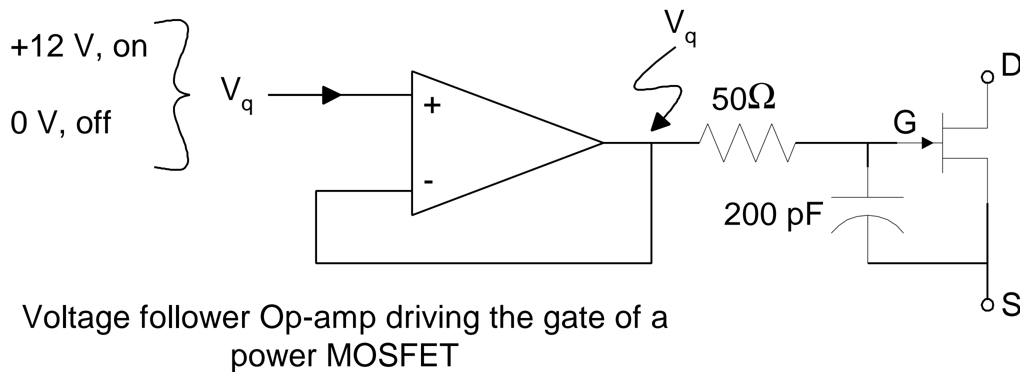
In comparison, a typical power MOSFET characteristic curve is shown schematically below on page 9 and an actual I-V curve on page 10. The I_{out} - V_{in} characteristic for $V_{in} > V_T$(threshold) is given by the transconductance g_m whose value for power MOSFET's is typically,1-10 Siemans.

MOSFET I-V Characteristics and Circuit Symbols



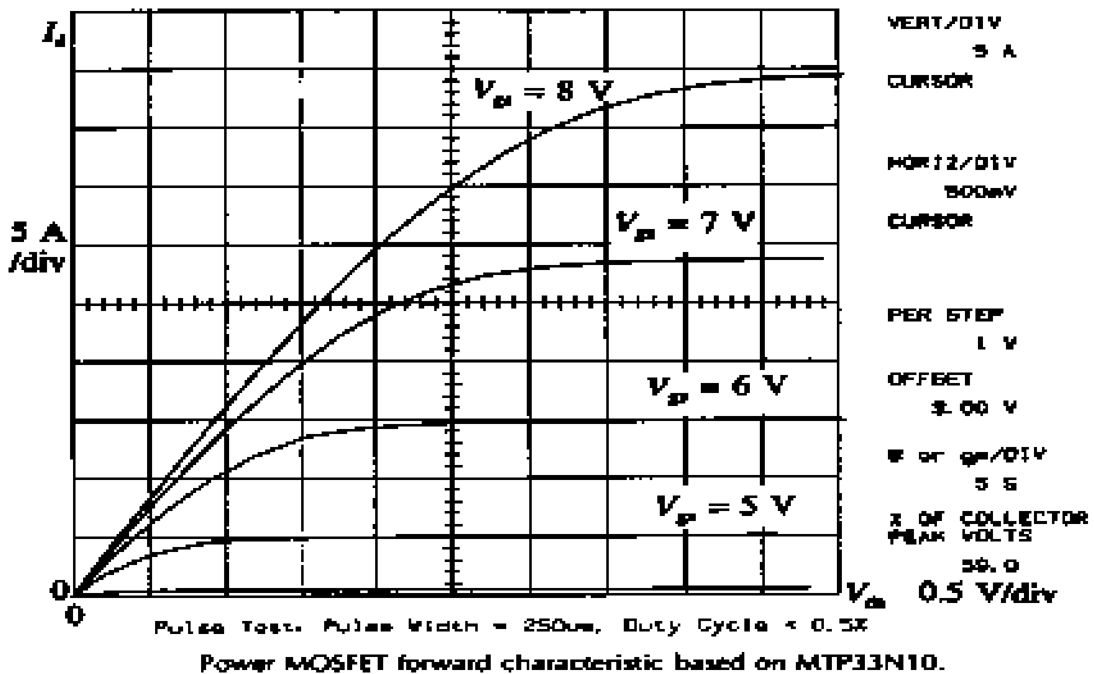
As seen, $V_{GS} > V_T$ (1-3V) the device turns on and I-V is linear up until saturation. For power MOSFET devices R_{on} reaches a minimum for $V_{GS} > 10V$ as compared to logic MOSFET's.

For switching control or driver circuits, conventional analog op-amps provide sufficient gate drive for the low to intermediate power switches. Special driver stages can supplement the op-amp. Fifty ohm Z_{out} for an op-amp gives RC of 100ns for the gate turn-on as shown on the following page.

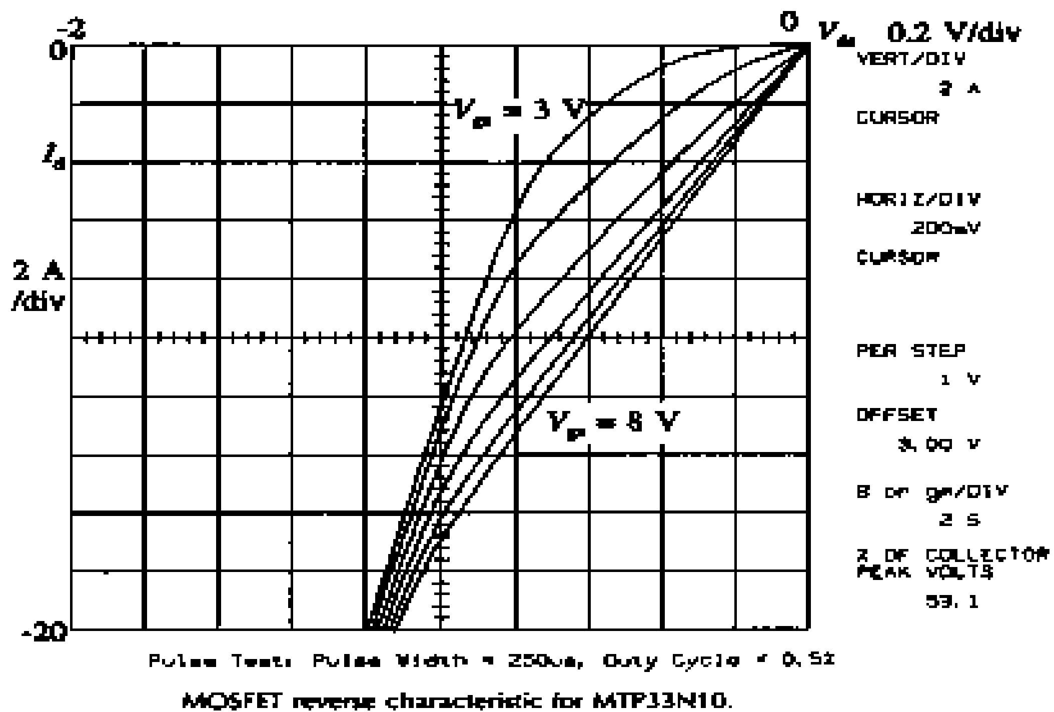


Voltage follower Op-amp driving the gate of a power MOSFET

The specifications of a typical low power MOSFET in forward mode are given below and on the next page in reverse mode. Data sheets for I_{DS} versus V_{DS} with V_{GS} as a parameter are shown directly below. From analysis of these curves we can extract the DC MOSFET parameters for the model of page 8.



Power MOSFET forward characteristic based on MTP33N10.

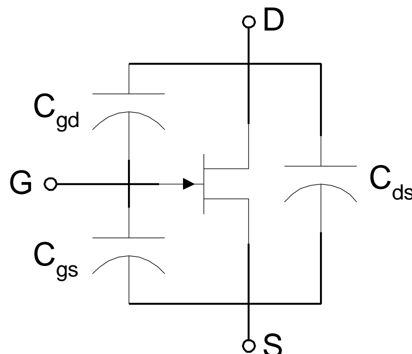


MOSFET reverse characteristic for MTP33N10.

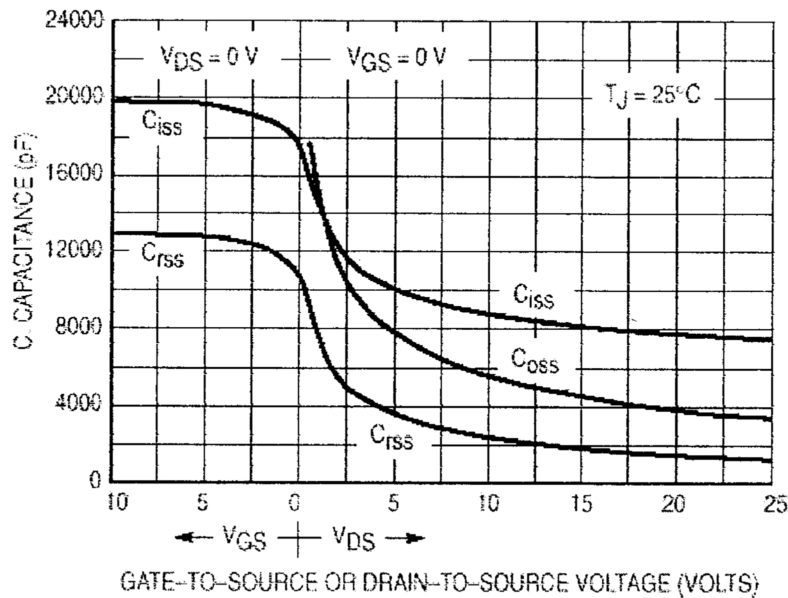
For **HW#4**
Estimate all values for the static model of the MOSFET shown on page 8 from the above data sheets.

2. MOSFET Capacitances

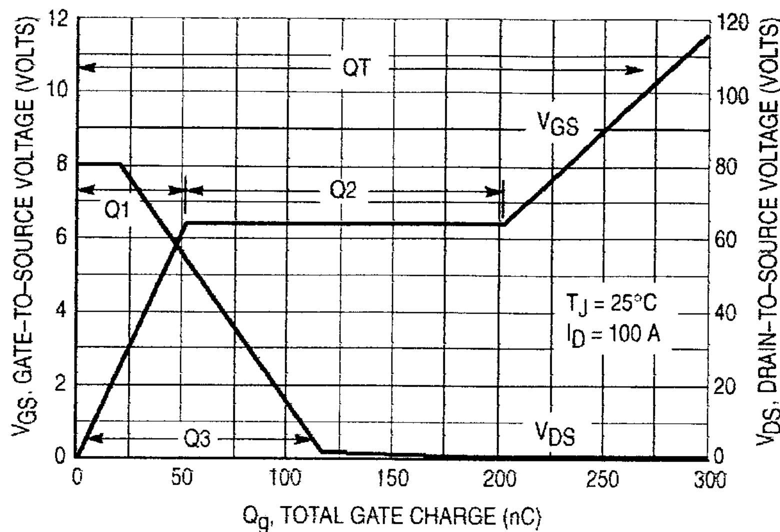
Shown below are the various device capacitance's for a MOSFET



Capacitance elements associated with MOSFET.



Note that for a charged gate the capacitance is nearly twice the value for an uncharged gate. This fact is very crucial to proper design of MOSFET gate drive circuits. That is, the turn-on delay for a given gate drive circuit has several regions in a plot of V_{GS} and V_{DS} versus total required gate charge as shown on the following page. We arbitrarily divide the total charge on the gate into three parts that we represent with the variable, Q , each is associated with a specific turn-on time. This level of detail is way beyond the intentions of this introductory course. Nevertheless, the issues are real and you should at least realize that power device turn-on has a variety of meanings as discussed on page 13 below. One way to discuss this is via changes in V_{GS} and V_{DS} versus the gate charge.



. Gate Charge versus Gate–to–Source Voltage

Q_1 is the gate charge to achieve a turn-on delay for a given gate drive current. Note the charge Q_1 for turn-on is smaller than Q_2 required for turn-off as described below

Q_2 is the gate charge to achieve a turn-on time delay if we consider the full Miller capacitance and associated charge. The gate capacitance is twice as large, if the MOSFET is turned on rather than turned off. Hence, twice as much charge, Q_2, is needed to turn-on when this effect is included as for turn-on when we do not take this into consideration. Roughly, speaking $Q_2 = 2 \times Q_1$

Q_3 is the value gate charge for turn-on and turn-off time including load effects. **It is only that part of the Miller charge essential to the SWITCH LOSS calculations**. Q_3 lies in-between the low Q_1 and high Q_2 values.
Q_{total} which equals (Q_1+ Q_2 + a little more charge) is the total charge to drive the MOSFET, not only on, but into the I-V region where the source-drain resistance is lowest.
We will revisit this later For MOSFET'S we find the crude rule

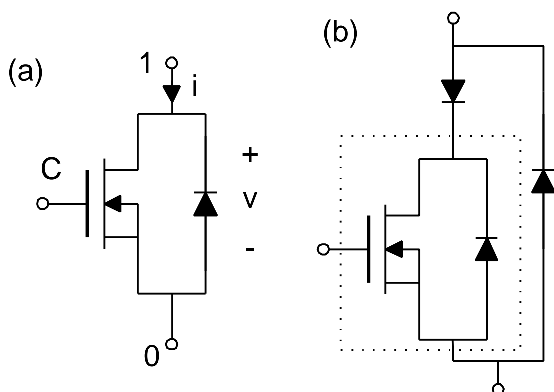
$C_{DS}(V_{ds}) : \frac{C_O}{\sqrt{V_{DS}}}$. Incidentally for MOS devices, C_{DS} is big when it should be and small when you don't need it. We will revisit this in lecture 21 where we will see that C_{DS} is an ideal snubber capacitor for inductive switching!

In summary, power MOSFET gate capacitance is typically 2000 - 8000 pF. These capacitances must be included in any realistic circuit model using the device.

3. Vertical MOSFET For High Current and High Stand-off Voltages

a. Low R_{ON} advantages and a circuit example

The old lateral MOSFET for low power VLSI doesn't scale well as we go to higher power levels. Neither the current through nor the voltage across a lateral MOSFET can hold a candle to the vertical MOSFET structure we will cover below. Moreover, vertical structures allow for more parallel devices per area and hence lower on-resistance. Nevertheless, some features will remain the same.

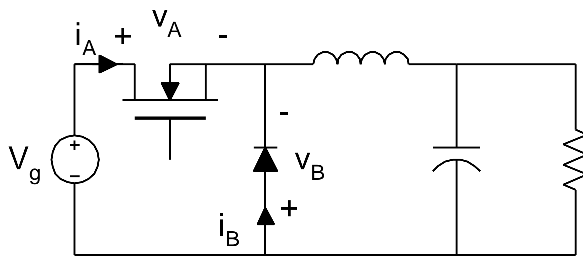


V positive the reverse body diode will NOT conduct but TR may or may not depending on control voltage. Bipolar conducts only 1 way naturally.

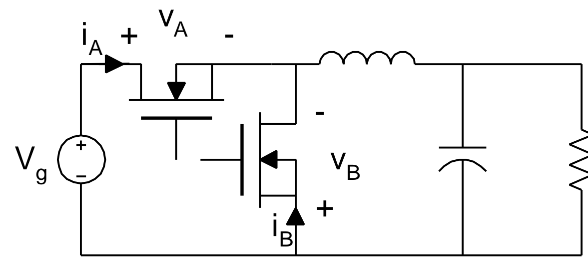
The power MOSFET inherently contains a built-in body diode: (a) equivalent circuit. (b) addition of two external diodes to prevent

conduction of body diode.

One result of the above discussion is that one may use a reverse connected FET to replace a diode in a PWM dc-dc converter provided we actively turn on and off the MOSFET when desired. In that case reverse current conduction is allowed and the CCM may prevail for all circuit conditions.



Implementation of the SPST switches using a transistor and diode.



Buck converter implemented using a synchronous rectifier by replacing the diode with a MOSFET.

In computer chip power supplies, this done for 1.5/3.0 V converter supplies because otherwise the diode loss is too big. That is we need a low R_{ON} device and the MOSFET is the ticket.

b. Evolution of the Vertical Structure MOSFET

1. Overview of Issues

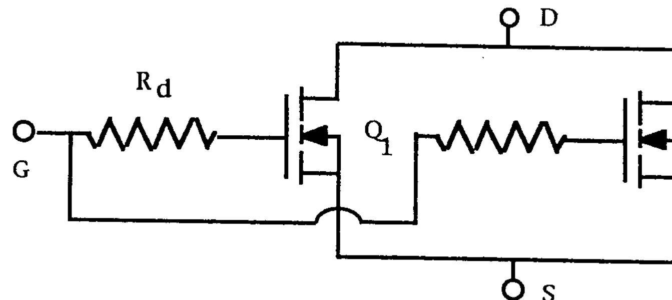
To get to the condition that the FET resistance causes much lower DC loss than, say a diode, we need to satisfy the relation below. To achieve this, we shall see that **vertical rather than lateral MOSFET structures can be sufficiently paralleled** in a given practical device area to reduce R_{ON}. In pages 15 –19 we will also outline the evolution of the vertical MOSFET from lateral DMOS to the present highest density UMOS that utilizes vertical trenches to **achieve the lowest possible R_{ON} yet still improve the stand-off voltage that the device can handle**.

$$I_{rms}^2 R_{ON}(FET) < I_{rms}^2 R_D(ON) + I_{rms} V_o$$

Don't ever forget a successful power MOSFET requires both high current through the device, low R_{ON} and a large voltage across it.

Below we first show that we could get a successful power MOSFET from just a big scaled up lateral MOSFET with **enormous gate width** to achieve high current drive at stand-off voltages up to 100 Volts but not beyond that. A big lateral transistor might drive big currents but it would never stand-off the large (>100 Volts) voltages that are also required to be blocked across the source-drain region of a practical power switch. We also give below a quick insight as to why we can indeed parallel MOSFETS as compared to bipolar transistors, which we cannot easily parallel. Without this knowledge it would be foolhardy to even invest the energy in trying.

- MOSFETs can be easily paralleled because of positive temperature coefficient of $r_{DS(on)}$.

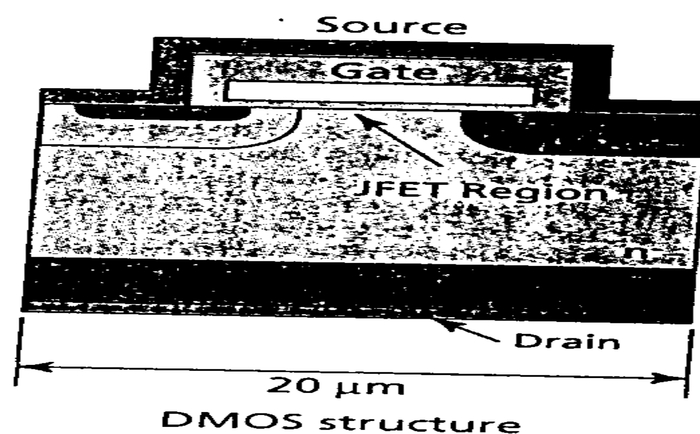


- Positive temperature coefficient leads to thermal stabilization effect.
  - If $r_{DS(on)1} > r_{DS(on)2}$ then more current and thus higher power dissipation in Q_2.
  - Temperature of Q_2 thus increases more than temperature of Q_1 and $r_{DS(on)}$ values become equalized.

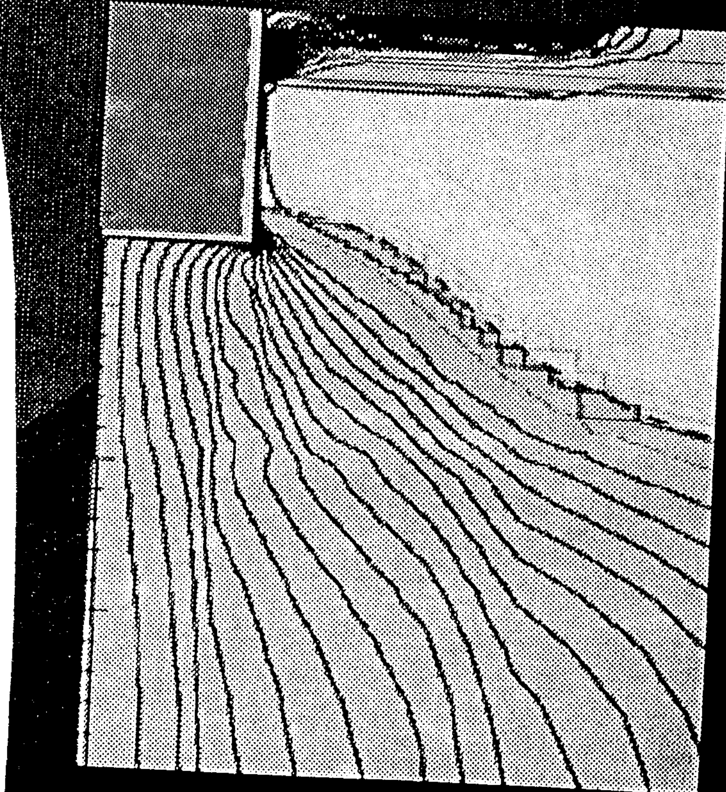
The above two factoids, will act as motivation and guide for the next five pages of text that culminate in the method and structures to achieve millions of paralleled MOSFETS by employing vertical rather than lateral MOSFET designs. On the next page we tell why the old but big lateral MOSFET is inadequate for the task but the vertical MOSFET, in contrast, is ideal.

2. Vertical MOSFET Structure

Shown below is the revolutionary vertical MOSFET structure. To achieve a large distance between the source and drain and yet utilize minimum area on a silicon wafer we place the drain on the bottom of the wafer and the source on the top. In between we employ low resistivity material which can more easily withstand the required stand-off voltages, as there is lots of room for large depletion regions from back biased junctions. The figure below depicts the off-state with no current flow from source to drain. The difficulty in DMOS is that the current flow is not confined in any way so that if we wish to place nearby other MOSFET'S, to achieve an array of parallel devices,we will have overlapping current flows. This current flow overlap situation spoils any attempt to achieve independent MOSFET action for parallel devices.



DMOS structure



Notice that in the vertical MOSFET as compared to the lateral MOSFET the **current flows vertically** from source to drain and vice versa depending on whether or not it is a p or n type MOSFET. What is shown above is the role of the deep trench and associated vertical inversion channel to cause the current flow to be spatially confined. The source and gate regions of the vertical MOSFET, on the top of the wafer, can still be patterned using conventional lithography to very small dimensions allowing many MOSFET'S per unit area of silicon. But vertical current flow through the bulk silicon, if it is not well spatially confined, limits the closeness of neighboring MOSFET'S that we wish to parallel.

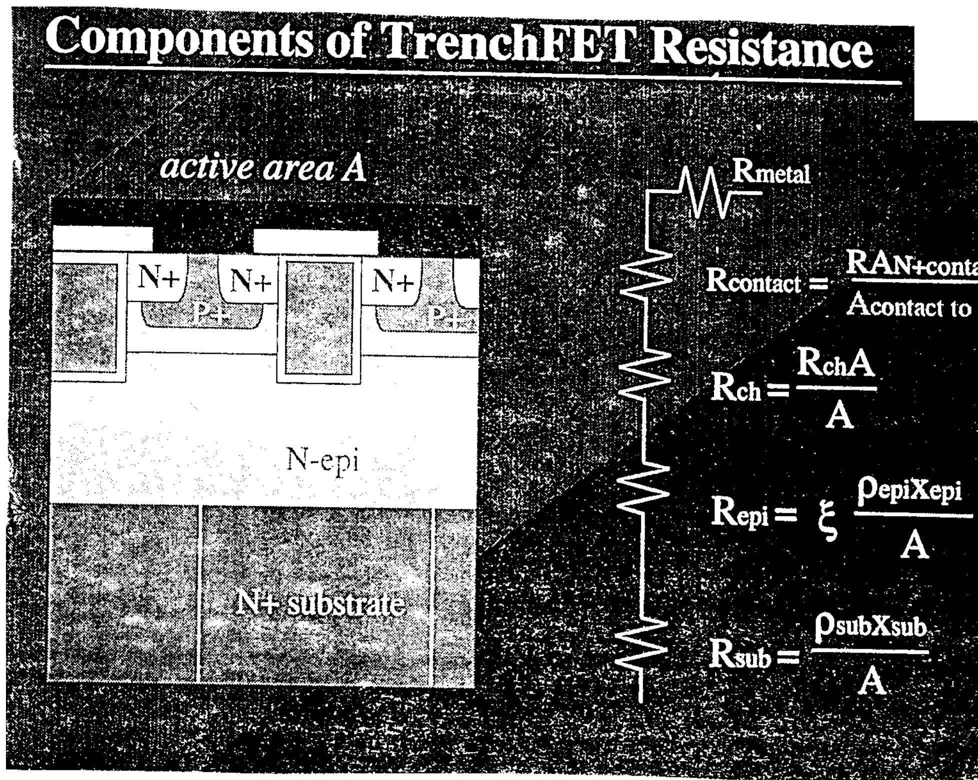
This unacceptable situation was solved by employing a buried trench that had both a conducting gate inside the trench and thin gate oxide sidewalls capable of creating a vertical inversion layer in the silicon next to the trench. The trench of “U” shape would be dug deep into the silicon so that vertical current flow in the two inversion channels would initially be guided along the sidewalls in a confined manner from the top downwards. The term UMOS is given to this structure which is shown on page 18.

At the top of the vertical MOSFET the source and gate regions would still be defined by lateral lithography so ultra-small device sizes could be manufactured next to each other to achieve very high device densities per unit area. Here the vertical current flow easily spreads out laterally because there is no current confining structure. Moreover, the resistivity of the lightly doped JFET region causes unacceptably high R_{ON}.

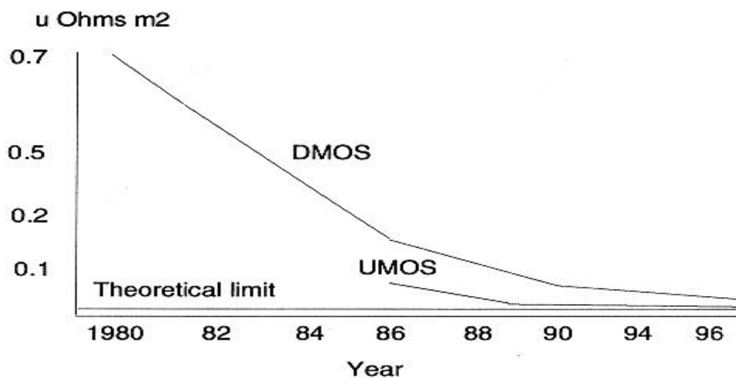
Compare the current flow with a vertical trench structure shown above. The vertical trench with associated inversion layers provides four beneficial effects.

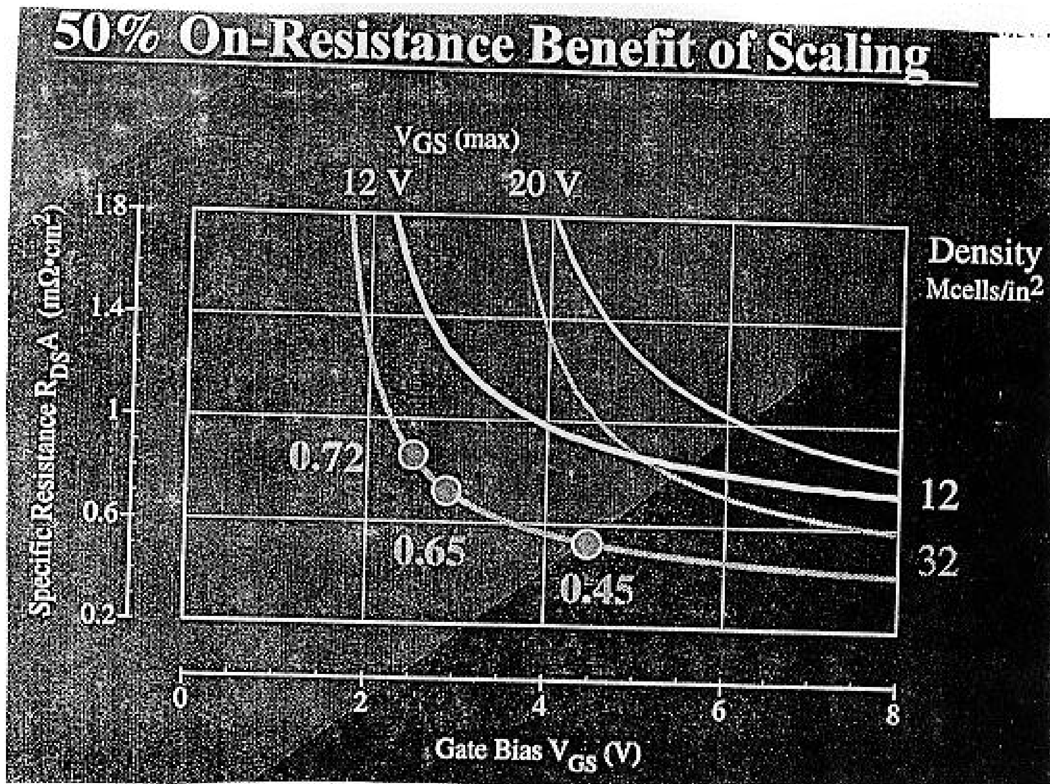
- Lower R_{ON} than the bulk silicon in the epi layer
- Much more confinement of the lateral current spread as well as improved uniformity of current density
- A higher packing density via tighter cell pitch of paralleled devices. The benefit of high-density is greatest at lower drain voltages
- Vertical current flow prevents snapback breakdown in MOSFET as well as in IGBT’s of lecture 20

To better visualize the vertical current path and associated spatially resolved contributions to total resistance we show the components of a single MOSFET resistance below on page 20.



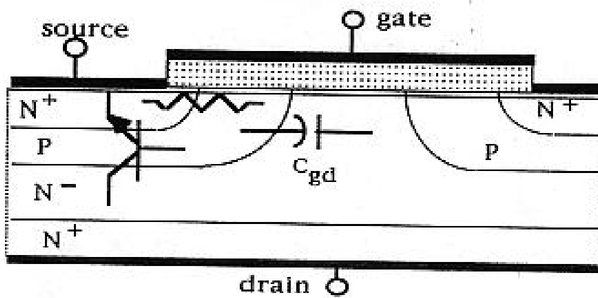
Clearly, with the trench, of variable depth and width, it is now easier to optimize both the stand-off voltage and the on resistance of a power MOSFET. Moreover, we are now able to pack millions of cells into a given area. If each cell carries one milliamp, with a million cells, we are able by paralleling to achieve KA levels of switch current. This situation is summarized on two graphs on page 21.Hence, UMOS reaches the theoretical limit of on resistance as shown below and on page 21.

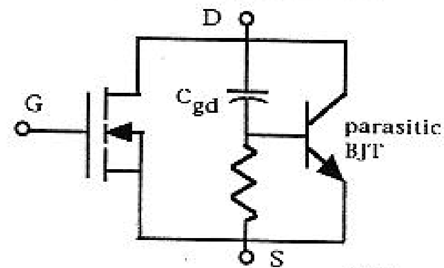




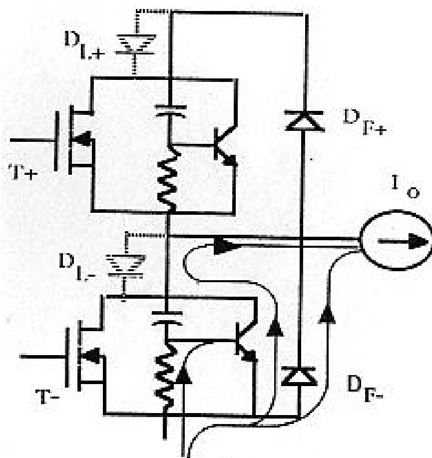
On the next page we look at the device cross-section for the vertical MOSFET and realize that there are more devices there than we designed for. In particular, we note the parasitic vertical BJT. This device is usually just a non-involved one in most forms of switch action. But, for positive dV_{DS}/dt conditions experienced during MOSFET turn-off, we note we we cause a parasitic BJT to turn-on inadvertently. $C_{GD} x\ dV_{DS}/dt$ drives the BJT into conduction. This situation is shown on the next page in more detail. The vertical parasitic BJT is outlined and the parasitic current path as well. The full MOS device model is also shown with the BJT. THIS IS A CAUTIONARY WARNING on the proper use of MOSFET's and is easily avoided by snubber circuits placed around the MOSFET to avoid too large dV/dt conditions described in lecture 21.

dV/dt Limits to Prevent Parasitic BJT Turn-on





- Large positive $C_{gd}\frac{dV_{DS}}{dt}$ could turn on parasitic BJT.



- Turn-on of T_+ and reverse recovery of D_{f-} will produce large positive $C_{gd}\frac{dv_{DS}}{dt}$ in bridge circuit.
- Parasitic BJT in T_- likely to have been in reverse active mode when D_{f-} was carrying current. Thus stored charge already in base which will increase likeyhood of BJT turn-on when positive $C_{gd}\frac{dv_{DS}}{dt}$ is generated.

Again, the way around this situation is to employ a snubber circuit to limit the dV/dt values placed across the MOSFET. The device capacitance itself will act as as first order snubber to limit dV/dt. We will cover this in detail in lecture 21