LECTURE 18
Switches and Switch Stress: The Concept of Safe Operating Area for a Device

I. Ideal Switch Characteristics
  A. Block $\pm$V with $I_{OFF} \equiv 0$
  B. Pass $\pm$I with $V_{ON} \equiv 0$
  C. Zero switching delay and its benefits
  D. Power loss due to switches: zero in every way
      1. DC Loss: $R_{ON} = 0$, $V_{ON} = 0$
      2. Switching Loss: No delays, no device stored charge
  E. No stray L_p or C_p for undesired ringing!

  F. Real Switches
      1. Limited quadrants of operation for real solid state switches
          a. One quadrant and device example

II. Active Switch Stress (S) and Switch Utilization (U)

  A. General Definitions

$$S(\text{active}) \sim V(\overset{sw}{\underset{\text{off}}{}}) \; \text{Irms}(\overset{sw}{\underset{\text{on}}{}}) \; \text{per switch}$$

$$U \equiv \frac{P(\text{load})}{S} \; \text{per switch}$$
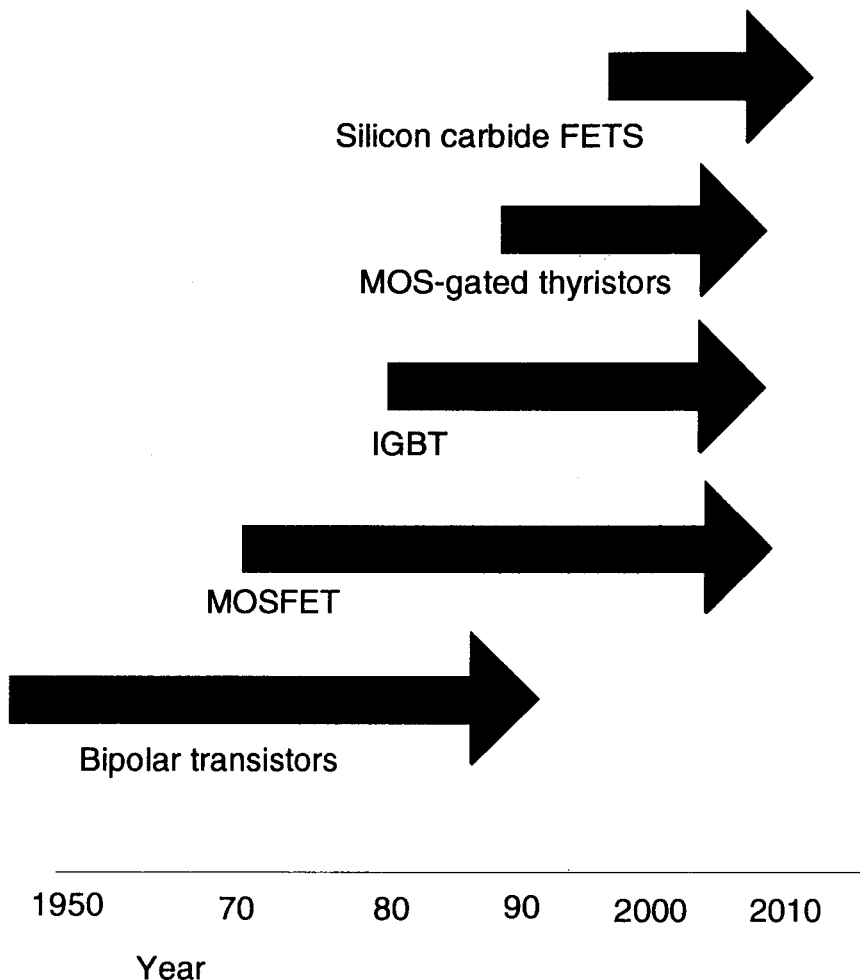
  B. Case of Flyback Converter

$$V(off) \sim V_g/D' \quad \} \; D_{opt}$$
$$\} \; for$$
$$I(on) \sim I \; \sqrt{D} \quad \} \; U_{max}$$

C. Table of U_{max} and D_{opt} for various Converters

Power Semiconductor technology map

Silicon carbide FETS

MOS-gated thyristors

IGBT

MOSFET

Bipolar transistors

| 1950 | 70 | 80 | 90 | 2000 | 2010 |

Year

The above selection of solid state switches will be matched to the I(D) through the device and the V(D) across the device as determined by detailed circuit analysis in the next few lectures. Analysis of V(D) and I(D) will follow the same procedure as M(D).

LECTURE 18
Switches and Switch Stress: The Concept of Safe Operating Area for a Device

A. Ideal Switch Characteristics:

There are five characteristics of a SPST <u>ideal</u> switch. You make think of a semiconductor power switch as you do of a light switch at home. It operates with no concern for losses in either the on or the off state.


+/-V
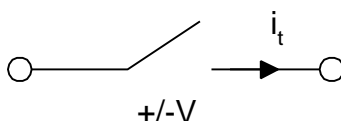
1. Block $\pm$V with $i_t = 0$: <u>No</u> leakage current flows when off

2. $V_{sw}(ON) \equiv 0$ at all i_t, either $\pm$i flow allowed

3. Switch on/off or off/on transitions occur with zero delay or instantaneous response time. Therefore, even for finite V and I during the switching, the energy E = (VI)(Δt) required to switch is near zero because the switch time is assumed to be zero. Removing this assumption is the first step to understanding real switches that operate at f_{SW}. Even if the switch transitions lose only a little energy and with a fast switch time, they switch at 100kHz to 1 MHz so that over one second close to a million transitions occur, each adding to the total lost energy.

4. Power required to drive the switch is negligible. No DC

losses nor any dynamic switching loss. Typically, a switch driver controls 100-1000 times the power it dissipates. However, for some devices this drive power can approach 10 % of the energy switched as we will see.

     5.   No device capacitance is charged or discharged during V_{OFF} or V_{ON} states. No charge Q is stored in semiconductor devices. No inductor current i storage occurs during the on state due to either real inductors or due to leakage inductance's of cores or due to wiring. Hence no additional stored energy flows to stress the switch via either I_{max} and V_{max}. Removing this assumption is the another big step to truly understanding switch losses

In summary an ideal switch is able to pass currents bi-directionally or to block voltages bi-directionally.

Note that SPDT switches may be modeled by two synchronized or commutated SPST switches. One is on while two is off and vice versa.
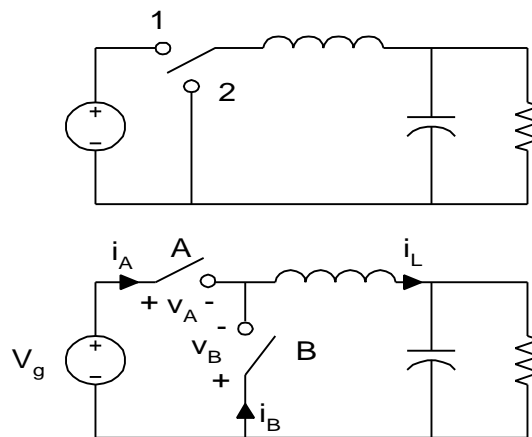
The ideal switch model now needs to be deconstructed assumption by assumption to better appreciate switch losses, which account for 5-15 % of total loss depending on the specific conditions of the PWM converter involved.
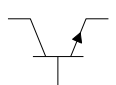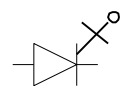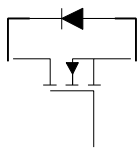
B.   Real Switches

There are five types of real switches we will predominantly deal with in power electronics, diodes, bipolar junction transistors(BJT), gate turn-off thyristors(GTO), field effect transistors(FET), and insulated gate bipolar transistors(IGBT), each of which has unique V-I characteristics shown below.

Five types of Real Switches

Switch Property

1. Passes current in one direction, blocks in the other	1. Diode
2. Passes or blocks current in one direction	2. BJT
3. Can pass in one direction or block in both directions	3. GTO
4. Can pass in both directions, but blocks in only one direction	4. FET
5. Passes or blocks current in one direction	5. IGBT

Device
Symbol

1. Diode

2. BJT

3. GTO

4. FET   (including body diode)

5. IGBT

We need to realize that each switch has unique and limited turn-on and turn-off characteristics. Hence, depending on what is required in terms of current passing through the device when it is on and voltage that the device is required to block when it is off, we may have only one choice for a switch regardless of cost. Of course some circuit circumstances allow for us to choose from several switch possibilities, perhaps introducing cost as a final

determining factor. Below we examine the diode and transistor switches briefly in a four quadrant V-I space to introduce the concept of **safe operating area** (SOA) for the specific switch . This is a rule of thumb that is easy to define and provided by each switch manufacturer to guide the user. For any real semiconductor switch as opposed to mechanical switches multi-quadrant operation is never easy unless we employ series and parallel combinations of our five main switches.
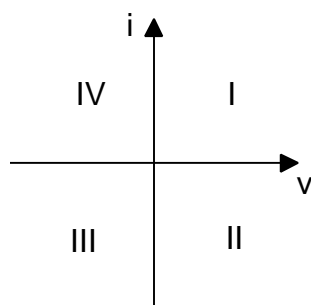
Four quadrant operation is not possible in single device solid state switches. To achieve four quadrants one needs several devices in various series/parallel combinations
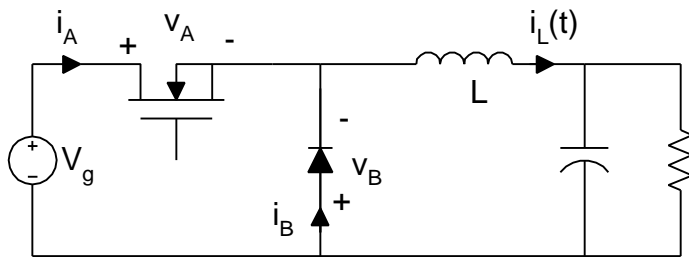
a.   One quadrant switches
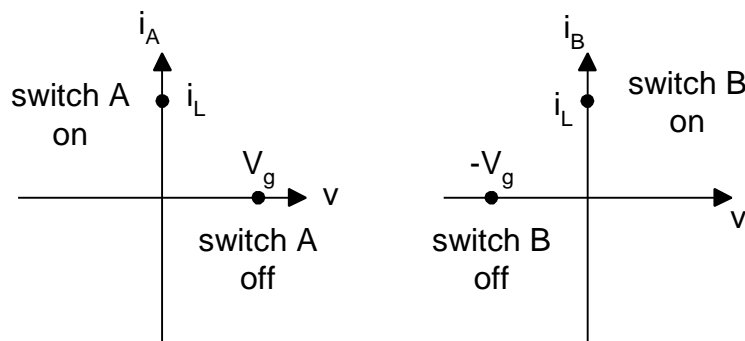
SW A is? Pnp bipolar? MOSFET?

SW B is? Diode, other?

Note the difference between bipolar transistors (only one-way current flow) and MOSFETs, (bi-directional current flow). Also, the bipolar of a different type can indeed stand off the opposite polarity but current flow is one-way, the other way. The key to consider in one quadrant switches is the V_{max}(off) and I_{max}(on) levels the switches are subjected to by circuit conditions.

To help thinking, consider the specific example of both switches above in a buck converter.
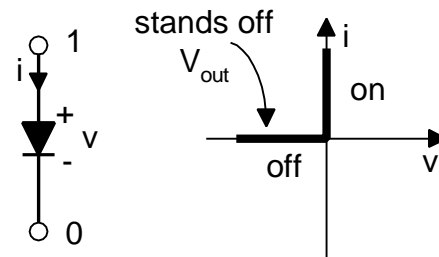
Several simple one quadrant switches are as shown below for both switches

SW A

SW B
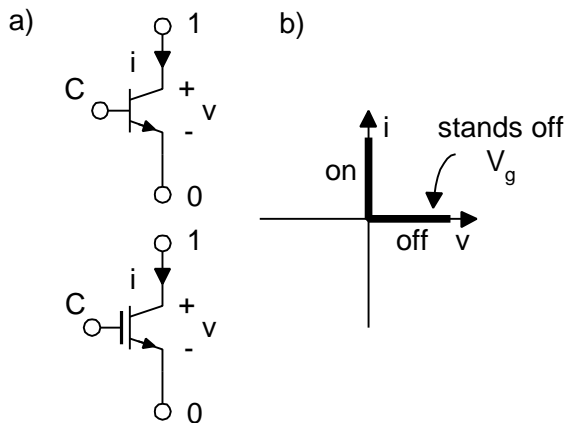
BJT and IGBT symbols (a), and their idealized switch characteristics (b).
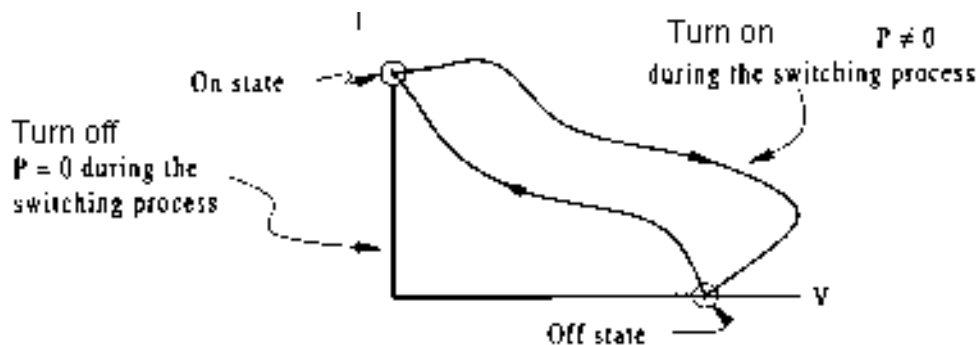
Diode symbol and its ideal characteristics.

The dynamic behavior during switching from a static off/on state to the other static state depends both on the switch device and the circuit. In the figure below we show three curves:
   1. Perfect Switch trajectories
   2. Typical turn-on V-I trajectory
   3. Typical turn-off V-I trajectory

Switch current vs. voltage, showing the switching trajectories.

The safe operating area as obtained from the manufacturers device specifications must lie well outside switching trajectories as shown below:
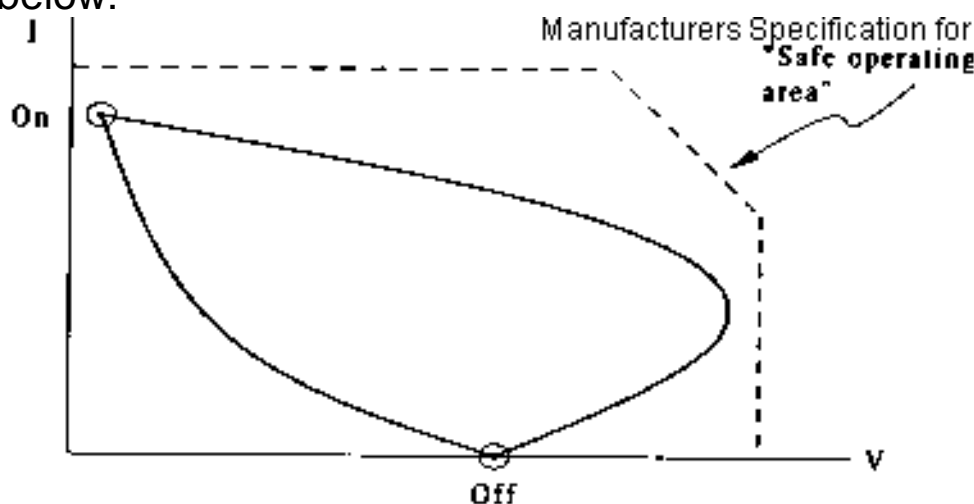

Switching trajectories within safe operating area.

Switch manufacturers also provide estimated device switching times based on operating conditions to better estimate the energy lost during switching $W = \int V*I \, dt$.

First lets refresh our memory on bipolar diode and transistor DC characteristics as well as some dynamic issues for these two one quadrant switches. Hopefully, this is a review for most students. If not we will cover these devices again when we focus in on the power electronic versions of these classic devices. All bets are off that these power electronic versions even vaguely resemble the microelectronic versions, especially for FET's
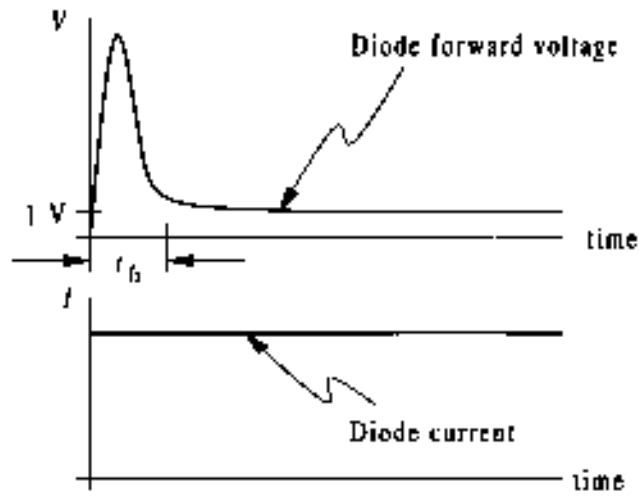
Static models of diodes involve the following:
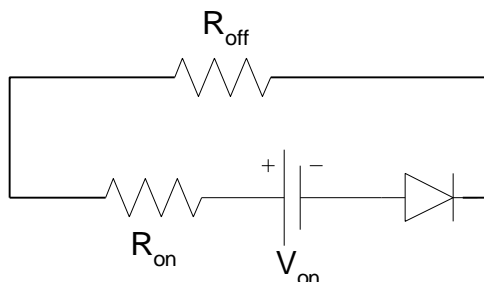
For HW #4 from the MUR3040PT diode data book for practice obtain all three values: R_{on} = 0.015, R_{off} = 40 mΩ, and V_{on} = 0.94 V.

Forward current vs. forward voltage for MUR3040PT fast diode.
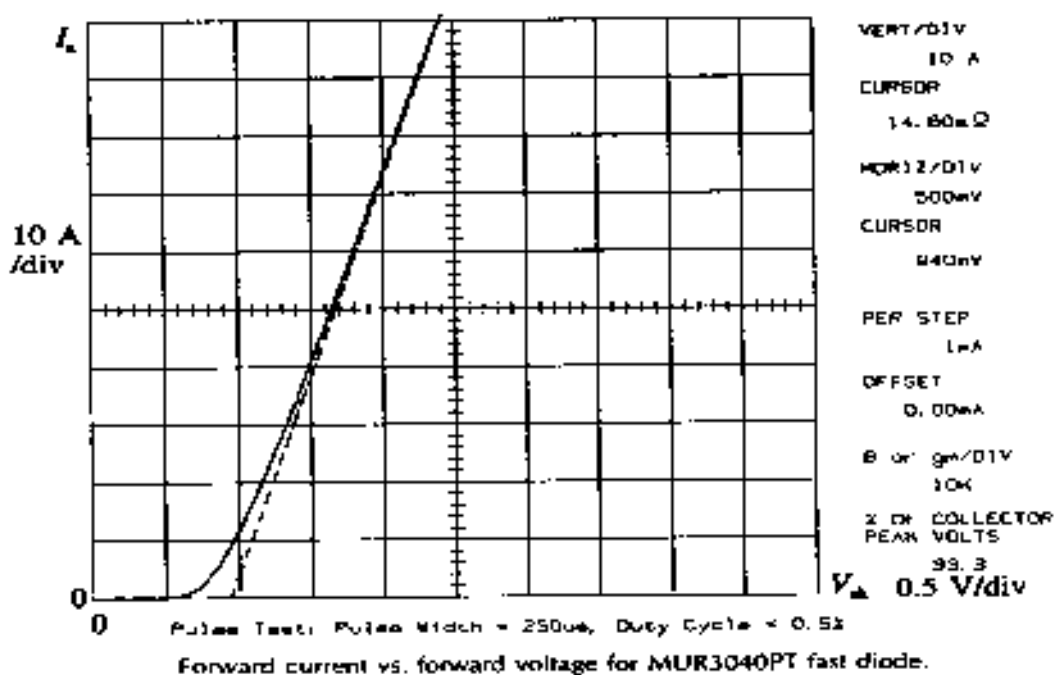
Static characteristics do not tell the full story of any device. Like people the dynamic characteristics may reveal new and unexpected behavior. For example, the V_{on} for the diode above does have a brief voltage overshoot when driven by a constant current source to turn it on. This needs to be accounted for in any dynamic model of diode operation as the dynamic I-V is unique.
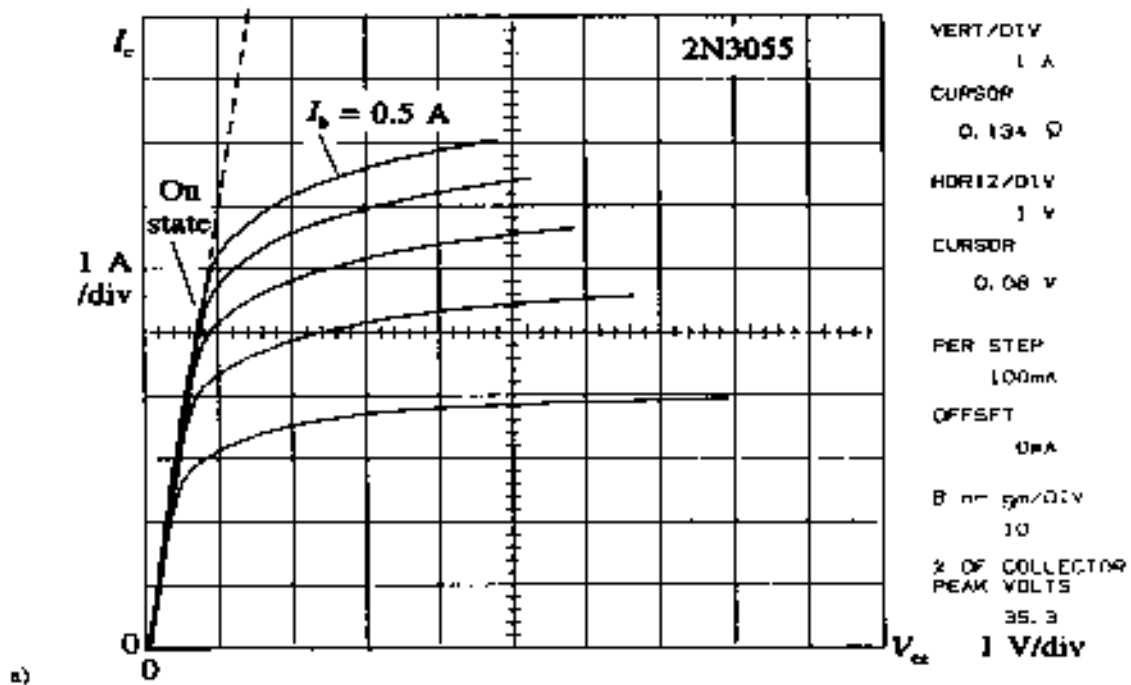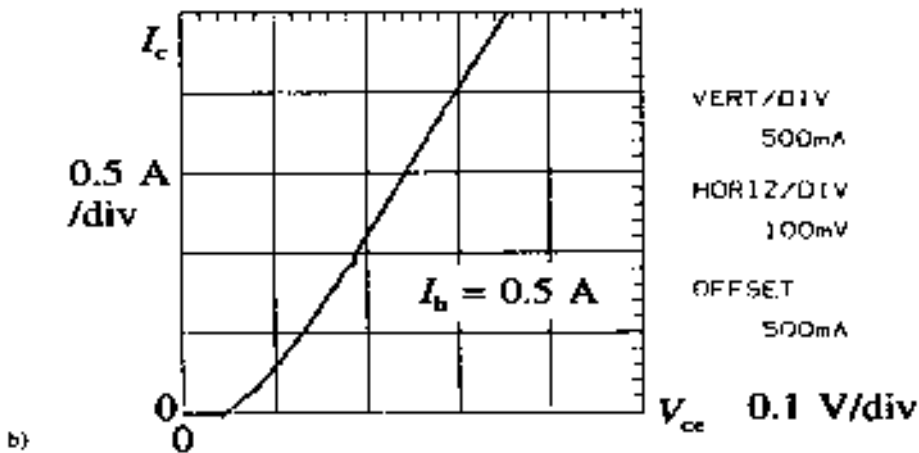
Forward recovery characteristic of a diode.

A static npn bipolar transistor model should involve the following two values:

R_{on} V_{on}
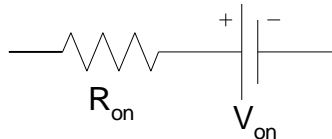
For HW #4 from the measured transistor characteristics below for practice obtain: $R_{on} = 134$ mΩ and $V_{on} = 0.08$ V.

Forward characteristic of power BJT. a) Forward characteristic; b) Expanded left portion.

The discussion of the thyristor, the gate turn-off thyristor and the insulated gate bipolar transistor will have to await a more full description of these unique switches. This will occur in later lectures.

II.　Active/Switch Stress and the Concept of Switch Utilization

We will below introduce quantatation to the concept of switch stress via a term, **S**, and also introduce an engineering term, **U**, to describe how well we are utilizing the chosen switch capability to the circuit need of that switch. The former can be compared to the SOA given by the switch manufacturer to avoid switch failure and the later can be used as a guide to answer the question of whether or not we are fully utilizing a chosen switch in the specific circuit to better access the costs on the bill of lading. What complicates the matter is that S and U depend on the duty cycle range employed causing tradeoffs to be made in any PWM converter design between the power switches and the controller conditions allowed.

A.　General: S(active) only

The cost of many PWM converters is primarily the expensive solid state <u>actively driven </u>switches as well as the passive diode switches. For a circuit of K such switches

$$S = \frac{\text{total switch}}{\text{stress}} \equiv \sum_k V(\overset{\text{peak}}{\text{blocking}}) I(\overset{\text{on}}{\text{rms}})$$

This sum, S, depends both on V blocking levels and current on levels as well as topology of the circuit and use of isolation transformers with known turns ratios. Ringing due to leakage inductance's only adds to peak voltage stress.

We want to minimize this stress yet still have maximum power flow! And we want to use the cheapest switch possible to make more profit on the PWM converter.

Utilization $\equiv \dfrac{P(\text{load})}{S(\text{active})}$ We want to maximize

U although typically it is a value <1 depending on the operating point, using transformers.

B.   Case of Flyback Converter with <u>one</u> transistor

(a)   Find peak blocking voltage
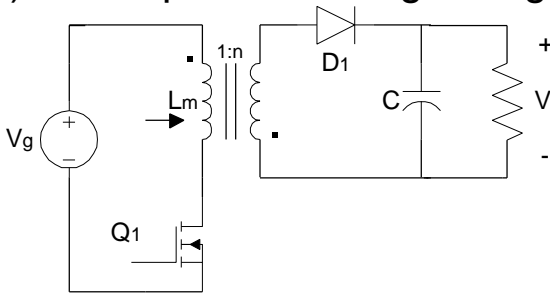
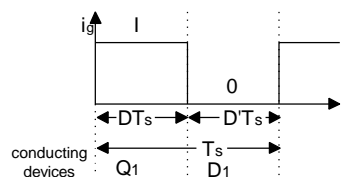(a) $V_{tr}(\overset{\text{stand}}{\text{off}}) = V_g + \dfrac{V_O}{n}$

and

$$\dfrac{V_O}{V_g} = n\dfrac{D}{D'} , \quad \dfrac{V_O}{n} = \dfrac{D}{D'} V_g$$

$$V_{tr}(\overset{\text{stand}}{\text{off}}) = V_g \left[1 + \dfrac{D}{D'}\right] = \dfrac{V_g}{D'} \text{ This is a peak value.}$$

(b) Find the rms current for on-conditions

$I_{Q1}(\text{RMS}) = I_g \text{ rms}$

$I_{Q1}(\text{rms}) = I\sqrt{D}$

I is in the magnetic

$$P_{load}/V_g\sqrt{D}$$

S active is the transistor stress!

$$S(active) \equiv V_{TR}(off)I_{Q1}(rms) = (V_g + \frac{V_o}{n})I\sqrt{D}$$

$$= V_g I\sqrt{D}/D'$$
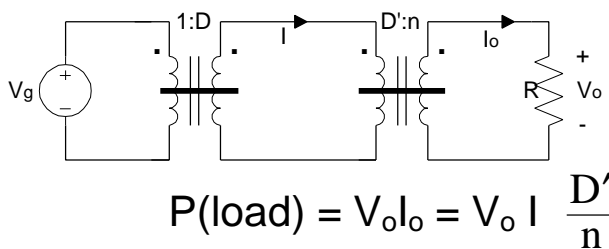
(c) Utilization $\equiv \dfrac{P(load)}{S(active)}$

(1) Lets find P(load) in terms of $V_o I_o$ for dc converter. Notice the three different currents in the flyback:

  I_g from dc input source: $I_g = DI$(magnetics)
  I_o into the load = I(magnetics)D'/N
  I the current in the magnetics

$$I_o = (I)\frac{D'}{n}$$

$$I = I_g/D$$

$$P(load) = V_o I_o = V_o I\frac{D'}{n}$$

2. S(active) should be in same variables as P(load) to get U(flyback).
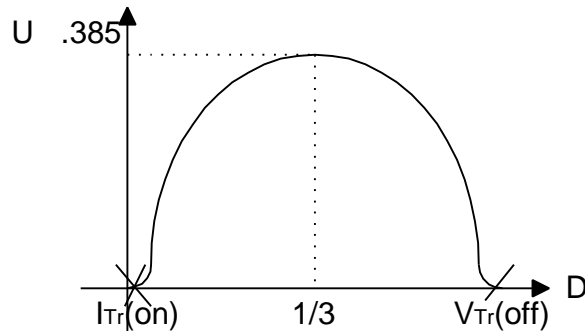
$$S(flyback) = \frac{V_g I\sqrt{D}}{D'} \text{ and } V_g = V_o\frac{D'}{n}\frac{1}{D}$$

$$S = \frac{V_o}{n}\frac{I}{\sqrt{D}} \quad \text{same variables as P(load) for flyback}$$

$$U(flyback) = \frac{P(loadflyback)}{S(activeflyback)} = \frac{V_o\,I\,\dfrac{D'}{n}}{\dfrac{V_o}{n}I/\sqrt{D}} = D'\sqrt{D}$$

To find U_{max}(flyback) versus D use dV/dD = 0.

$$dV/dD = \frac{\P[(1-D)\sqrt{D}]}{\P D} = 0$$

½ $D^{-1/2}$ - 3/2$D^{1/2}$ = 0 thus D = 1/3.

U_{max} = 0.385
at D = 1/3 for
1 transistor flyback

D = 1/3 minimizes the product of V_{tr}(off) * I_{tr} (on rms). We know a maximum occurs between D = 0, V = 0 and D = 1 V = 0 for the flyback. However, U_{max} is not the only issue so D @ U_{max} is a starting point all other issues neglected. In design we have some fixed quantities such as:

V_o, V_g and load power (V_o*I_o) product.

Then D and n for example are free to choose.

Summarize (transformer/isolated) flyback:

$$I_Q(rms) = I\sqrt{D}, \quad \frac{Vo}{Vg} = n\frac{D}{D'}$$

$$V_Q(off) = \frac{Vg}{D'}$$

Given:

$\frac{Vo}{Vg}$ fixed we can trade off n vs D to achieve $\frac{Vo}{Vg}$

Since $\frac{Vo}{Vg} = \frac{nD}{D'}$ two extremes are: (1) D → 1.0 ⇒ n ↓

but this means for fixed V_o, V_g ↑ which causes V_{tr}(off) ↑

(2) D → 0 ⇒ n ↑ on secondary but for fixed V_{out} this causes I_{tr}(on) ↑

∴ D ≈ 1/3 a good first guess.

# (3) General Table of Switch Utilization for Six Major Converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

	Converter	U(D)	max U(D)	max U(D) occurs at D=	
1	Buck	$\sqrt{D}$	1	1	
2	Boost	$\dfrac{D'}{\sqrt{D}}$	∞	0	
3	Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\dfrac{2}{3\sqrt{3}}$ =0.385	1/3	U↑ for nonisolated
4	Forward, $n_1 = n_2$	$\dfrac{1}{2}\sqrt{D}$	$\dfrac{1}{2\sqrt{2}}$ =0.353	½	
5	Other isolated buck-derived converters (full- bridge, half-bridge, push-pull)	$\dfrac{\sqrt{D}}{2\sqrt{2}}$	$\dfrac{1}{2\sqrt{2}}$ =0.353	1	isolated have U↓
6	Isolated boost-derived converters (full-bridge, push-pull)	$\dfrac{D'}{2\sqrt{1+D}}$	$\dfrac{1}{2}$	0	

Flyback line 3 you sacrifice U to achieve input/output isolation.
Some comments are:

(a) Line 3 flyback results also work for other converters.

(b) Line 2 boost without trf. isolation
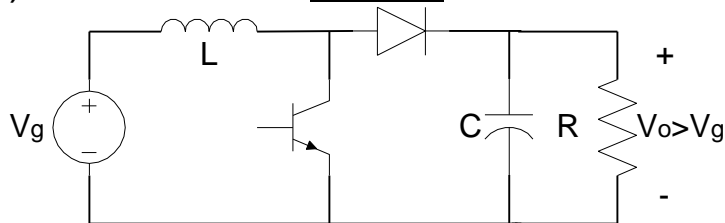
D = 0: Tr is always off, diode always on, U = P/S then goes to a large value.

No I_{on} stress but V_{off} (stress)

D = 0 gives maximum utilization but $V_o = V_g$ is limited.

(c) Line 6 only get a maximum switch utilization U=½ at D=0
Add transformer isolation to boost to get dc isolation BUT
V(off) on switches increases! WIN - WIN Case

(d) Line 5 full-bridge buck-derived
Given: $V_g = 500$ $V_o = nDV_g$
        $V_o = 5$
$P_o = kW$ is a fixed constraint
Choose n → 100 because D → 1 and at D = 1
U(max) = .35 the best we can hope for.

$$\frac{P(\text{load})}{S(\text{active})} \Rightarrow S(\text{active})@\,U_{max} = \frac{kW}{.35} = 2.9 \text{ kVA} = S_{max}$$

Compare to line 1 non-isolated buck $V_o = DV_g$ and
$V_g = 500$, $V_o = 5$ $I_o = kW$
$\Rightarrow$ D must be .01

$$\Rightarrow U_{max} = \sqrt{D} = .1, \quad S = \frac{kW}{0.1} = 10kVA$$

In summary the tradeoffs with extra cost of transformers and core reset complexity we find:

isolated buck	non-isolated
U higher	U lower
S lower	S higher

A reminder grading in this course is 60% HW (We are doing this weekly). So far we had
HW#1 Chapter 2 Erickson Pbms 2,3,4,6 and class note questions
HW#2 Chapter 3 Pbms 6,7 of Erickson and class note questions
HW#3 Chapter 6 Pbms 6,7 of Erickson and class note questions
HW#4 Chapter 4 Erickson Pbms2,4,5,6 and class note questions

Note that we reassigned HW pbm. 6.11 which is now a design problem due for your midterm exam not in HW # 3. See section 6.4.2 to guide you.

As a help to Erickson's Chapter 4 HW problems
below we give a converter circuit, analyze its DC states of operation to find the maximum or worst case DC voltage and current requirements of the switches employed in that specific circuit topology. These maximums set by the circuit must be exceeded by the manufacturers device specifications under all conditions of operation. There will be both DC maximums and transient maximums.

We will start with the DC levels.

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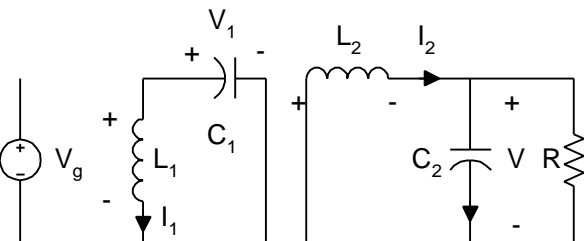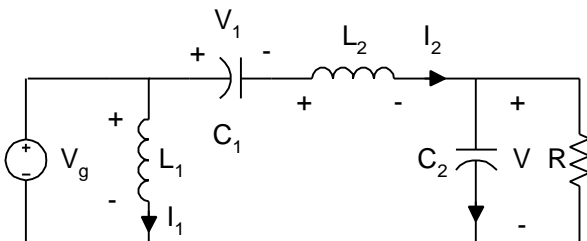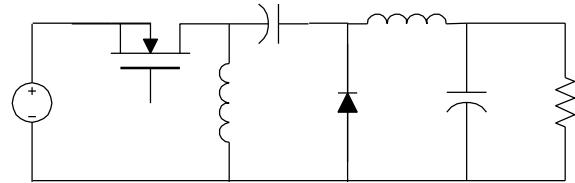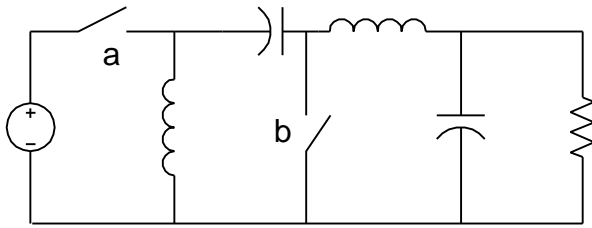
SWa on/SWb off
$V_{L1} = V_g$
$V_{L2} = - V_1 + V_g - V$
$I_{C1} = I_2$
$I_{C2} = I_2 - V/R$

Volt-sec balance on L_1

$V_{L1} = DV_g + D'V_1$

$V_1 = -\dfrac{D}{D'} V_g$

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SWa off/SWb on
$V_{L1} = V_1$
$V_{L2} = - V$
$I_{C1} = - I_1$
$I_{C2} = I_2 - V/R$

Volt-sec balance on L_2
$V_{L2} = D(-V_1 + V_g - V) - D'V$
$0 = - DV_1 + DV_g - V$

$= \dfrac{D^2 V_g}{D'} + DV_g - V$

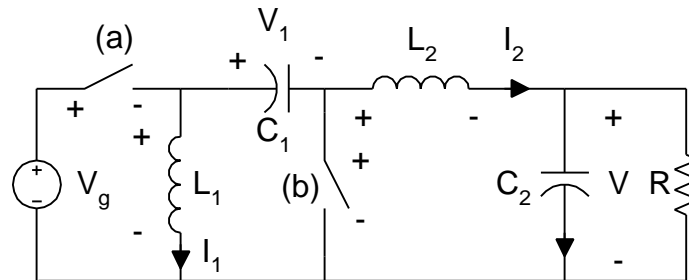$= \dfrac{DV_g(D+D')}{D'} - V$

$V_2 = V = \dfrac{DV_g}{D'}$

</div>

I-sec balance on C

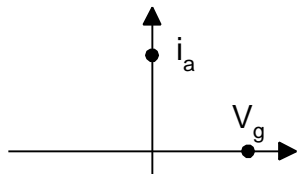$$I_{C1} = DI_2 - D'I_1$$

$$I_2 = \frac{V}{R}$$

$$I_1 = \frac{DV}{D'R}$$

The above equations give the equations for the DC operating voltages. Now we consider values of V_{off} and I_{on} for both switches.

Maximum DC switch ratings will be functions of both circuit values and switching duty cycles but will not vary with, f_{sw}.
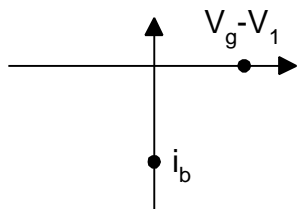
$\underline{V_{OFF}}$ and $\underline{I_{ON}}$ for switch a

$$V_a = V_g - V_{L1} = V_g - DV_g - D'\left(\frac{-D}{D'}V_g\right)$$

$$\therefore V_a = V_g$$

$$I_a = I_2 + I_1 = \frac{V}{R} + \frac{D}{D'}\frac{V}{R} = \frac{V}{D'R}$$

$\underline{V_{OFF}}$ and Ion for switch b

$$V_b = V_g - V_1 = V_g/D'$$

$$I_b = -I_1 - I_2$$

$$= \frac{-DV}{D'R} - \frac{V}{R} = -\frac{DV_g}{D'^2R}$$

$$\therefore I_b < 0$$

HW#4 problem 4.6 of Erickson, is a also a one quadrant switch