LECTURE 17
Bipolar Core Excited Boost Converters Utilizing $2T_s$ Timing and the Power Factor Problem

I. Boost: Bridge Rectified with 4 Switch Input
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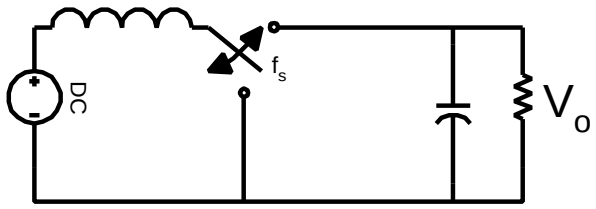
LECTURE 17

Bipolar Core Excited Boost Converters Utilizing $2T_s$ Timing and the Power Factor Problem

I. Boost-Based Isolated Converters Operating in CCM

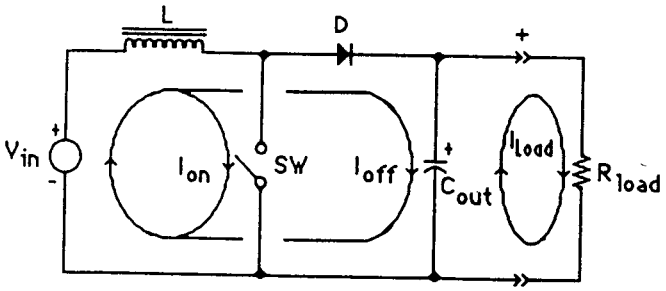
A. Review of Boost Topology

Inductor is attached to crude dc (rectified mains): again note that the inductor, L, is preventing kvl violations during switching as well as storing energy.

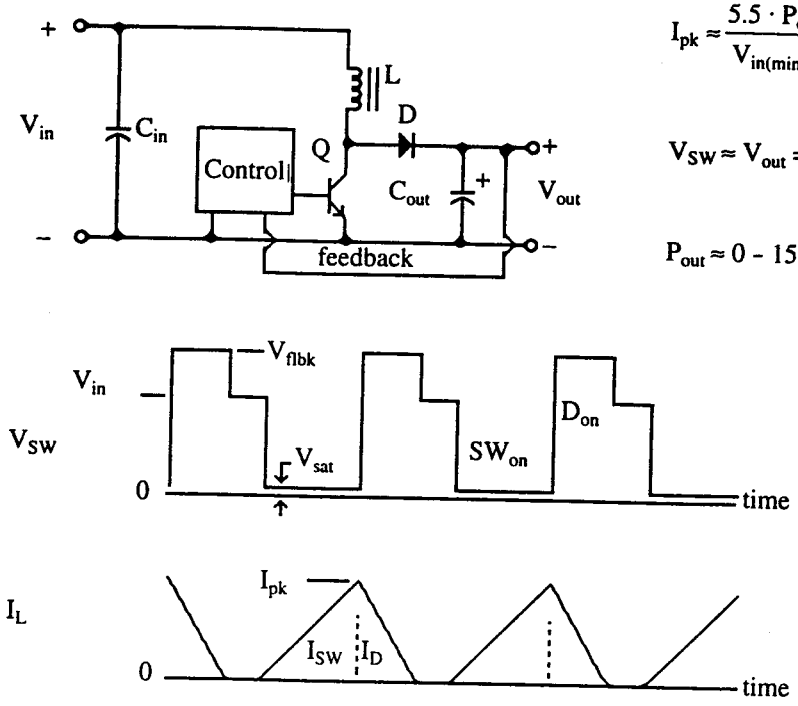


- V_{out} NEVER REACHES ZERO. v_{out}(minimum) = v_{dc} and can exceed v_{dc}
- V_{out} IS UNIPOLAR but can achieve $v_o > v_{in}$
- $V_o/V_{in} = 1 / (1-D)$. non-linear dependence on d will be shown in later lectures
- Note that the input and the output are NOT electrically isolated from each other as we have a common terminal to both the input and the output. How to easily fix this??. Finally, we consider one special case for the duty cycle- D=1/2

Consider the switch duty cycle of ½ and consider the power in the inductor for each switch position.
$p_{in}(av) = v_{dc}i/2$ while $p_{out}(av)=(v_{out} - v_{dc})i/2=p(inductor)$
if no losses occur in switching, wires or in reactive elements:
$p_{in}=p_{out}$ which implies $v_o=2v_{dc}$.



A basic flyback-mode converter (boost converter shown).



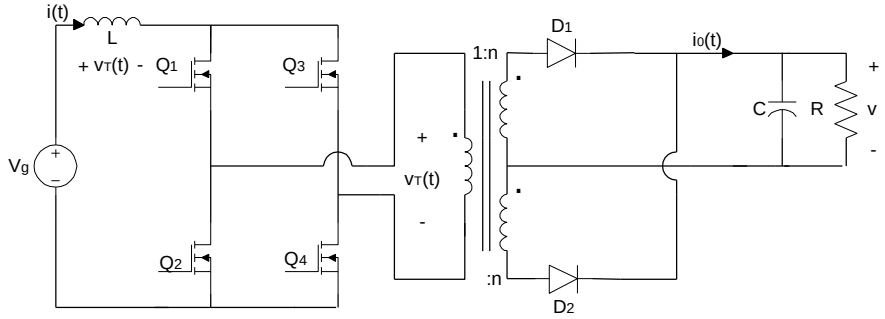
The boost regulator topology.

The boost circuit while delivering an output voltage above V(in) does have to ask the solid state switch to handle a **peak current 6 times the nominal** average current when the switch is on. When the switch is off the solid state switch must withstand across itself a voltage up to the full output value.

As the power required form the boost circuit increases above 150 W, the switch stress required of a single switch may become

excessive. Thus, ever more costly single switches are needed. We can get around this by employing more switches and dividing the switch stress among them. Hence, lower cost multiple switches may be employed. A boost circuit employing this approach is given below.

B. Full Circuit Topology and Advantages



Four Bridge transistors is costly but worthwhile if:

· Input current is steady and not a pulsating noise source to the line. This circuit will also be employed later, in Chaps. 15-18 of Erickson, as a low harmonic rectifier**. We will outline this a approach in part III of this lecture**

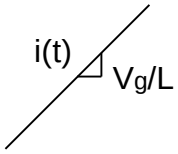
· Current like drive due to series L, of the transformer primary avoids undesired core saturation. If the transformer did saturate output diodes go off and we automatically get voltage balance as we show below.

· Timing sequence has <u>two</u> T_s periods, each has a D and D^1 section within T_s.

B. Four Transistor Boost Operating Conditions

1) First T_s Interval

V_p is primary: one coil
V_s is secondary: two center tapped coils

DTs	D'T_s
Q_1-Q_4 all on placing V_g across the series boost "L"	Q_1 and Q_4 on placing V_g on primary Q_2 and Q_3 off
	i_L built up in boost L is piped into the primary via Q_1 & Q_4
$V_p = 0$ so $V_s = 0$ and diodes D_1 & D_2 are both off with V_o+	$V_p = +V_g$ i_L enters primary into dot i secondaries by the dot turn diode D_1 on and diode D_2 off

2) Second T_s Interval

Same as first DT_s case above building up current in the series boost L during D and releasing this current during D'	Q_1 and Q_4 off Q_2 and Q_3 are on connecting the primary to $-V_g$ with - on the dot $\Rightarrow$ i_L goes into un-dot side of primary or out the dot side. $\therefore$ i_{sec} out of un-dot or into the dotted side causing D_2 on D_1 off

Balanced drive with ideal transistors says no core saturation occurs

$$\langle V_{primary} \rangle = \langle V_{Lm} \rangle = 0$$

Consider two cases:
(a) V_{on} of the transistors are equal
(b) Transistor off times are equal with no delays

$$\langle V_{secondary} \rangle = 0$$

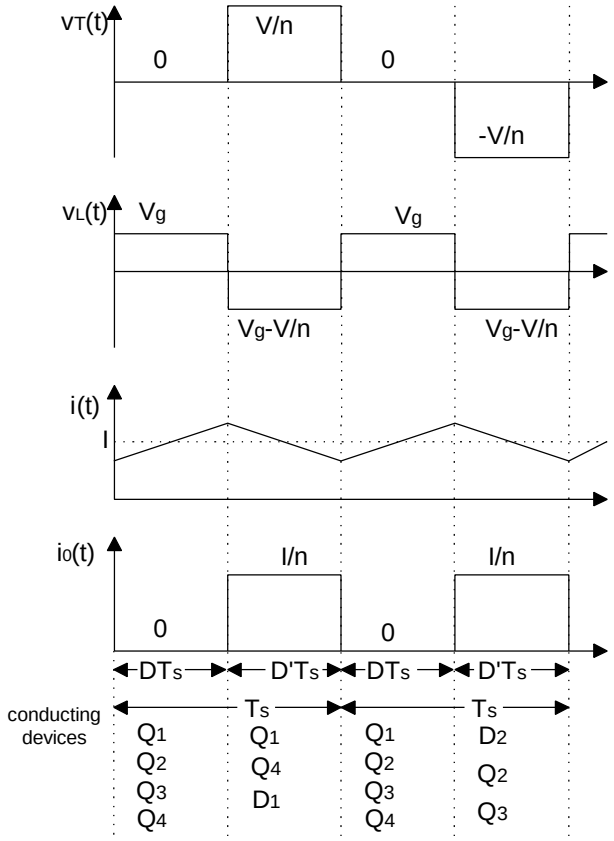
If:

(a) Both diodes V_{on} are equal.

$$<V_L> = 0 \; D(V_g)+D'(V_g-V/n)=0 \; \frac{Vo}{Vg} = M(D) = \frac{n}{D'}$$

gives flexibility to tradeoff n and D'. Also note V_o/n is the reflected load voltage to the primary = V_g/D'

C. i and v waveforms vs. $2T_s$

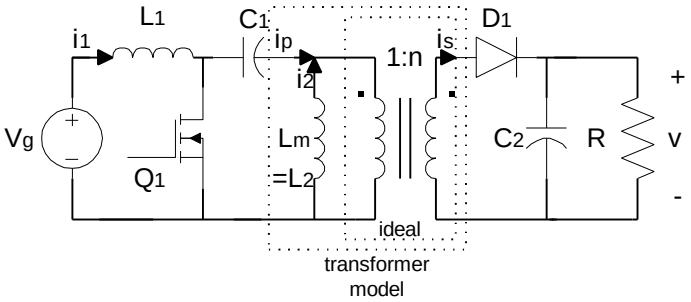


II. Transformer Isolated Two Inductor Converters in CCM

A. General Issues

Use n:1 in converters to give added flexibility for M(D) design at cost of increased switch voltage stress! Transformer acts both as flyback and as a regular trf as shown below in 2 and 3. Because of this topology magnetic core effects are even more complex than a flyback. See circuit below for sepic converter.

B. Sepic with Isolation



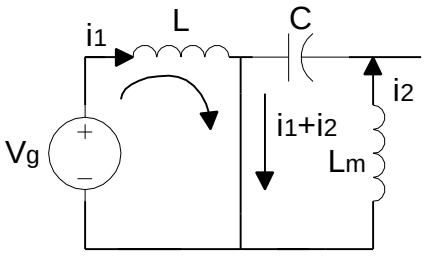
$i_p + i_2 = 0$ at primary node. isolates input dc from output.

Sepic current waveforms

DT_s: Trans Q_1 on but diode D_1 is off

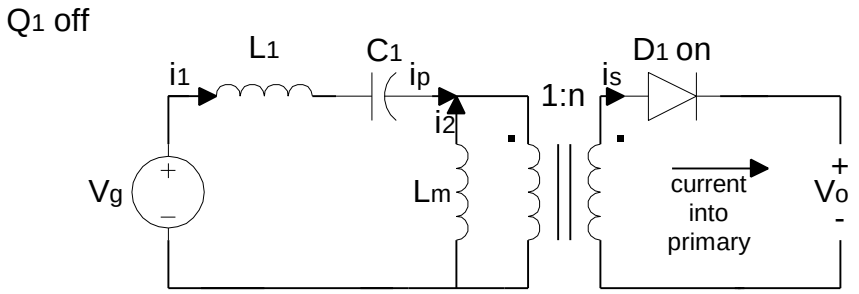
$\Rightarrow$ only i_m - flow is negative

Q_1 on



$V_s = 0$ since diode D_1 is off therefore $V_p = 0$ says no current drawn in primary from secondary loading

$D'T_s$: Q_1 off, diode D_1 on so i(secondary) times 1/n is drawn in primary,1 turn coil, and also in L_m we have the same current.



From mmf conservation we find i
$n_s i_s = 1*i(\text{primary})$ for the current directions shown above with i flow into the primary dot and out of the secondary dot.

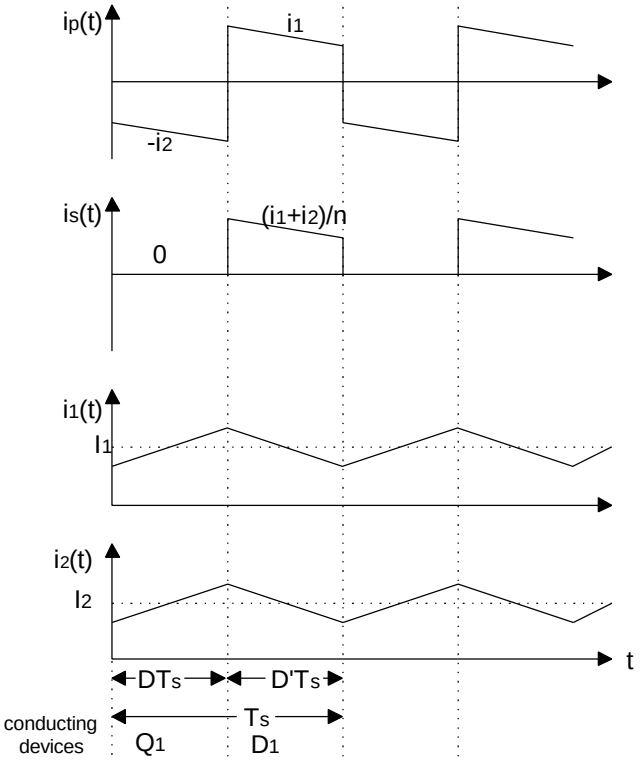
$\underline{n i_s} = i_p + i_2 = i_1 + i_2$

or $i_s = \frac{i_1}{n} + \frac{i_2}{n}$

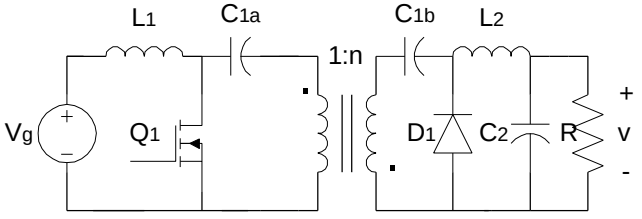
$\frac{V_o}{n}$ appears on the primary coil. Using v-sec balance on both L_m and L, we find:

$$\frac{Vo}{Vg} = \frac{nD}{D'}$$

tradeoff $\rightarrow$ n, D & D'
Since the transistor must block V_g/D' we want D' large.



C. Cuk with Transformer Isolation



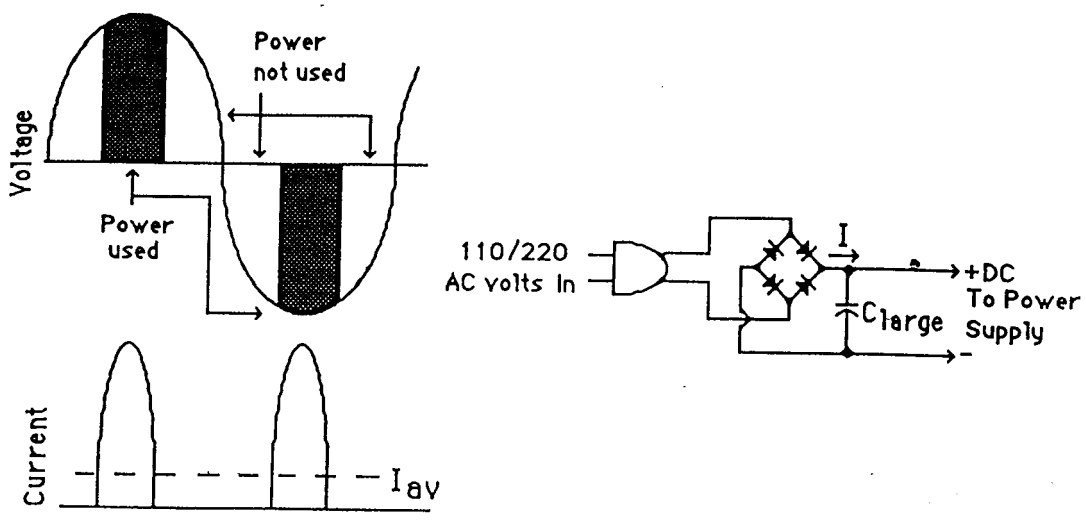
Later will show use as a low harmonic ac-dc converter. Primary is the same as sepic.

II. The Power Factor and Harmonic Pollution Problem with PWM Converters

We will below briefly cover the two major problems of PWM converters that must be recognized early, if we are to be honest about power electronics. In the second semester we will give full blown solutions to both problems that we only outline here.

A. The Power Factor and Harmonic Pollution Problems and International Laws

The use of direct Ac to Dc conversion on the front end of a PWM converter introduces two major problems due to the very different waveforms for the input voltage and current as shown below

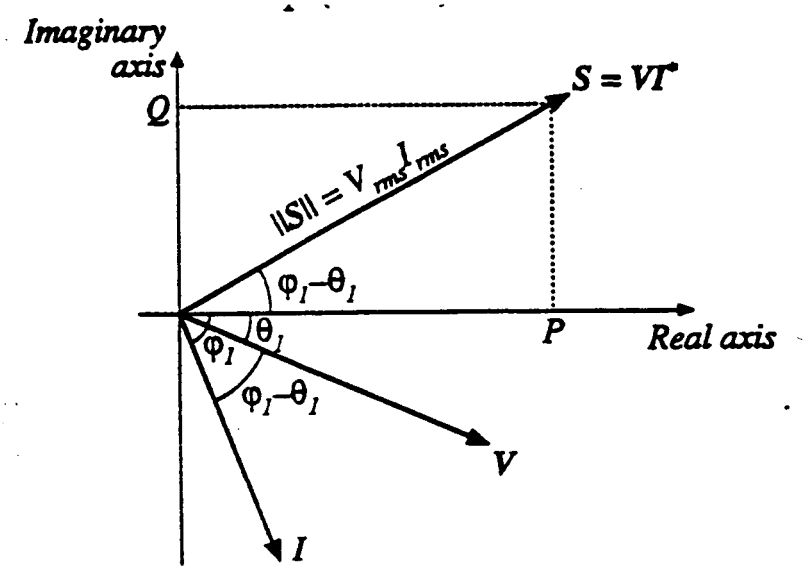


The waveforms of a capacitive input filter.

The power factor is poor and harmonics high.

1. Power Factor

We are no faced with the fact that the power factor for power supplies is below 0.5 while the power industry requires the power factor to be above 0.9. This is demanded because the power company must generate an apparent power S (V-A units) in order to provide real usable power, P(Watts). We inadvertently generate a large and unwanted amount of reactive power, Q in VARS when employing PWM converter technology as shown below.



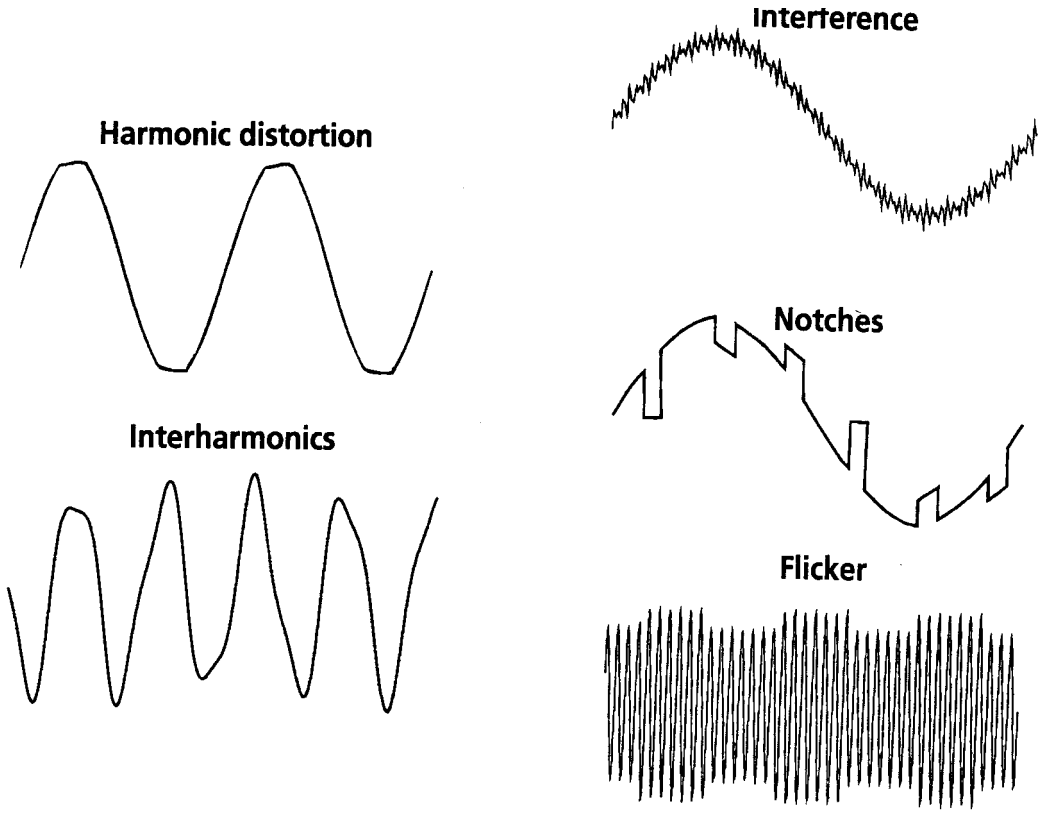
Power phasor diagram, for a sinusoidal system, illustrating the voltage, current, and complex power phasors.

That is, we force the utility to provide an excess generating capacity, thereby wasting valuable non-renewable resources. We seek ways, therefore, to make the current waveform more closely follow the

voltage waveform and reduce unwanted VARS, Q. This will require us to increase the conduction angle of the rectifiers, making the current waveform more sinusoidal. As a rule of thumb, a rectifier must conduct for at least 315 of the 360 degrees to reach a power factor of 0.9. The dead angle of conduction must not exceed 45 degrees.

2. Harmonic Pollution

The non-sinusoidal current waveform creates harmonics and other conductive EMI on the mains.



Harmonic pollution causes a variety of failures on equipment connected to the same mains. These include: transformer burnout, capacitor and inductor failure, flickering lights and oscillations in motors. In

the US Navy failure of critical weapons and computer systems has occurred. The spectrum of interference from AC to Dc conversion in the old fashion way is much wider than you might guess as shown below in a histogram of harmonic amplitudes.

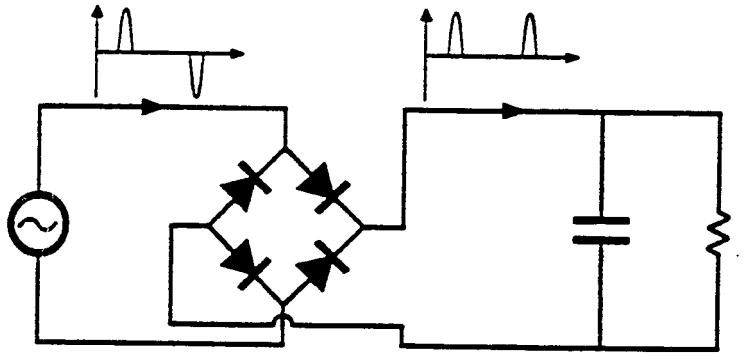
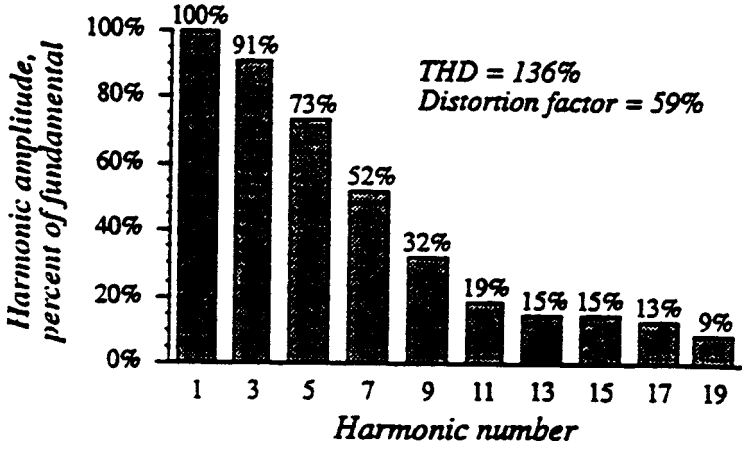


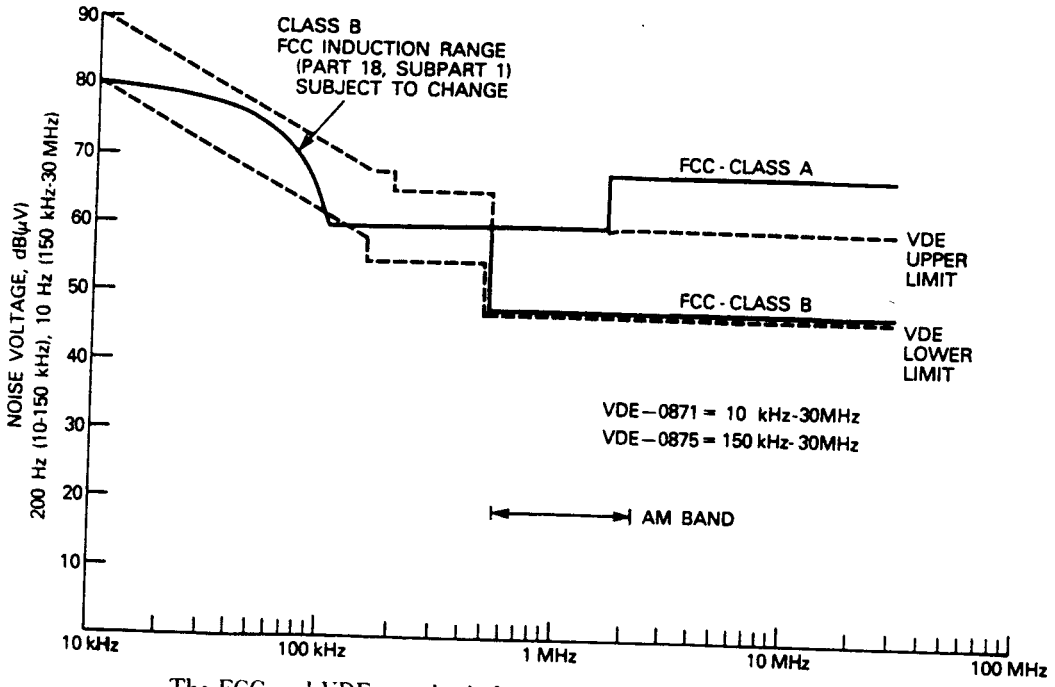
Fig. 15.6. Conventional peak detection rectifier.



Typical ac line current spectrum of a peak detection rectifier. Harmonics 1-19 are shown.

As a consequence, of the mains driven failures of associated equipment new LAWS have been written in the world that make certain old fashion electric

circuits ILLEGAL. On the following page we show the allowable noise voltage levels versus frequency as well as a table of absolute current limits



The FCC and VDE standards for conducted EMI.

We now must build power supplies that meet the laws in various countries in the world. Europe's laws are stricter than the USA-why??

In Europe the electrical system distributes mains at 240 Volts so they can use smaller guage wire and lower amperage fuses. But, this makes Europe more sensitive to harmonic currents than the USA. The European standards are called IEC 555 and are summarized on the following page. There are three broad categories of electrical equipment, which are termed A, B, C, and D. Each has a different EMI

standard to meet. See the next page for a table of allowed harmonic current limits for equipment having an input current below 16 A connected to 240 V.

IEC 555 HARMONIC CURRENT LIMITS

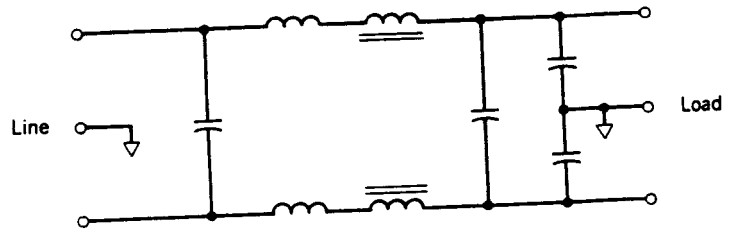
Odd harmonics (n)	Class A limits (A)	Class D absolute (A)	Class D relative mA/W
3	2.30	1.08	3.6
5	1.14	0.60	2.0
7	0.77	0.45	1.5
9	0.44	0.30	1.0
11	0.33	0.18	0.6
13	0.21	0.15	0.51
15 to 39	0.15x(15/n)	0.18x(11/n)	0.6x(11/n)
Even harmonics			
2	1.08	.3	1
4	.43	.15	0.5
6	.3	-	-
8 to 40	0.23x(8/n)	-	-

Power supply manufactures are concerned with only Class A and D. It is in general twice as hard to meet class D requirements as class A specifications. For example, class A equipment limits third harmonic current to 2.3 A while class D limits third harmonic to just 1.08 A. In short, a PWM converter drawing more than 150 W form the mains will exceed class D rules, while the same power supply could draw 300 W from the mains before violating

class A regulations.

3. Old Fashion Attempts to Solve these Problems
    a. Filter for conductive EMI

A simple input filter between the mains and the input rectifier could employ **series inductors** to increase or extend the conduction angle of the line or mains current and capacitors to take out any high frequency harmonic pollution. This is cost effective but requires a big and heavy inductors and capacitors operating at mains frequencies not suitable to all applications. This is shown below.

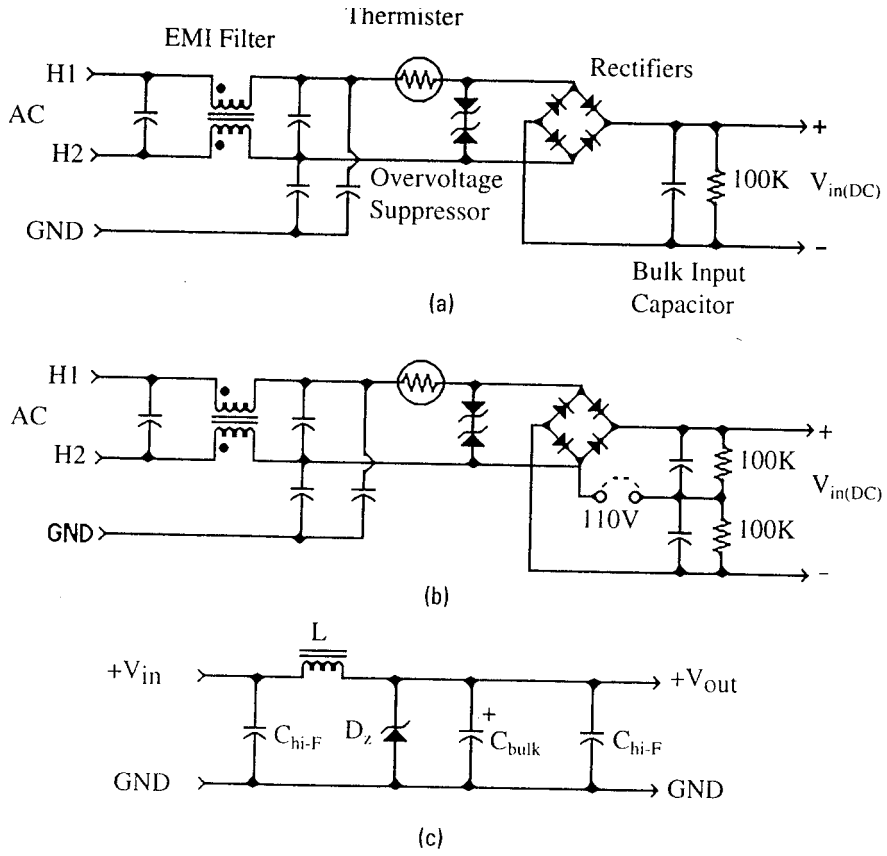


Filter for conducted EMI.

To improve on this basic EMI filter we could add:

- A thermister to limit peak current
- Overvoltage suppressors to eliminate peak excursions above the expected levels
- Of course we would need the classic EMI filter as well as the bulk input capacitor

The three to five part input rectifier/filter section is shown on the following page and was adequate for many applications, but not all.

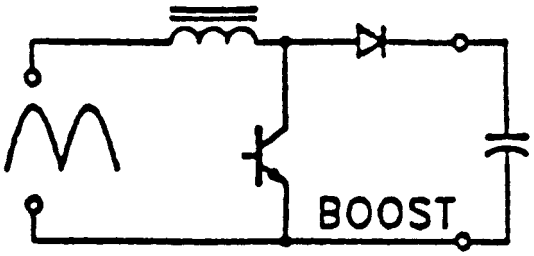


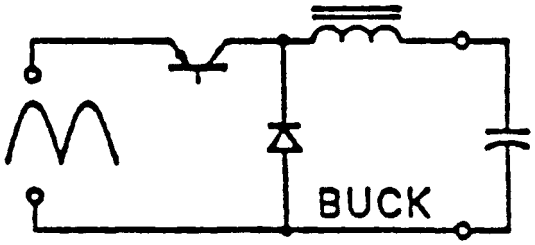
Typical ac and dc input filter circuits. (a) AC input filter circuit for a single or universal input power supply (common-mode EMI filter shown). (b) Voltage doubling ac input circuit for 110 V and 220 V ac inputs. (c) Single dc bus input filter.

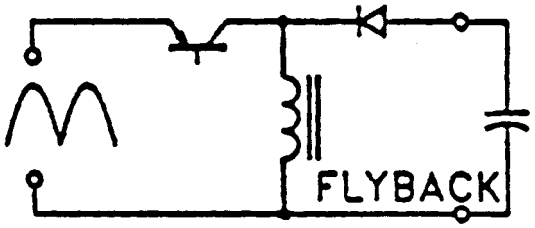
This old fashion solution was replaced by a programmed active switch power electronics solution that could be varied to meet all four classes of EMI interference as well as various countries varying EMI laws. Moreover, the solution was, you guessed it, lighter, smaller and more efficient than the above passive circuit solution.

B.Power Electronic Solutions

The key concept is to introduce active switching to increase the rectifiers conduction angle. We also wish to do so with small, light and efficient means. Of the three basic topologies shown below which is best suited to the tasks and why??



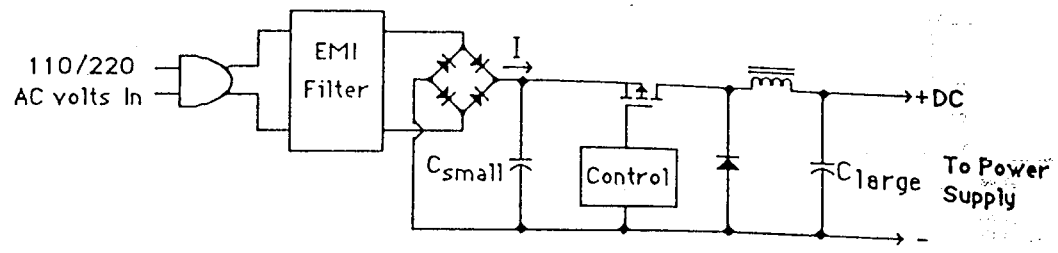




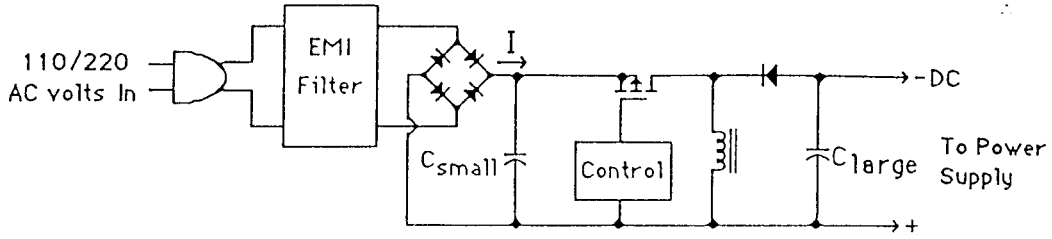
The boost converter is best because:

- the V(out) exceeds V(in) enhancing the energy storage capacity of the capacitor
- The boost provides a more stable V(out) with larger variations in the input mains voltage

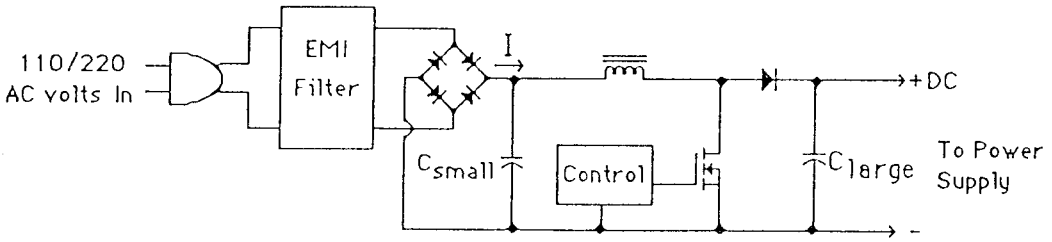
On the next page we more fully compare the three



A buck power factor correction circuit.

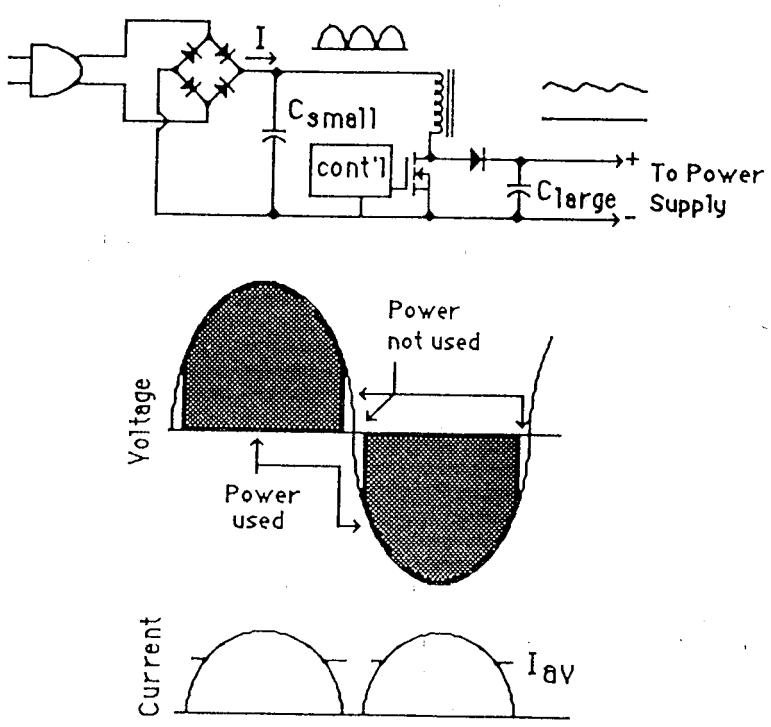


A buck/boost power factor correction circuit.



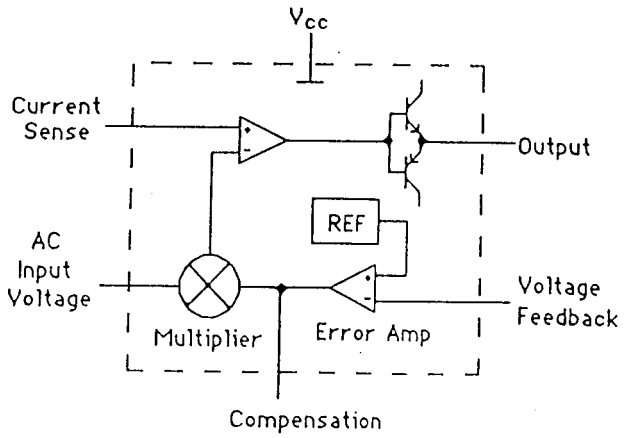
A boost power factor correction circuit

Notice that the boost converter topology has a low side switch that is easy to drive , whereas the buck-boost need a high side switch drive. Also the buck-boost gives a negative output while the boost gives a positive polarity output. The only restriction to the boost is that the V(out) must exceed 390 V to be useful in all world-wide power grids. 390 V is the highest expected AC crest voltage world-wide. The result is a low weight, small size, and highly efficient power corrected rectifier that can be suitable for universal power supplies as shown on the next page.



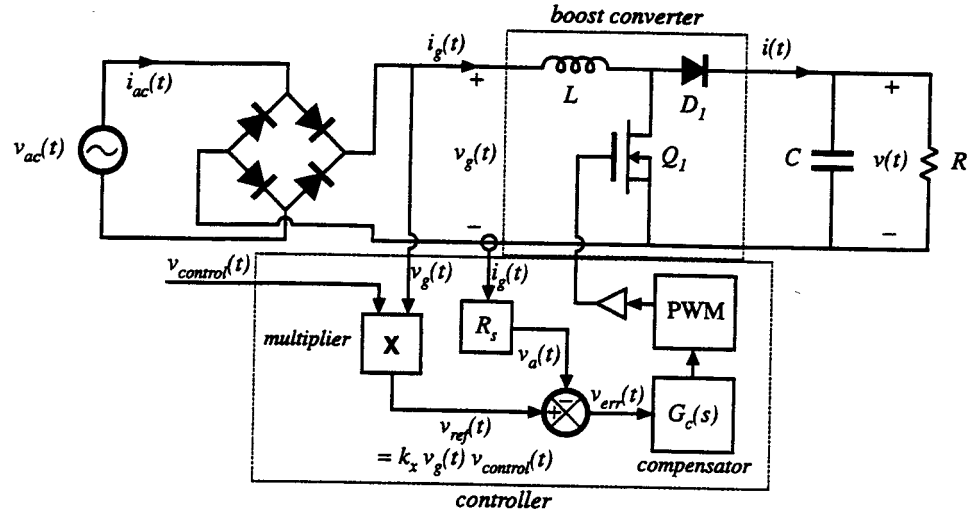
Power factor corrected input.

In this circuit fix to the rectifier problem we achieve both improved power factor and reduced generation of conductive EMI and do so in a universal way. We also allow for control programming to meet various laws in differing countries for four classes of EMI-A through D. Control of the power factor correction is beyond this lecture and will be covered in second semester. However, we will outline the solution to give a sense of completion to this section. The key point is to employ current mode control to extend the conduction angle in a controlled way as shown on the next page.



A generalized typical power factor control IC.

A multiplier subsection takes the product of the full wave rectified voltage waveform with the output of the error amplifier. This makes the input currents follow a sinusoidal wave-shape over a wider conduction angle. A full schematic with a multiplying controller is given below.



Rectifier system based on the boost converter, with multiplying controller.