LECTURE 16
Bipolar Core Excited Full Bridge and Push-Pull Converters Utilizing 2T$_{sw}$ Timing
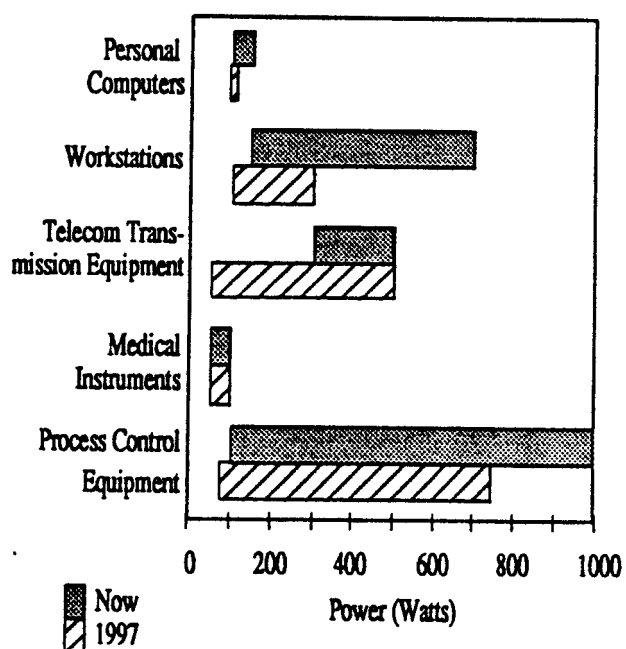
I. Full Bridge and Push-Pull Converters
    A. General Issues

    B. Alternating $\pm$V$_g$ but balanced Primary Drives: +V$_g$ and zero for first T$_{sw}$ followed by -V$_g$ and zero for second T$_{sw}$

    C. Bridge Rectified Buck with 4 Switch Input
        1. 2T$_{sw}$ drive timing
            a. Primary Conditions D and D' during first T$_{sw}$
            b. Secondary Conditions D and D' during second T$_{sw}$
        2. Input/Output Currents
        3. i and v Waveforms over 2T$_{sw}$
        4. Other 2T$_{sw}$ Switching Schemes

A. General Issues
    1. Power Levels
The power needs of various electronic power supplies varies as shown below.

A bar chart titled "Power (Watts)" showing two series, "Now" and "1997", for the following categories: Personal Computers, Workstations, Telecom Transmission Equipment, Medical Instruments, and Process Control Equipment. The x-axis ranges from 0 to 1000.

As the power level changes we also will need to determine which of the big eight PWM converter topologies is best suited to the required power level. Choice of PWM topology will in turn determine the switch stress experienced by the power switches. Moreover, the timing sequence for driving the various topologies will also vary. In particular, we will cover both switches drives at f_{sw} and switches synchronized at $\frac{1}{2}$ x f_{sw} in our discussions below. On the next page we briefly summarized what we learned in lecture 11 as regards switch topology and power as well as voltage and current levels in the associated switches.

In lectures 16 and 17 we will cover the last of the big eight topologies. We need to employ these circuits to achieve kW power operation. With topology comes different switch stress. That is as the input voltage changes we use different topologies as shown below. The flyback has low parts count but high peak currents than those in a forward converter. The half bridge reduces switch voltage stress because only ½ the V_{in} appears across the primary winding. The full bridge requires four switches, two of which require floating gate drive. The push-pull, as we will see below, also works but has a danger of CORE SATURATION. This could cause us to fry the switch if not careful to balance the

Comparison of the PWM Switching Regulator Topologies

Topology	Power Range (W)	$V_{in(dc)}$ Range	In/Out Isolation
Buck	0–1000	5–1000	No
Boost	0–150	5–600	No
Buck-boost	0–150	5–600	No
Half-forward	0–150	5–500	Yes
Flyback	0–150	5–500	Yes
Push-pull	100–1000	50–1000	Yes
Half-bridge	100–500	50–1000	Yes
Full-bridge	400–2000+	50–1000	Yes

core so that no imbalances or DC levels occur.
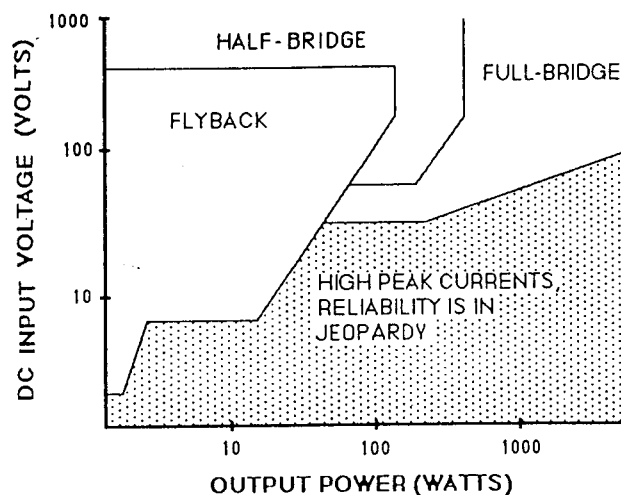
Where various transformer-isolated topologies are commonly used.

2.   Timing Sequence

To date we have employed switches driven at f_{sw}. Today we will change this timing on individual switches to $f_{sw}/2$ so that we can use more switches with less stress per switch as we describe below in more detail

B.   Alternating $\pm V_g$ but balanced Primary Drives: $+V_g$ and zero for first T_{sw} followed by $-V_g$ and zero for second T_{sw}

Bridge type isolated Buck converters are employed with two separate but balanced T_{sw} time periods. This is timing sequence is used for high power converters P > 1kW since we employ twice as many switches to reduce switch stress. Below we will first introduce the concepts via a half bridge and then employ a full bridge with a full analysis.

$$I_{pk} \approx \frac{2.8 \cdot P_{out}}{V_{in(min)}}$$

$$V_{SW} \approx V_{in}$$

$$P_{out} \approx 0 - 500 \text{ W}$$
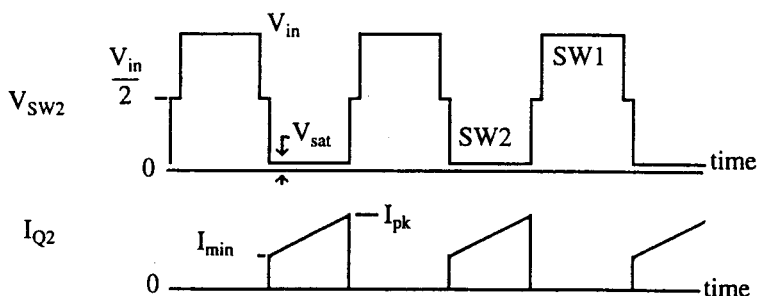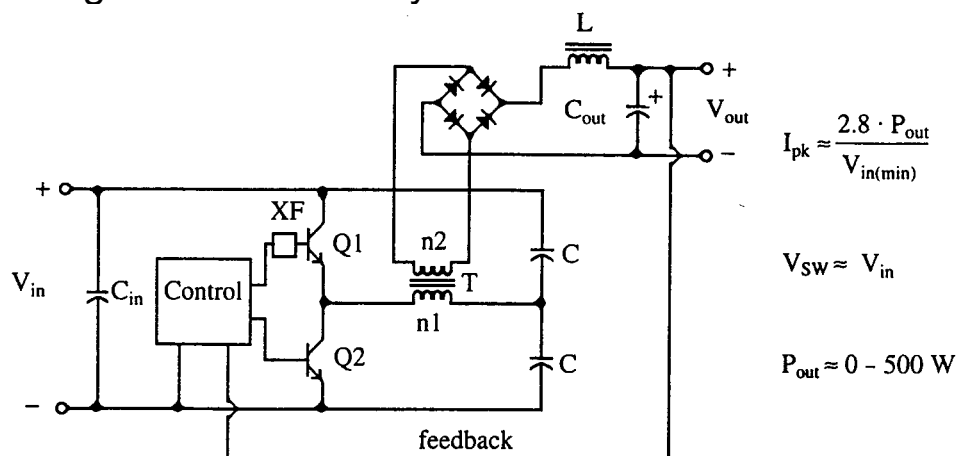
The half-bridge regulator topology.

Notice that the two switches alternate in time applying V_{in} alternatively to the transformer primary. Switch voltage stress is
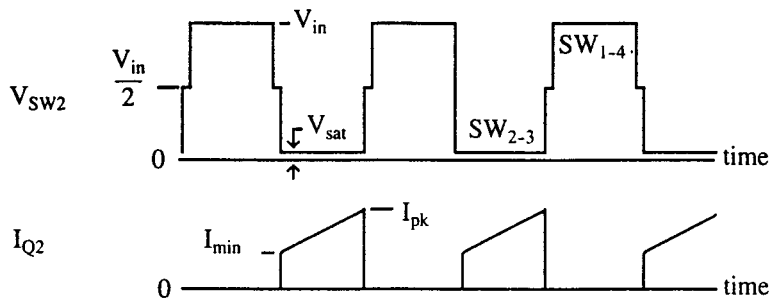
Given by the full input voltage. A similar situation occurs for the full bridge shown below which also alternatively places V_{in} across the primary winding, but this time using four switches.
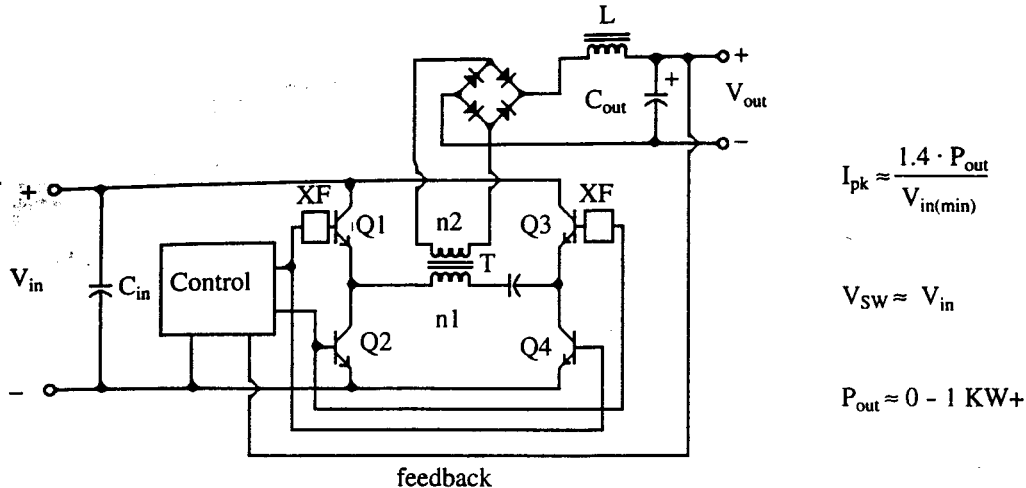
$$I_{pk} \approx \frac{1.4 \cdot P_{out}}{V_{in(min)}}$$

$$V_{SW} \approx V_{in}$$

$$P_{out} \approx 0 - 1 \text{ KW+}$$

feedback

The full-bridge regulator topology.

We synchronize switches 1 and 4 together in time and then switches 2 and 3. Note that we place the full V_{in} across two switches in series when the timing puts Sw_{2-3} in the same sequence and SW_{1-4} in the alternative sequence. Hence, we reduce switch voltage stress when we employ the required high input voltage to reach high power levels. Again we have a trade-off as we employ more switches but their individual cost may well be much lower-hopefully a factor of ten.

On the next page we will summarize the switch sequence as well as the voltage ramp on the duty cycle circuit for the full bridge converter topology.

Full-bridge DC-DC converter

Assumptions:

$i_L > 0$ (CCM)

$v_o(t) \approx V_o$
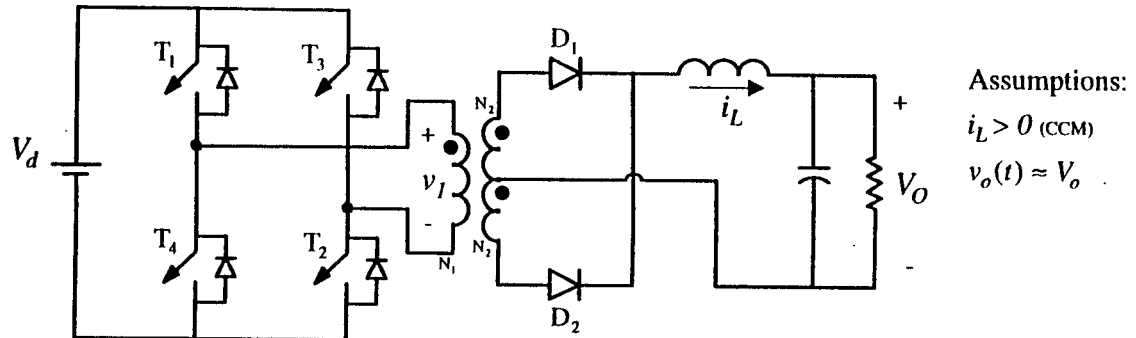
Control
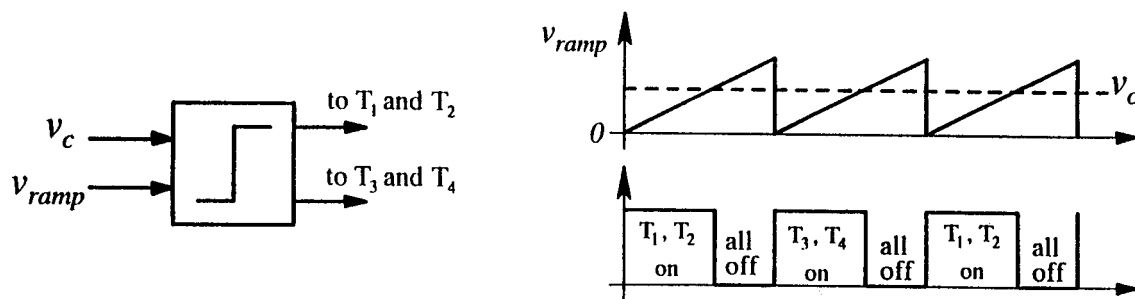
Now we are ready to go step by step through the timing sequence when the primary is driven by + and − V_{in} and the secondary is center tapped.

1.   Primary During balanced drive of duration $2T_s$

Match components very well to get V_{dc}(offset) on the core zero if the two switch periods are exactly balanced. Use a bridge circuit to drive the input to the transformer alternatively positive and negative. Output of the transformer is center tapped as shown below.
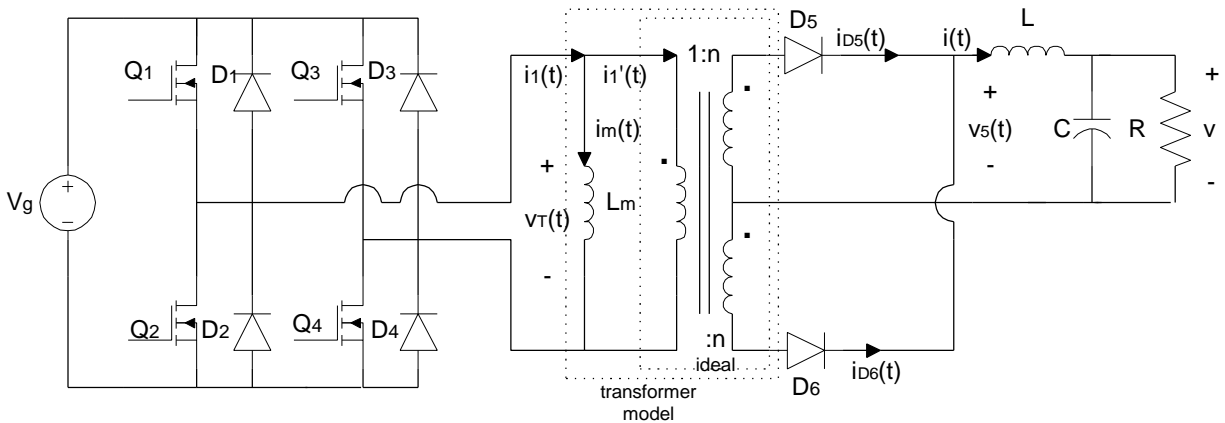
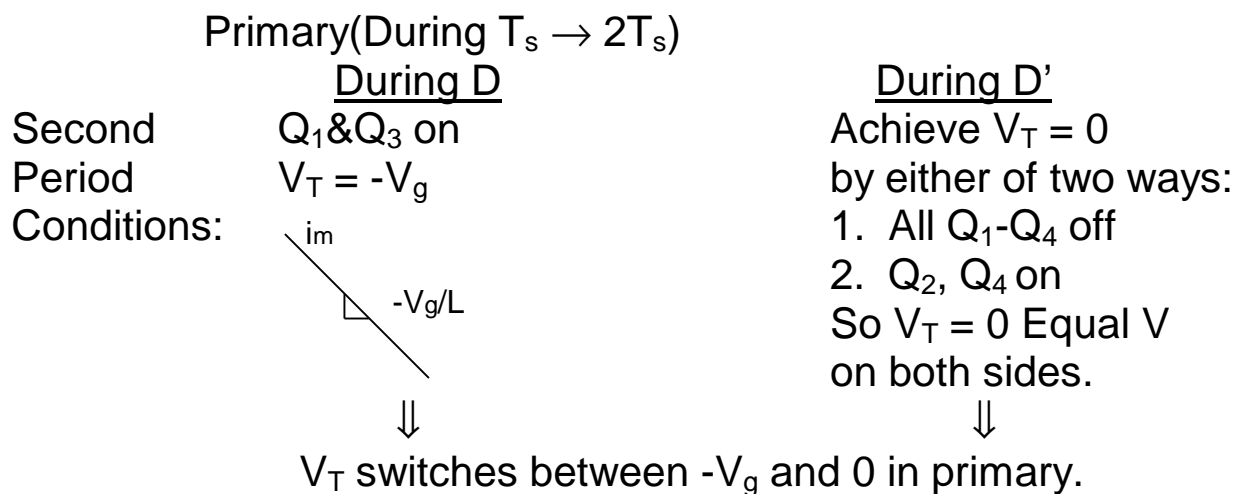a. First T_s switch interval: $+V_g$ and zero applied sequentially

There are therefore two T_{sw} intervals one with $+V_g$ and one with $-V_g$ across the primary. Below is that during the first T_s in the primary with $+V_g$. V_T switches between 0 and V_g like non-isolated buck as follows during T_{sw}. During D V_g is applied and during D' zero is applied.

<u>Primary</u> (during first T_s)

<u>During D</u>	<u>During D'</u>
Q_1&Q_4 on	To achieve
$V_T = V_g$	$V_T = 0$

either of two ways:
1. All Q_1-Q_4 off, $V_T = 0$
2. Q_1, Q_3 on, $V_T = 0$

$V_T \equiv 0$ via equal V both sides
This means i_{Lm} is flat during D'

im / V_g/L
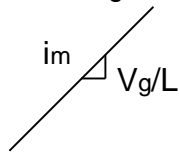
b) Second T_{sw} interval: $-V_g$ and zero applied

The primary circuit looked at during the second T_s timing interval is different $T_{sw} \rightarrow 2T_{sw}$ because $-V_g$ is applied during D and zero during D'.

Primary(During $T_s \rightarrow 2T_s$)

	During D	During D'
Second	Q_1&Q_3 on	Achieve $V_T = 0$
Period	$V_T = -V_g$	by either of two ways:
Conditions:	im	1. All Q_1-Q_4 off
		2. Q_2, Q_4 on
	-Vg/L	So $V_T = 0$ Equal V
		on both sides.
	⇓	⇓

V_T switches between -V_g and 0 in primary.

By symmetry we <u>reset</u> the core of the transformer L_m over $2T_s$. Up during D of the first T_s and down during D of second T_s.

$$\langle v_{Lm} \rangle_{2Ts} \equiv 0$$

Because of the switching configuration the transformer waveforms are at a frequency $f_s/2$, not at f_{sw}.

2. Secondary Voltage V_s Timing:

a) During first T_s interval

During D	During D'
V on secondaries	V on secondaries
<u>is $nV_g \equiv V_s$</u>	<u>is zero as $V_T = 0$</u>
* on coils tell	* on coils tell
diode D_5 on and	<u>both</u> D_5 and D_6 will be on
diode D_6 off	D_5 stays on due to i_L
	D_6 goes on due to
	secondary polarity and
	the dot convention

b) During Second T_s interval

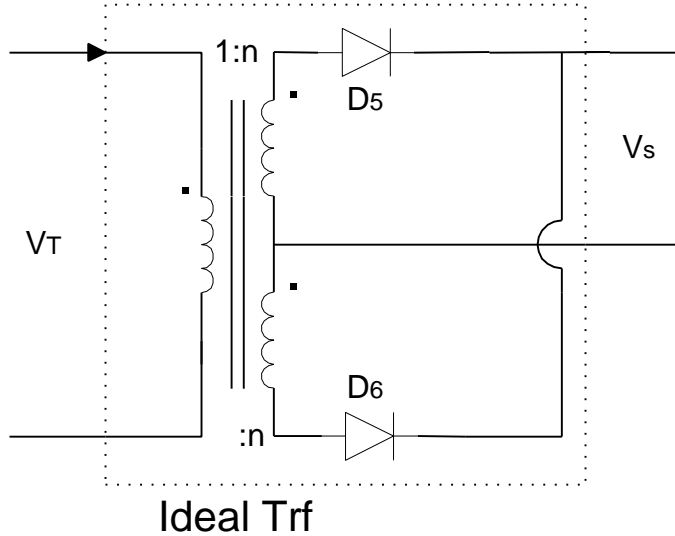Find on your own for D Q_2, Q_3 and D_6 are on while for D' diodes D_5

and D_6 are on.

    2.   Input and output currents

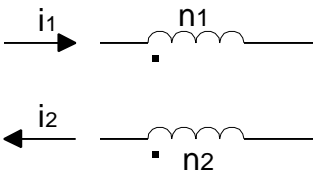i(out) = i_{D5} + i_{D6}. How it splits is uncertain, but if at anytime it

splits equally then: $i_{D5} = i_{D6} = \dfrac{i(out)}{2}$

During first T_s interval i_{in}(transformer) = ? When i_{D5} = i_{D6}

Ideal Trf

At the output
i_{D5} + i_{D6}
while in the primary
i_{D5} causes ni_{D5}
i_{D6} causes ni_{D6}

Review the dot convention on a two turn transformer that says:

if n_1i_1 is positive $\Rightarrow$ +n_1 then

is negative $\Rightarrow$ -n_2i_2

watch dots i_1
n_1i_1 + n_2i_2 = 0

coming into the dot
in secondary and
into dot of primary

At the primary on top of the page we have three currents.
i_{D5} and i_{D6} flow in opposite directions with respect to the coil dots:
i_{in} and i_{D6} are assumed flowing into the dot

    i_{in} - ni_{D5} + ni_{D6} = 0 $\Rightarrow$ i_{in} = 0
     ↓   ↓   ↓

```
        flows      cancel        assuming
     out of dot    if equal      i_{D5} = i_{D6}
```

For I_{in} alternating then in general i_{D5} and i_{D6} alternate the flows as shown below but always the load receives current either for i_{D5} or i_{D6}:
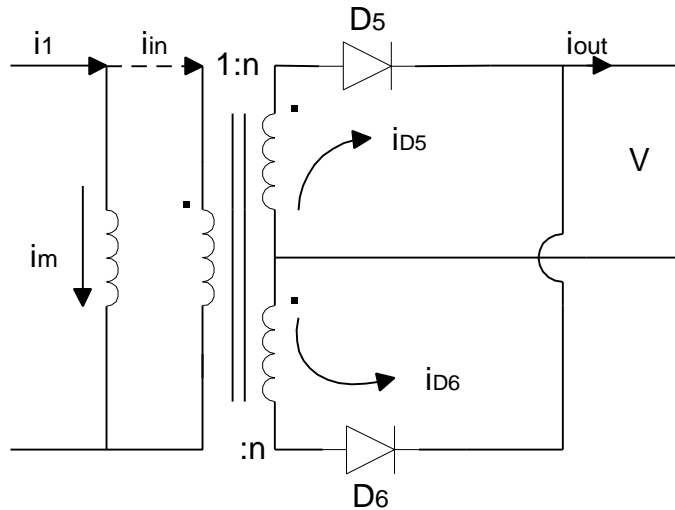
$i_1 = i_{in} + i_M.$

During the first T_s we find during interval D the two equations

below $i_m = i_1 - ni_{D5} + ni_{D6}$ }   Transformer input

           $i(out) = i_{D5} + i_{D6}$ }   Transformer output

During the second T_s period $T_s \rightarrow 2T_s$ during the same interval D we get the <u>same result</u> for i_m and i_{out}. Note in the first T_s with $+V_g$ applied $i_{D5} \neq 0$ but $i_{D6} = 0$. Where as in the second T_s with $-V_g$ applied $i_{D5} = 0$ but $i_{D6} \neq 0$.

           $\Rightarrow$ Switching ripple at f_s

           $\Rightarrow$ Transformer ripple occurs at $f_s/2$!

3.   Selected i and v waveforms vs $2T_s$ in the Bridge Converter
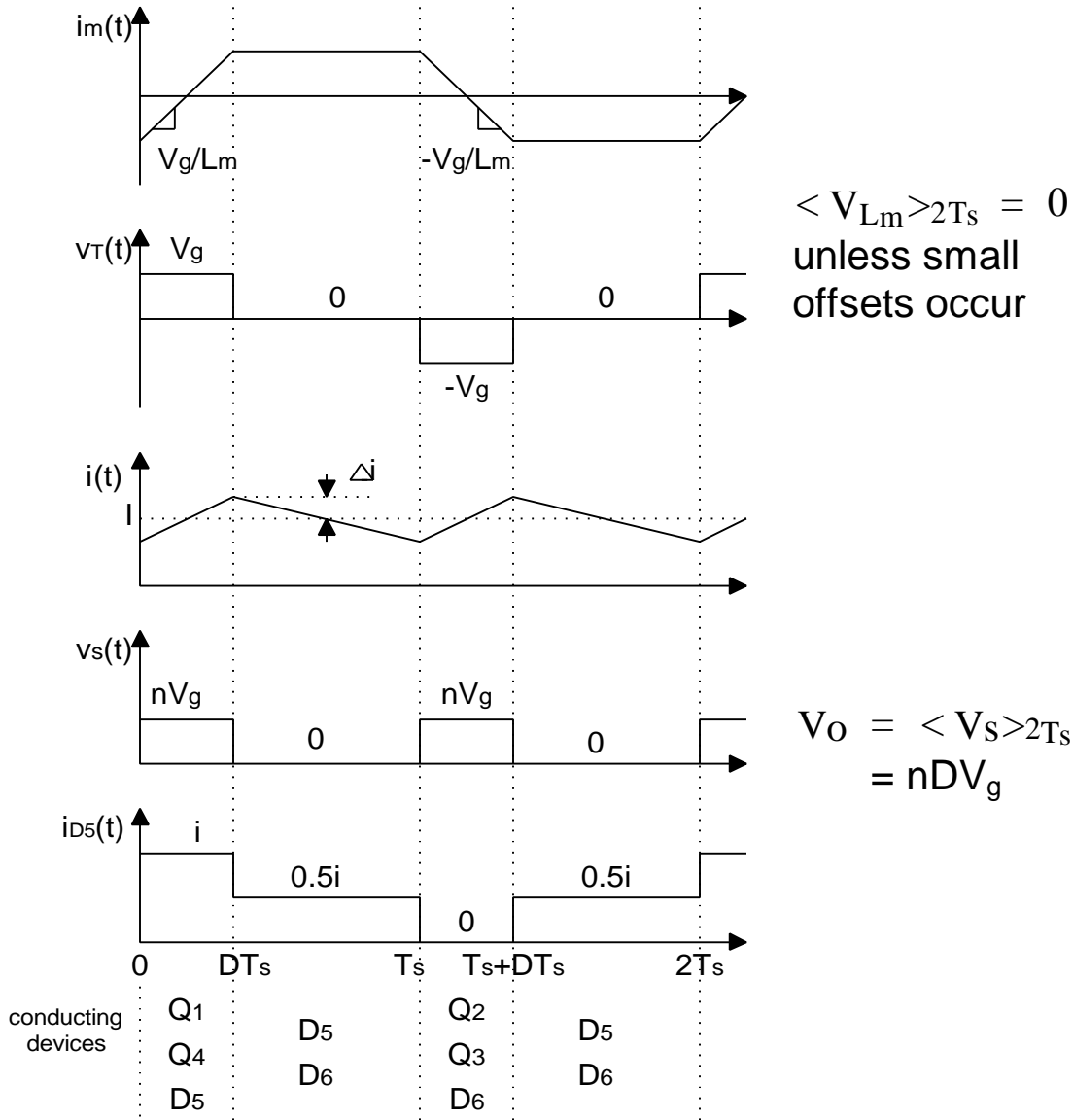

$<V_{Lm}>_{2T_s} = 0$
unless small
offsets occur

$V_O = <V_S>_{2T_s}$
$= nDV_g$

Clearly Q_1 and Q_2 cannot both be on at the same time nor Q_3 and Q_4 or V_g is shorted all other commutations are possible. D_1 and D_2 clamp the primary to a maximum of V_g.

Note bipolar use of the primary i_{LM} winding. The center tapped secondary winding is unipolar since in each half cycle alternate coils conduct.

4.   Other switching schemes over a $2T_s$ period are also possible that include.

1.   Alternative polarities applied to V(primary) during 1st and 2nd T_s periods for duration DT_s.

2.   A dead active switching period during both 1st and 2nd T_s periods, where all switches are off.
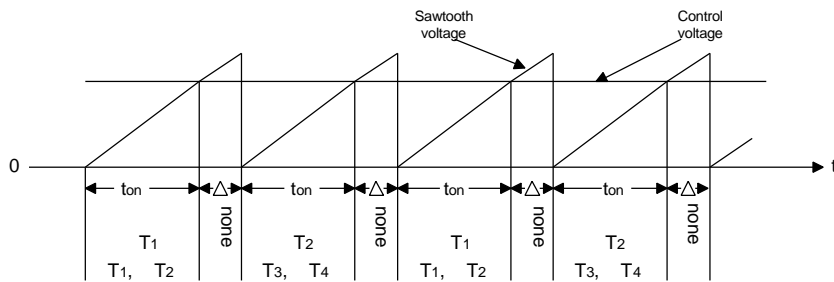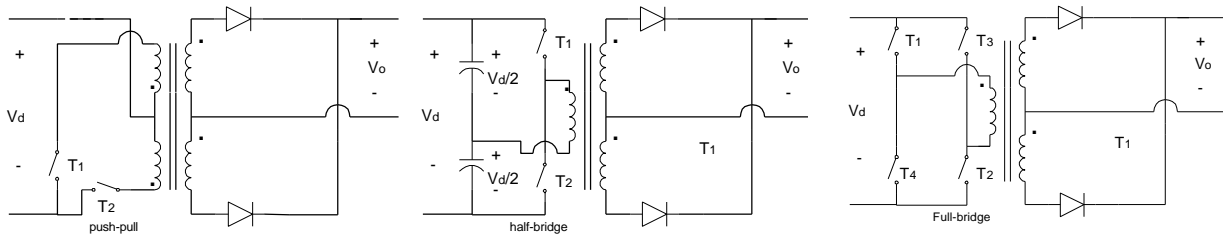
Explore this possibility for an extra credit HW assignment.

5.   Switch Stress Review

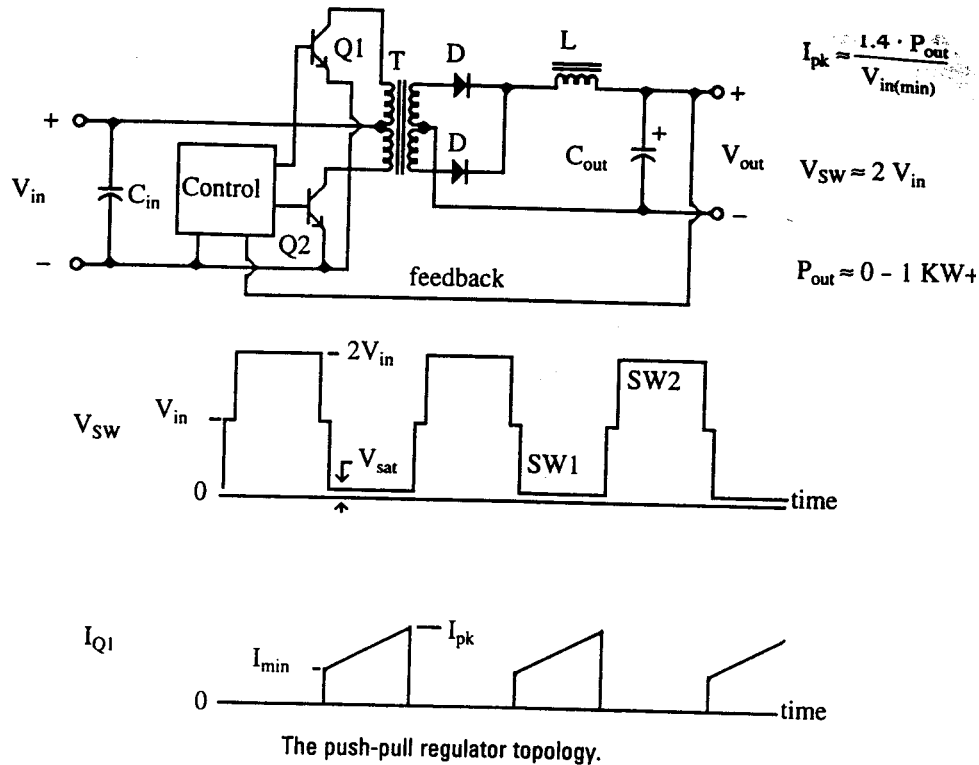**Estimating the Significant Minimum Parameters of the Power Semiconductors**

Topology	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
	V_{CEO}	I_C	V_{DSS}	I_D	V_R	I_F
Half-bridge	V_{in}	$\dfrac{2P_{out}}{V_{in(min)}}$	V_{in}	$\dfrac{2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Full-bridge	V_{in}	$\dfrac{1.2P_{out}}{V_{in(min)}}$	V_{in}	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}

Above the half and full bridge switch stress are estimated.

C.   Push-Pull Transformer Isolated Buck

1.   Circuit Topology and Timing

We first show a brief sketch of circuit waveforms in the push-pull circuit. The secondary is the same as the full bridge converter. Here however, the primary winding is also center-tapped.

$$I_{pk} \approx \frac{1.4 \cdot P_{out}}{V_{in(min)}}$$

$$V_{SW} \approx 2 \, V_{in}$$

$$P_{out} \approx 0 - 1 \, KW+$$

The push-pull regulator topology.

Notice that the switch voltage stress is nearly 2 V_{in} and the switches alternatively conduct the current to the two portions of the center tapped primary winding.When one switch is on the other is off. On the next page we rearrange the schematic and do a full blown analysis to capture circuit waveforms at $f_{sw}/2$, with full cycle duration of 2 T_{sw}.
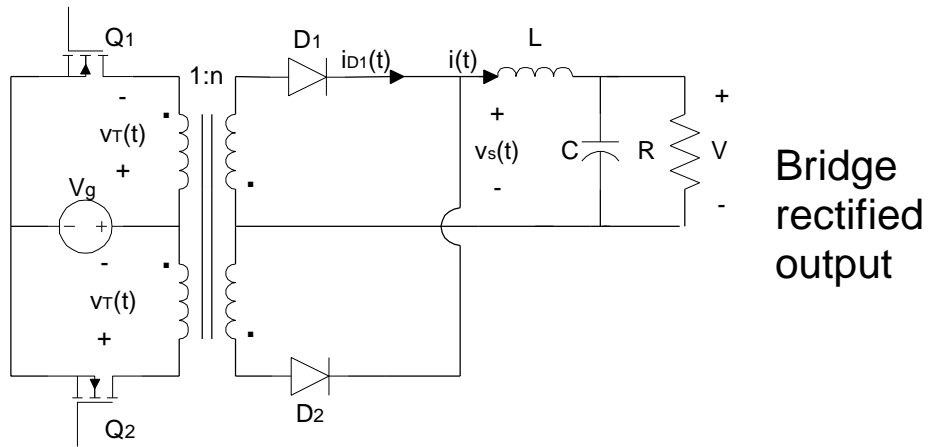
There are two periods of duration T_s per full cycle. In the first Q_1 is on for D while in the second Q_2 is on for D.

1st T_s	2nd T_s
Q_1 on for D putting $+V_g$	Q_2 on for D putting $+V_g$
on upper half of primary	on lower half of primary
but with + on un-dot side	with + on dotted side
Causes $+V_s$ on	Causes $+V_s$ on
upper right secondary	lower secondary

As regards the transformer L_m we find:

        1st T_s: Builds up i_m

        2nd T_s: Reduces i_m
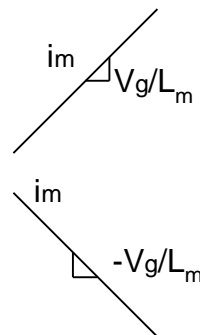
$V_o = nDV_g$ for DC conditions.

2. i and v waveforms vs $2T_s$

$$< V_{Lm} >_{2Ts} = 0$$
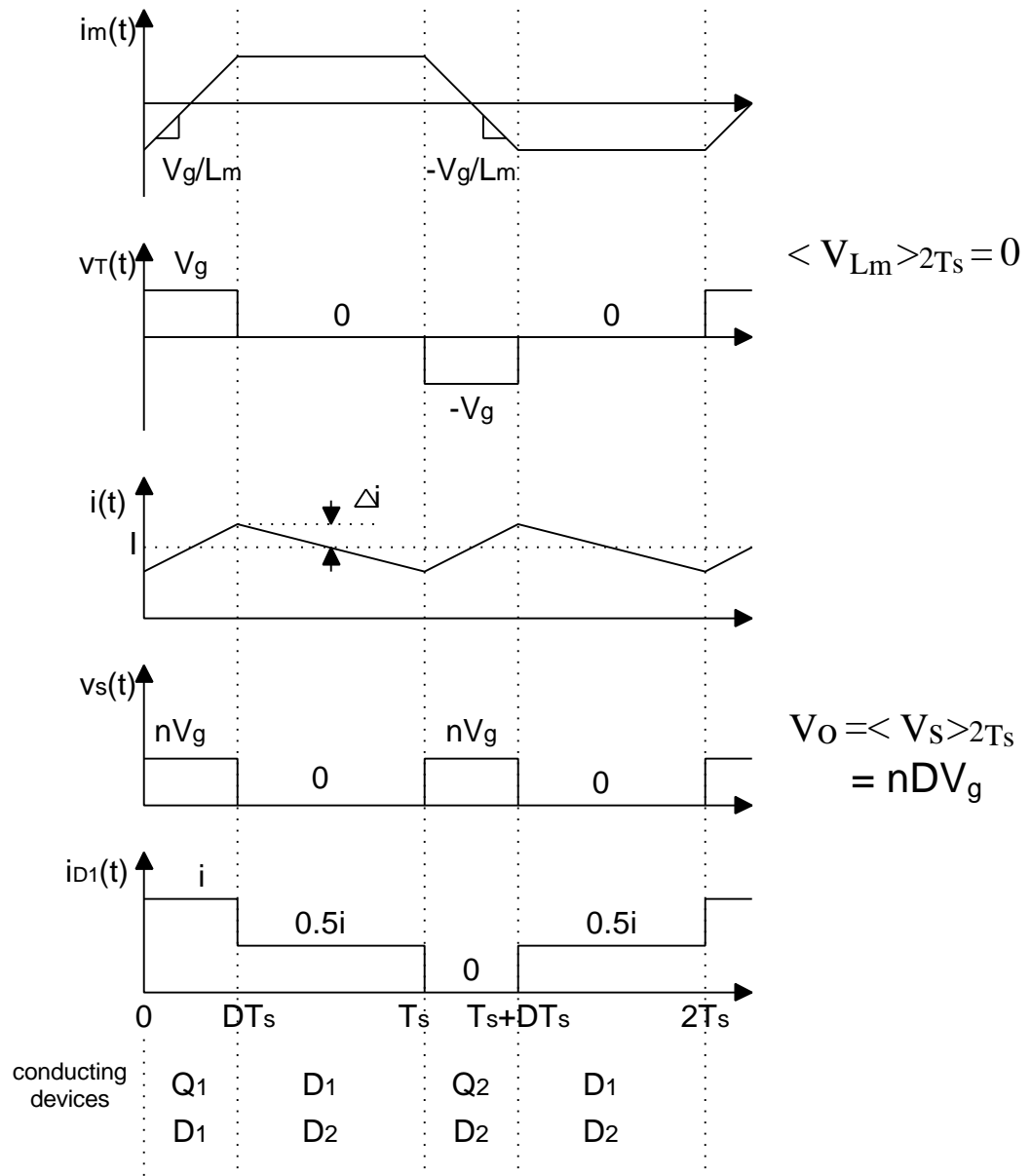
$$V_O = < V_S >_{2Ts}$$
$$= nDV_g$$

conducting devices	Q_1	D_1	Q_2	D_1
	D_1	D_2	D_2	D_2

Q_1 is on first T_s for DT_s and Q_2 is on second T_s for DT_s but are Q_1 and Q_2 the same? If not, What might occur? How we might avoid this core saturation is given below in section 3.

First we review the switch stress of the push-pull compared to the half and full bridge covered earlier.

Estimating the Significant Minimum Parameters of the Power Semiconductors

| Topology	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
	V_{CEO}	I_C	V_{DSS}	I_D	V_R	I_F
Push-pull	$2V_{in}$	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{in}$	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Half-bridge	V_{in}	$\dfrac{2P_{out}}{V_{in(min)}}$	V_{in}	$\dfrac{2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Full-bridge	V_{in}	$\dfrac{1.2P_{out}}{V_{in(min)}}$	V_{in}	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}

Note that the push-pull is equivalent to the full bridge in switch stress and better than the half bridge. However, the push-pull is a dangerous circuit as it has a tendency towards core saturation which will cause the transformer input to look like a short and will likely kill the switches. This arises when the flux within the core is inadvertently non-symmetric so that a small DC offset occurs. Unfortunately, this small offset will cause a walk towards saturation over many switch cycles. Usually, current mode feedback must be employed rather than voltage feedback to control this difficulty of push-pull. Also possible, is active core re-balancing as illustrated on the next page.

3.   Push-Pull Transformer Balance Problem

Load
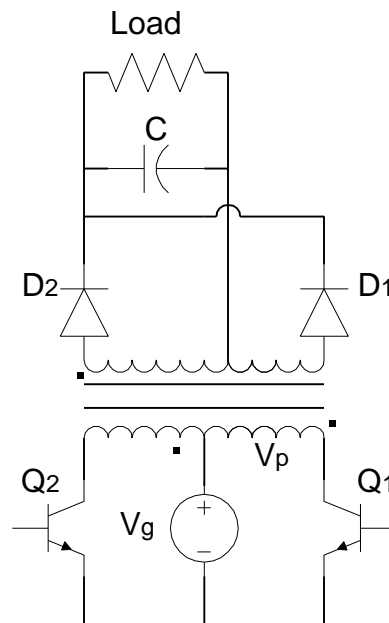
To monitor SATURATION of Transformer Core we will employ current sensors in Q_1 and Q_2 collector's to look for high current spikes.
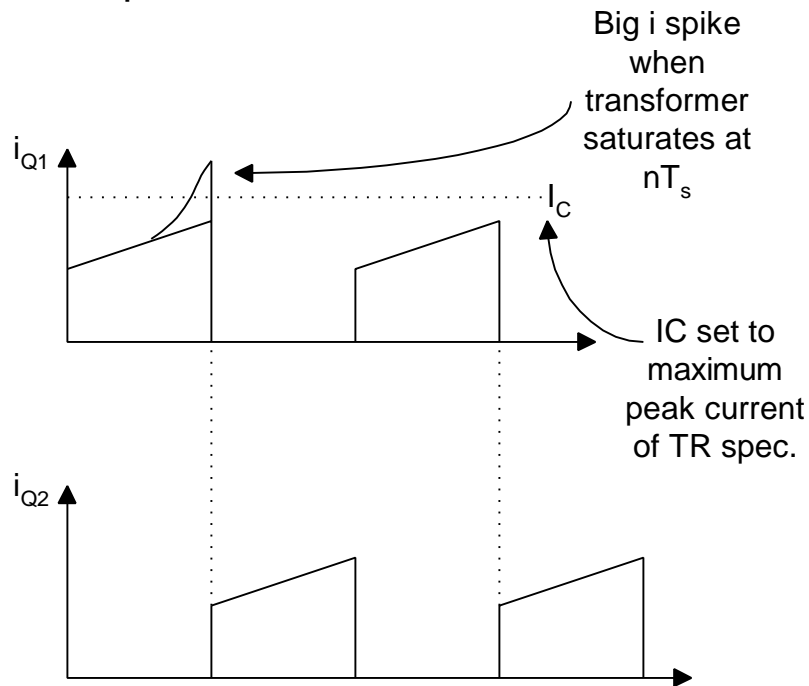
We compare to $I_{control}$(ref) and we shut off Q_1 and/or Q_2 if $I > I_{control}$.

Q_1 and Q_2 off Q_1 on Q_2 off

V_g

Q_1 on for DT_s Q_2 off

-Vg
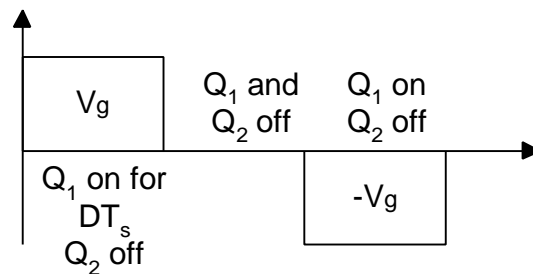
$$i_{Lm} = \frac{\int V_{Lm} dt}{Lm} \neq 0 \text{ over } T_S$$

Due $V_{on}(Q_1) \neq V_{on}(Q_2)$ and $\Delta t (Q_1) \neq \Delta t(Q_2)$ we might have a slight offset each clock cycle and i_{Lm} is not zero.

Even a small imbalance adds up after 100 switch periods and the transformer will ultimately saturate. Then for example the current on $i(Q_1)$ will shoot up when $L_m \to 0$

Big i spike
when
transformer
saturates at
nT_s

i_{Q1}

I_C

IC set to
maximum
peak current
of TR spec.

i_{Q2}

Use I_c(control) as a maximum to sense if i_{Q1} gets excessive and shut it down if it does. In practice we never build push pull converter with duty cycle control and voltage. Rather we use current programmed control of Chapter 11. Below we compare switch stress in the topologies of lectures 15 and 16.

Estimating the Significant Minimum Parameters of the Power Semiconductors

Topology	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
	V_{CEO}	I_C	V_{DSS}	I_D	V_R	I_F
Flyback	$1.7V_{in(max)}$	$\dfrac{2P_{out}}{V_{in(min)}}$	$1.5V_{in(max)}$	$\dfrac{2P_{out}}{V_{in(min)}}$	$10V_{out}$	I_{out}
One Transistor Forward	$2V_{in}$	$\dfrac{1.5P_{out}}{V_{in(min)}}$	$2V_{in}$	$\dfrac{1.5P_{out}}{V_{in(min)}}$	$3V_{out}$	I_{out}
Push-pull	$2V_{in}$	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{in}$	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Half-bridge	V_{in}	$\dfrac{2P_{out}}{V_{in(min)}}$	V_{in}	$\dfrac{2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Full-bridge	V_{in}	$\dfrac{1.2P_{out}}{V_{in(min)}}$	V_{in}	$\dfrac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}